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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70844ad80fpv

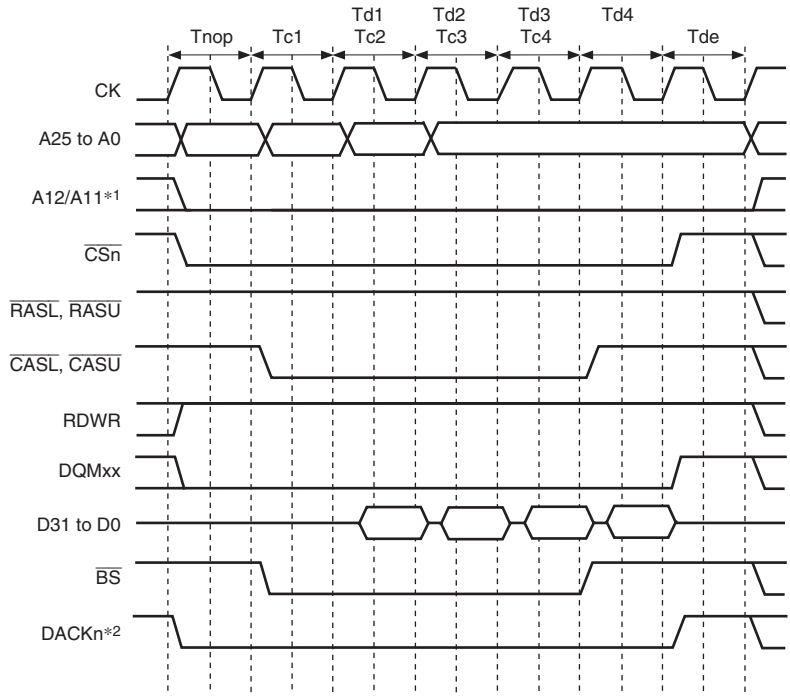
1.4 Pin Functions

Table 1.2 summarizes the pin functions.

Table 1.2 Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pins. Connect all Vcc pins to the system. There will be no operation if any pins are open.
	Vss	I	Ground	Ground pin. Connect all Vss pins to the system power supply (0V). There will be no operation if any pins are open.
	V_{CL}	O	Power supply for internal power-down	External capacitance pins for internal power-down power supply. Connect these pins to Vss via a 0.47 μF capacitor (placed close to the pins).
Clock	PLLVss	I	PLL ground	Ground pin for the on-chip PLL oscillator
	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
	CK	O	System clock	Supplies the system clock to external devices.
Operating mode control	MD1, MD0	I	Mode set	Sets the operating mode. Do not change values on these pins during operation.
	FWE	I	Flash memory write enable	Pin for flash memory. Flash memory can be protected against programming or erasure through this pin.

Bit	Bit Name	Initial Value	R/W	Description
14, 13	WTRP[1:0]	00	R/W	Number of Wait Cycles for Precharge Completion Specify the number of minimum wait cycles to be inserted for completion of precharge. • From activation of auto precharge to ACTV command issuance for the same bank. • From issuance of PRE/PALL command to ACTV command issuance for the same bank. • From PALL command issuance to REF command issuance in auto refresh. • From PALL command issuance to SELF command issuance in self-refresh. The setting for areas 2 and 3 is common. 00: 0 cycle (No wait cycles) 01: 1 cycle 10: 2 cycles 11: 3 cycles
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11, 10	WTRCD [1:0]	01	R/W	Number of Wait Cycles from ACTV Command to READ(A)/WRIT(A) Command Specify the number of minimum wait cycles from issuing ACTV command to issuing READ(A)/WRIT(A) command. The setting for areas 2 and 3 is common. 00: 0 cycle (No wait cycles) 01: 1 cycle 10: 2 cycles 11: 3 cycles
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.24 Burst Read Timing (Bank Active, Same Row Address)

A. Insert one idle cycle to access the interface other than the SDRAM interface after the write access cycle is performed in the SDRAM interface.
B. Insert one idle cycle to access the SDRAM interface after the normal space interface with the external wait invalidated or the byte-selection SRAM interface with the BAS bit = 0 specified is accessed.
C. Insert one idle cycle to access the SDRAM interface after the MPX-I/O interface is accessed.
D. Insert two idle cycles to access the MPX-I/O interface from the external bus that is in the idle status.
E. Insert one idle cycle to access the MPX-I/O interface after a read cycle is performed in the normal space interface, byte-selection SRAM interface with the BAS bit = 0, and the SDRAM interface.
F. Insert two idle cycles to access the MPX-I/O interface after a write cycle is performed in the SDRAM interface.

Tables 9.29 to 9.34 list the minimum number of idle cycles to be inserted for the normal space interface and the SDRAM interface. The CSnBCR Idle Setting column in the tables describes the number of idle cycles to be set for IWW, IWRWD, IWRWS, IWRRD, and IWRRS.

Table 9.30 Minimum Number of Idle Cycles between Access Cycles during DMAC Dual Address Mode and DTC Transfer for the Normal Space Interface

BSC Register Setting		When Access Size is Less than Bus Width		When Access Size Exceeds Bus Width			
CSnWCR. WM Setting	CSnBCR Idle Setting	Read to Write	Write to Read	Continuous Read*1	Read to Write*2	Continuous Write*1	Write to Read*2
1	0	2	0	0	2	0	0
0	0	2	1	1	2	1	1
1	1	2	1	1	2	1	1
0	1	2	1	1	2	1	1
1	2	2	2	2	2	2	2
0	2	2	2	2	2	2	2
1	4	4	4	4	4	4	4
0	4	4	4	4	4	4	4

Notes: DMAC and DTC are driven by Bϕ. The minimum number of idle cycles is not affected by changing a clock ratio.

1. Minimum number of idle cycles between the word access to address 0 and the word access to address 2 in the 32-bit access with a 16-bit bus width,
   minimum number of idle cycles between the byte access to address 0 and the byte access to address 1 in the 16-bit access with an 8-bit bus width,
   minimum number of idle cycles between the byte accesses to address 0, to address 1, to address 2, and to address 3 in the 32-bit access with an 8-bit bus width, and
   minimum number of idle cycles between consecutive accesses in 16-byte transfer.
2. Other than the above cases.

11.7.13 Counter Value during Complementary PWM Mode Stop

When counting operation is suspended with TCNT_3 and TCNT_4 in complementary PWM mode, TCNT_3 has the timer dead time register (TDDR) value, and TCNT_4 is held at H'0000.

When restarting complementary PWM mode, counting begins automatically from the initialized state. This explanatory diagram is shown in figure 11.132.

When counting begins in another operating mode, be sure that TCNT_3 and TCNT_4 are set to the initial values.

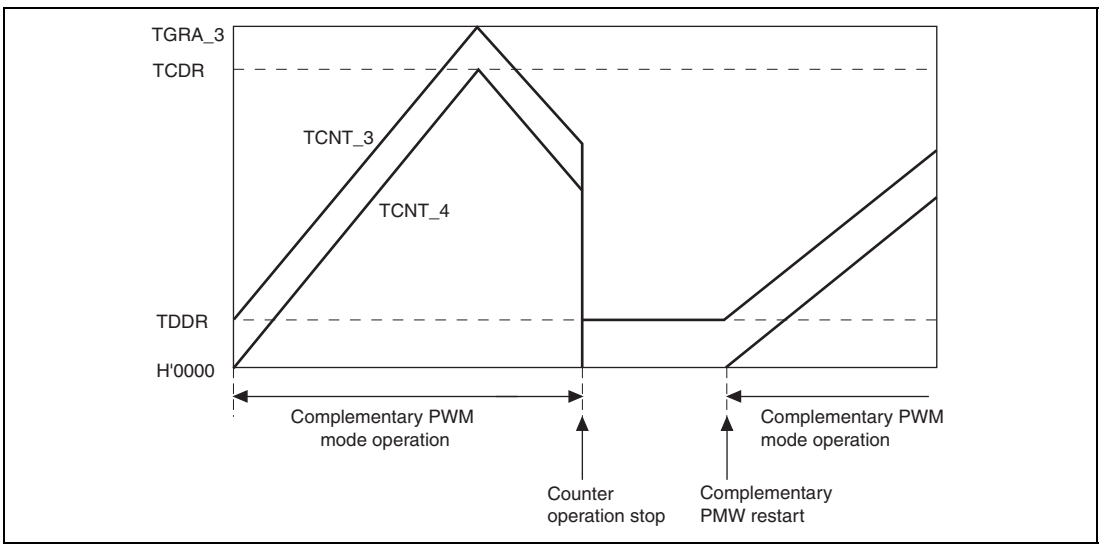


Figure 11.132 Counter Value during Complementary PWM Mode Stop

11.7.14 Buffer Operation Setting in Complementary PWM Mode

In complementary PWM mode, conduct rewrites by buffer operation for the PWM cycle setting register (TGRA_3), timer cycle data register (TCDR), and duty setting registers (TGRB_3, TGRA_4, and TGRB_4).

In complementary PWM mode, channel 3 and channel 4 buffers operate in accordance with bit settings BFA and BFB of TMDR_3. When TMDR_3's BFA bit is set to 1, TGRC_3 functions as a buffer register for TGRA_3. At the same time, TGRC_4 functions as the buffer register for TGRA_4, and TCBR functions as the TCDR's buffer register.

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Reset-Synchronized PWM Mode: Figure 11.146 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in reset-synchronized PWM mode after re-setting.

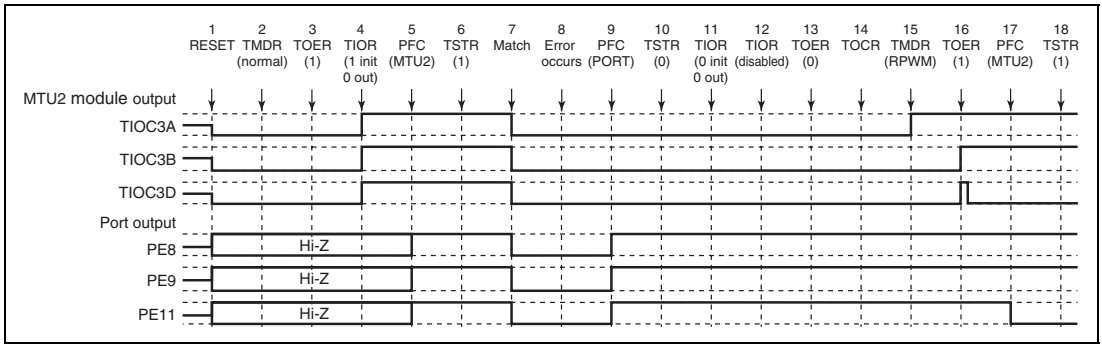


Figure 11.146 Error Occurrence in Normal Mode, Recovery in Reset-Synchronized PWM Mode

1 to 13 are the same as in figure 11.141.

14. Select the reset-synchronized PWM output level and cyclic output enabling/disabling with TOCR.
15. Set reset-synchronized PWM.
16. Enable channel 3 and 4 output with TOER.
17. Set MTU2 output with the PFC.
18. Operation is restarted by TSTR.

14.3 Register Descriptions

The WDT has the following two registers. Refer to section 27, List of Registers, for the details of the addresses of these registers and the state of registers in each operating mode.

Table 14.2 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Watchdog timer counter	WTCNT	R/W	H'00	H'FFFFE810	8, 16
Watchdog timer control/status register	WTCSR	R/W	H'00	H'FFFFE812	8, 16

14.3.1 Watchdog Timer Counter (WTCNT)

WTCNT is an 8-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a reset in watchdog timer mode and an interrupt in interval time mode. The WTCNT counter is not initialized by an internal reset due to the WDT overflow. The WTCNT counter is initialized to H'00 only by a power-on reset using the $\overline{\text{RES}}$ pin. Use a word access to write to the WTCNT counter, with H'5A in the upper byte. Use a byte access to read WTCNT.

Note: WTCNT differs from other registers in that it is more difficult to write to. See section 14.3.3, Notes on Register Access, for details.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 16.13 SCSMR Settings and SCIF Communication Formats

SCSMR Settings					SCIF Communication Format		
Bit 7 C/$\overline{A}$	Bit 6 CHR	Bit 5 PE	Bit 3 STOP	Mode	Data Length	Parity Bit	Stop Bit Length
0	0	0	0	Asynchronous	8-bit	Not set	1 bit
			1				2 bits
		1	0			Set	1 bit
			1				2 bits
	1	0	0		7-bit	Not set	1 bit
			1				2 bits
		1	0			Set	1 bit
			1				2 bits
1	x	x	x	Clock synchronous	8-bit	Not set	None

[Legend]

x: Don't care

Table 16.14 SCSMR and SCSCR Settings and SCIF Clock Source Selection

SCSMR	SCSCR Settings			SCIF Transmit/Receive Clock	
Bit 7 C/$\overline{A}$	Bit 1 CKE1	Bit 0 CKE0	Mode	Clock Source	SCK Pin Function
0	0	0	Asynchronous	Internal	SCIF does not use the SCK pin. The state of the SCK pin depends on both the SCKIO and SCKDT bits.
		1			Clock with a frequency 16 times the bit rate is output.
	1	0		External	Input a clock with frequency 16 times the bit rate.
		1		—	Setting prohibited.
1	0	x	Clock synchronous	Internal	Serial clock is output.
	1	0		External	Input the serial clock.
		1		—	Setting prohibited.

[Legend]

x: Don't care

17.4.6 $\overline{\text{SCS}}$ Pin Control and Conflict Error

When bits CSS1 and CSS0 in SSCRH are set to B'10 and the SSUMS bit in SSCRL is cleared to 0, the SCS pin becomes an input pin (Hi-Z) before the serial transfer is started and after the serial transfer is complete. Because of this, the SSU performs conflict error detection during these periods. If a low level signal is input to the SCS pin during these periods, it is detected as a conflict error. At this time, the CE bit in SSSR is set to 1 and the MSS bit is cleared to 0.

Note: While the CE bit is set to 1, transmission or reception is not resumed. Clear the CE bit to 0 before resuming the transmission or reception.

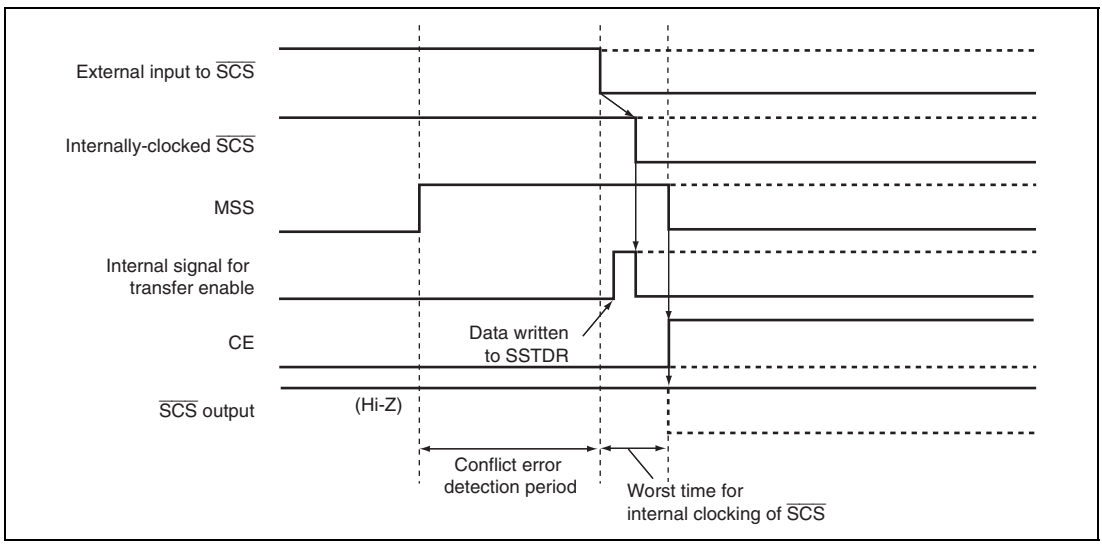


Figure 17.10 Conflict Error Detection Timing (Before Transfer)

Bit	Bit Name	Initial Value	R/W	Description
5	SDAO	1	R/W	SDA Output Value Control This bit is used with SDAOP when modifying output level of SDA. This bit should not be manipulated during transfer. 0: When reading, SDA pin outputs low. When writing, SDA pin is changed to output low. 1: When reading, SDA pin outputs high. When writing, SDA pin is changed to output Hi-Z (outputs high by external pull-up resistance).
4	SDAOP	1	R/W	SDAO Write Protect This bit controls change of output level of the SDA pin by modifying the SDAO bit. To change the output level, clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0. This bit is always read as 1.
3	SCLO	1	R	SCL Output Level This bit monitors SCL output level. When SCLO is 1, SCL pin outputs high. When SCLO is 0, SCL pin outputs low.
2	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
1	IICRST	0	R/W	IIC Control Part Reset IICRST resets the BC[2:0] bits in the ICMR register and the internal circuits of IIC2. If the MCU hangs because of a communication failure while the I²C bus is operating, the BC[2:0] bits in the ICMR register and the internal circuits of IIC2 can be reset by setting the IICRST bit to 1.
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

Notes: When 1 is written to the IICRST bit in ICCR2, the state becomes as follows.

- The SDAO and SCLO bits in ICCR2 are set to 1.
- If the module is in master transmit mode or slave transmit mode, the TDRE bit in ICSR is set to 1.
- Writing to the BBSY, SCP, and SDAO bits in ICCR2 is invalid while a reset is being applied by writing 1 to IICRST.

20.5.4 Conflict between Byte-Write and Count-Up Processes of CMCNT

Even when the count-up occurs in the T2 cycle while writing to CMCNT counter in bytes, the byte-writing has priority over the count-up. In this case, the count-up is not performed. The byte data on another side, which is not written to, is also not counted and the previous contents remain.

Figure 20.7 shows the timing when the count-up occurs in the T2 cycle while writing to CMCNT in bytes.

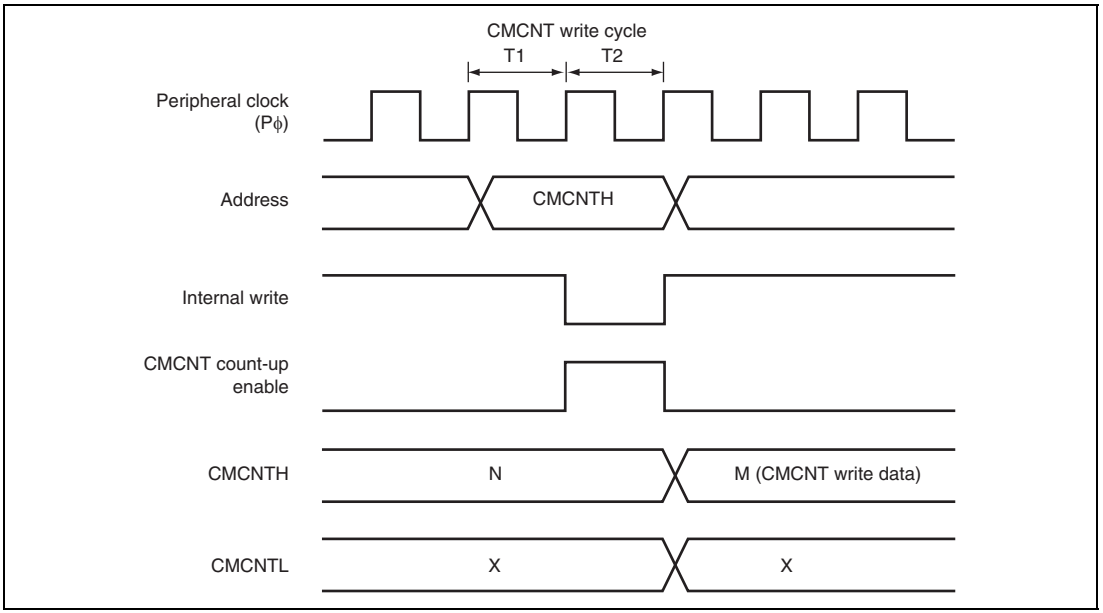


Figure 20.7 Conflict between Byte-Write and Count-Up Processes of CMCNT

20.5.5 Compare Match between CMCNT and CMCOR

Do not set the same value in CMCNT and CMCOR while CMCNT is not counting. If set, the CMF bit in CMCSR is set to 1 and CMCNT is cleared to H'0000.

- PAPRH (SH7086)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PA29 PR	PA28 PR	PA27 PR	PA26 PR	PA25 PR	PA24 PR	PA23 PR	PA22 PR	PA21 PR	PA20 PR	PA19 PR	PA18 PR	PA17 PR	PA16 PR
Initial value:	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	PA29PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
12	PA28PR	Pin state	R	
11	PA27PR	Pin state	R	
10	PA26PR	Pin state	R	
9	PA25PR	Pin state	R	
8	PA24PR	Pin state	R	
7	PA23PR	Pin state	R	
6	PA22PR	Pin state	R	
5	PA21PR	Pin state	R	
4	PA20PR	Pin state	R	
3	PA19PR	Pin state	R	
2	PA18PR	Pin state	R	
1	PA17PR	Pin state	R	
0	PA16PR	Pin state	R	

All commands in the above table, except for the boot program state inquiry command (H'4F), are valid until the boot program accepts the transition-to-programming/erasure state command (H'40). That is, until the transition command is accepted, the host can continue to send commands listed in the above table until it has made the necessary inquiries and selections. The host can send the boot program state inquiry command (H'4F) even after acceptance of the transition-to-programming/erasure state command (H'40) by the boot program.

(1) Inquiry on supported devices

In response to the inquiry on supported devices, the boot program returns the device codes of the devices it supports and the product names of their respective boot programs.

Command	H'20

— Command H'20 (1 byte): Inquiry on supported devices

Response	H'30	Size	No. of devices	
	Number of characters	Device code		Product name
	…			
	SUM			

— Response H'30 (1 byte): Response to the inquiry on supported devices

— Size (1 byte): The length of data for transfer excluding the command code, this field (size), and the checksum. Here, it is the total number of bytes taken up by the number of devices, number of characters, device code, and product name fields.

— Number of devices (1 byte): The number of device models supported by the boot program embedded in the microcomputer.

— Number of characters (1 byte): The number of characters in the device code and product name fields.

— Device code (4 bytes): Device code of a supported device (ASCII encoded)

— Product name (n bytes): Product code of the boot program (ASCII encoded)

— SUM (1 byte): Checksum
This is set so that the total sum of all bytes from the command code to the checksum is H'00.

— Response H'31 (1 byte): Response to the inquiry on clock modes
— Size (1 byte): The total length of the number of modes and mode data fields.
— Mode (1 byte): Selectable clock mode (example: H'01 denotes clock mode 1)
— SUM (1 byte): Checksum

(4) Clock-mode selection

In response to the clock-mode selection command, the boot program sets the specified clock mode. The boot program will return the information on the selected clock mode in response to subsequent inquiries.

Command	H'11	Size	Mode	SUM

— Command H'11 (1 byte): Clock mode selection
— Size (1 byte): Number of characters in the clock-mode field (fixed at 1)
— Mode (1 byte): A clock mode returned in response to the inquiry on clock modes
— SUM (1 byte): Checksum

Response	H'06

— Response H'06 (1 byte): Response to clock mode selection
The ACK code is returned when the specified clock-mode matches one of the available clock modes.

Error response	H'91	ERROR

— Error response H'91 (1 byte): Error response to clock mode selection
— ERROR (1 byte): Error code
H'11: Sum-check error
H'22: Non-matching clock mode

Table 23.18 (3) Usable Area for Programming in User Boot Mode (cont)

		Storable/Executable Area			Selected MAT		
	Item	On-Chip RAM	User Boot MAT	External Space	User MAT	User Boot MAT	Embedded Program Storage Area
Programming procedure	Setting programming parameters	√	X	√	√		
	Programming	√	X	X	√		
	Judging programming result	√	X	√	√		
	Programming error processing	√	X*2	√	√		
	Key register clearing	√	X	√	√		
	Switching MATs by FMATS	√	X	X		√	

Notes: 1. If the data has been transferred to on-chip RAM in advance, this area can be used.
2. If the MATs have been switched by FMATS in on-chip RAM, this MAT can be used.

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Deep Software Standby	Module Standby	Sleep	Module
PACRL2	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PACRL1	Initialized	Retained	Retained	Initialized	—	Retained	
PAPRH	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PAPRL	Initialized	Retained	Retained	Initialized	—	Retained	
PBDRL	Initialized	Retained	Retained	Initialized	—	Retained	
PBIORL	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PBCRL3	Initialized	Retained	Retained	Initialized	—	Retained	
PBCRL2	Initialized	Retained	Retained	Initialized	—	Retained	
PBCRL1	Initialized	Retained	Retained	Initialized	—	Retained	
PBPRL	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PCDRH	Initialized	Retained	Retained	Initialized	—	Retained	
PCDRL	Initialized	Retained	Retained	Initialized	—	Retained	
PCIORH	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PCIORL	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRH3	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRH2	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRH1	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL4	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL3	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL2	Initialized	Retained	Retained	Initialized	—	Retained	
PCCRL1	Initialized	Retained	Retained	Initialized	—	Retained	
PCPRH	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PCPRL	Initialized	Retained	Retained	Initialized	—	Retained	
PDDRH	Initialized	Retained	Retained	Initialized	—	Retained	
PDDRL	Initialized	Retained	Retained	Initialized	—	Retained	
PDIORH	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PDIORL	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH4	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH3	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH2	Initialized	Retained	Retained	Initialized	—	Retained	
PDCRH1	Initialized	Retained	Retained	Initialized	—	Retained	

Item	Page	Revision (See Manual for Details)
15.7.3 Break Detection and Processing	804	Description amended Break signals can be detected by reading the RXD pin directly when a framing error (FER) is detected. In the break state the input from the RXD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set. After a break is received, the SCI halts receive operation. At this time not only transfer of receive data from SCRSR to SCRDR stops; setting in SCRSR of serial data input on the RXD pin stops as well. To restart receive operation, input a high-level signal on the RXD pin, and clear the overrun error (ORER), FER, and PER flags.
15.7.4 Sending a Break Signal		Description amended To send a break signal during serial transmission, set the SPB0IO bit to 1 and clear the SPB0DT bit to 0 (low level), then clear the TE bit to 0 (halting transmission). When the TE bit is cleared to 0, the transmitter is initialized regardless of the current transmission state, and the low level is output from the TXD pin.
16.7.3 Break Detection and Processing	873	Description amended When data containing a framing error is received, and then space 0 (low level) is input for more than one frame length, a break (BRK) is detected. When a break is detected, not only the transfer of receive data (H'00) to SCFRDR but also the setting in SCRSR of serial data input on the RXD pin is stopped. If the RIE or REIE bit in SCSCR is set to 1, a break interrupt request (BRI) is issued. Reception resumes when the break ends and the receive signal is mark 1 (high level). It is also possible to perform break detection by reading the value of the RXD pin directly when a framing error (FER) is detected. Use the port register to read the value of the RXD pin. In the break state the input from the RXD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set.

Item	Page	Revision (See Manual for Details)
18.4.9 Example of Use Figure 18.20 Sample Flowchart for Master Transmit Mode	957	Figure amended