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Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70845ad80fpv

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SH7083, SH7084, SH7085, and SH7086 Group Manuals:

Document Title	Document No.
SH7080 Group Hardware Manual	This manual
SH-1/SH-2/SH-DSP Software Manual	REJ09B0171

User's Manuals for Development Tools:

Document Title	Document No.
SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package V.9.04 User's Manual	REJ10J2202
High-performance Embedded Workshop User's Manual	REJ10J2169

Application Note:

Document Title	Document No.
SuperH RISC engine C/C++ Compiler Package Application Note	REJ05B0463

9.4.3 CSn Space Wait Control Register (CSnWCR) (n = 0 to 8)

CSnWCR specifies various wait cycles for memory accesses. The bit configuration of this register varies as shown below according to the memory type (TYPE 2, TYPE 1, or TYPE 0) specified by the CSn space bus control register (CSnBCR). Specify CSnWCR before accessing the target area. CSnWCR should be modified only after CSnBCR setting is completed.

(1) Normal Space, SRAM with Byte Selection

- CS0WCR, CS1WCR, CS2WCR, CS3WCR, CS4WCR, CS5WCR, CS6WCR, CS7WCR, CS8WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	BAS	-	WW[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	SW[1:0]		WR[3:0]				WM	-	-	-	-	HW[1:0]	
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BAS	0	R/W	Byte Access Selection when SRAM with Byte Selection is Used Specifies the $\overline{\text{WRxx}}$ and RDWR signal timing when SRAM interface with byte selection is used. 0: Asserts the $\overline{\text{WRxx}}$ signal at the read/write timing and asserts the RDWR signal during the write access cycle. 1: Asserts the $\overline{\text{WRxx}}$ signal during the read/write access cycle and asserts the RDWR signal at the write timing.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

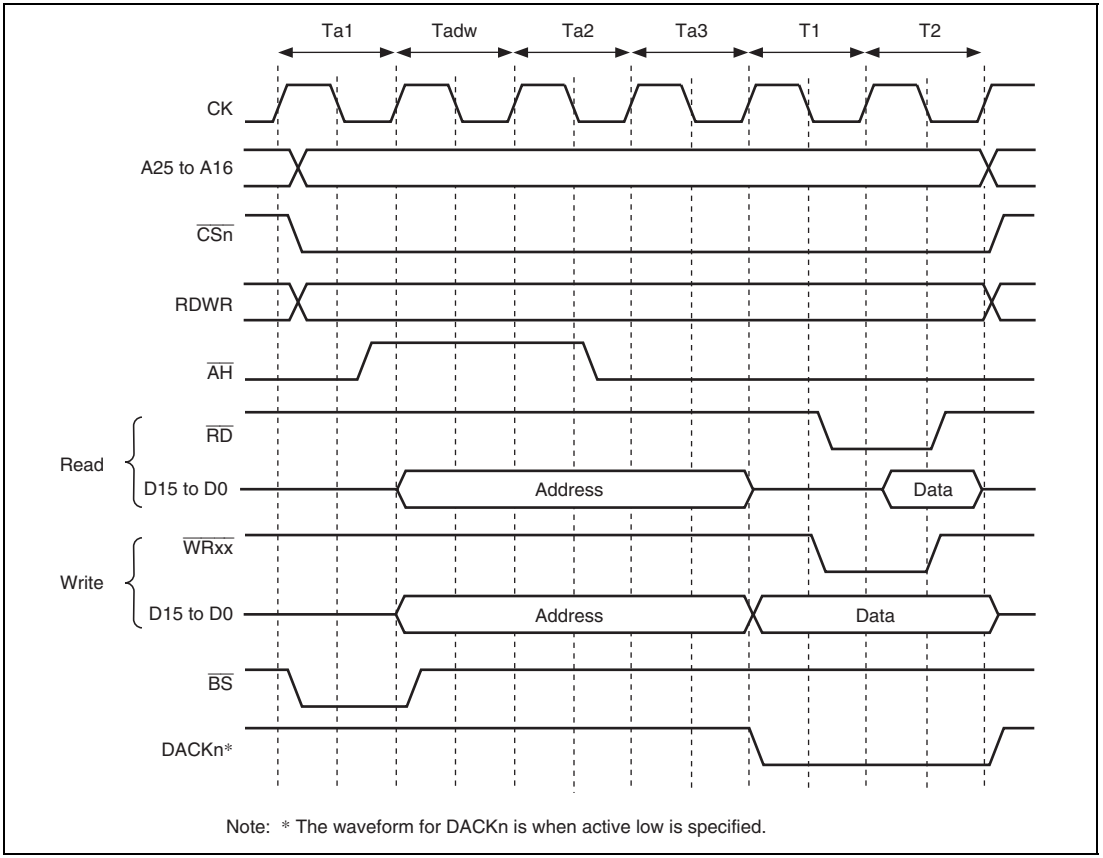


Figure 9.13 Access Timing for MPX Space (Address Cycle Wait 1, Data Cycle No Wait)

A. Insert one idle cycle to access the interface other than the SDRAM interface after the write access cycle is performed in the SDRAM interface.
B. Insert one idle cycle to access the SDRAM interface after the normal space interface with the external wait invalidated or the byte-selection SRAM interface with the BAS bit = 0 specified is accessed.
C. Insert one idle cycle to access the SDRAM interface after the MPX-I/O interface is accessed.
D. Insert two idle cycles to access the MPX-I/O interface from the external bus that is in the idle status.
E. Insert one idle cycle to access the MPX-I/O interface after a read cycle is performed in the normal space interface, byte-selection SRAM interface with the BAS bit = 0, and the SDRAM interface.
F. Insert two idle cycles to access the MPX-I/O interface after a write cycle is performed in the SDRAM interface.

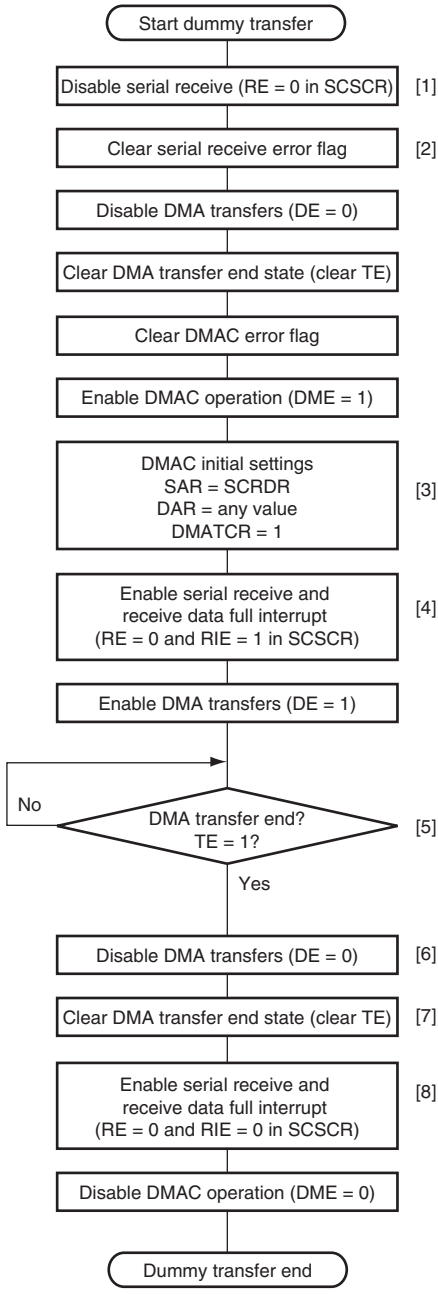
Tables 9.29 to 9.34 list the minimum number of idle cycles to be inserted for the normal space interface and the SDRAM interface. The CSnBCR Idle Setting column in the tables describes the number of idle cycles to be set for IWW, IWRWD, IWRWS, IWRRD, and IWRRS.

Table 9.30 Minimum Number of Idle Cycles between Access Cycles during DMAC Dual Address Mode and DTC Transfer for the Normal Space Interface

BSC Register Setting		When Access Size is Less than Bus Width		When Access Size Exceeds Bus Width			
CSnWCR. WM Setting	CSnBCR Idle Setting	Read to Write	Write to Read	Continuous Read*1	Read to Write*2	Continuous Write*1	Write to Read*2
1	0	2	0	0	2	0	0
0	0	2	1	1	2	1	1
1	1	2	1	1	2	1	1
0	1	2	1	1	2	1	1
1	2	2	2	2	2	2	2
0	2	2	2	2	2	2	2
1	4	4	4	4	4	4	4
0	4	4	4	4	4	4	4

Notes: DMAC and DTC are driven by Bϕ. The minimum number of idle cycles is not affected by changing a clock ratio.

1. Minimum number of idle cycles between the word access to address 0 and the word access to address 2 in the 32-bit access with a 16-bit bus width,
   minimum number of idle cycles between the byte access to address 0 and the byte access to address 1 in the 16-bit access with an 8-bit bus width,
   minimum number of idle cycles between the byte accesses to address 0, to address 1, to address 2, and to address 3 in the 32-bit access with an 8-bit bus width, and
   minimum number of idle cycles between consecutive accesses in 16-byte transfer.
2. Other than the above cases.



[1] [1] Disable serial receive so no interrupt (RXI) occurs during the transfer sequence.

[2] Clear the serial receive error flag. At this point, do not clear the interrupt source flag (RDRF in SCSSR).

[3] Initialize the DMAC. Set the DMA transfer count to 1 (DMATCR = 1).

[4] While serial receive remains disabled, enable the receive data full interrupt (RE = 0 and RIE = 1 in SCSCR).

[5] Wait for the DMA transfer to end. If the DEI interrupt is enabled (IE = 1), a DEI interrupt will be generated when the DMA transfer ends.

[6] Disable DMA transfers (DE = 0).

[7] Clear the DMA transfer end state (clear TE).

[8] Disable the receive data full interrupt (RIE = 0 in SCSCR) to disable interrupt requests.

Figure 10.23 Example Dummy Transfer Sequence (RXI)

11.3.2 Timer Mode Register (TMDR)

The TMDR registers are 8-bit readable/writable registers that are used to set the operating mode of each channel. The MTU2 has five TMDR registers, one each for channels 0 to 4. TMDR register settings should be changed only when TCNT operation is stopped.

Bit:	7	6	5	4	3	2	1	0
	-	BFE	BFB	BFA	MD[3:0]			
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value should always be 0.
6	BFE	0	R/W	Buffer Operation E Specifies whether TGRE_0 and TGRF_0 are to operate in the normal way or to be used together for buffer operation. Compare match with TGRF occurs even when TGRF is used as a buffer register. In channels 1 to 4, this bit is reserved. It is always read as 0 and the write value should always be 0. 0: TGRE_0 and TGRF_0 operate normally 1: TGRE_0 and TGRF_0 used together for buffer operation
5	BFB	0	R/W	Buffer Operation B*[1]*[2] Specifies whether TGRB is to operate in the normal way, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare do not take place in modes other than complementary PWM mode, but compare match with TGRD occurs in complementary PWM mode. Since the TGFD flag will be set if a compare match occurs during Tb interval in complementary PWM mode, the TGIED bit in timer interrupt enable register 3/4 (TIER_3/4) should be cleared to 0. In channels 1 and 2, which have no TGRD, bit 5 is reserved. It is always read as 0 and cannot be modified. 0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation

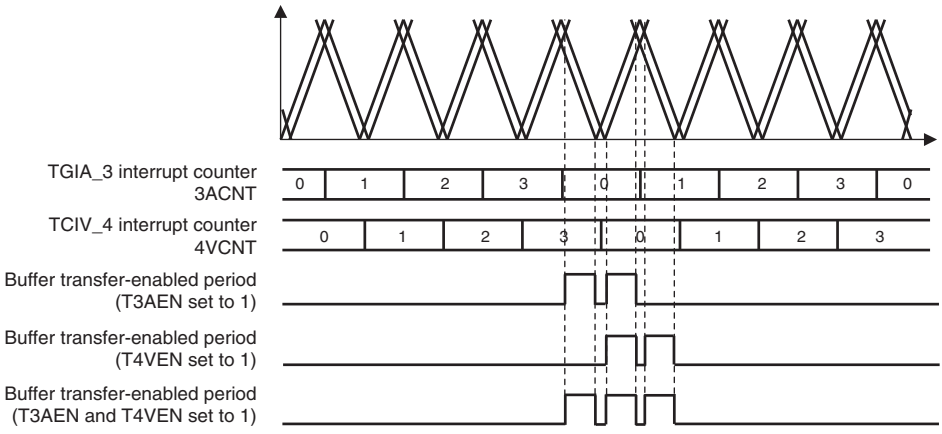
Bit	Bit Name	Initial Value	R/W	Description
6	TTGE2	0	R/W	A/D Converter Start Request Enable 2 Enables or disables generation of A/D converter start requests by TCNT_4 underflow (trough) in complementary PWM mode. In channels 0 to 3, bit 6 is reserved. It is always read as 0 and the write value should always be 0. 0: A/D converter start request generation by TCNT_4 underflow (trough) disabled 1: A/D converter start request generation by TCNT_4 underflow (trough) enabled
5	TCIEU	0	R/W	Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1 and 2. In channels 0, 3, and 4, bit 5 is reserved. It is always read as 0 and the write value should always be 0. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3	TGIED	0	R/W	TGR Interrupt Enable D Enables or disables interrupt requests (TGID) by the TGFD bit when the TGFD bit in TSR is set to 1 in channels 0, 3, and 4. In complementary PWM mode, clear the TGIED bit to 0 on channels 3 and 4. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and the write value should always be 0. 0: Interrupt requests (TGID) by TGFD bit disabled 1: Interrupt requests (TGID) by TGFD bit enabled

11.3.7 Timer Buffer Operation Transfer Mode Register (TBTM)

The TBTM registers are 8-bit readable/writable registers that specify the timing for transferring data from the buffer register to the timer general register in PWM mode. The MTU2 has three TBTM registers, one each for channels 0, 3, and 4.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	TTSE	TTSB	TTSA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TTSE	0	R/W	Timing Select E Specifies the timing for transferring data from TGRF_0 to TGRE_0 when they are used together for buffer operation. In channels 3 and 4, bit 2 is reserved. It is always read as 0 and the write value should always be 0. When using channel 0 in other than PWM mode, do not set this bit to 1. 0: When compare match E occurs in channel 0 1: When TCNT_0 is cleared
1	TTSB	0	R/W	Timing Select B Specifies the timing for transferring data from TGRD to TGRB in each channel when they are used together for buffer operation. When using a channel in other than PWM mode, do not set this bit to1. 0: When compare match B occurs in each channel 1: When TCNT is cleared in each channel



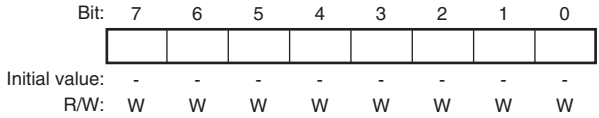
Note: Bits MD[3:0] in TMDR_3 are set to 1111, selecting buffer transfer at the crest and trough. The skipping count is set to three. T3AEN and T4VEN are set to 1.

Figure 11.78 Relationship between Bits T3AEN and T4VEN in Timer Interrupt Skipping Set Register (TITCR) and Buffer Transfer-Enabled Period

16.3.4 Transmit FIFO Data Register (SCFTDR)

SCFTDR is a 16-stage 8-bit FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves transmit data written in the SCFTDR into SCTSR and starts serial transmission. Continuous serial transmission is performed until there is no transmit data left in SCFTDR. SCFTDR can always be written to by the CPU.

When SCFTDR is full of transmit data (16 bytes), no more data can be written. If writing of new data is attempted, the data is ignored.

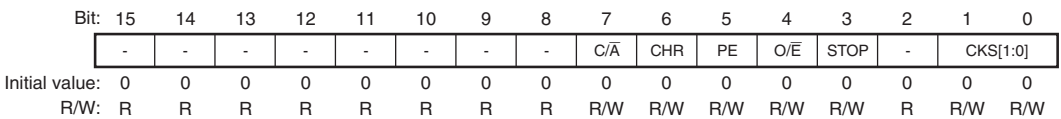


Bit	Bit Name	Initial value	R/W	Description
7 to 0		Undefined	W	FIFO for transmits serial data

16.3.5 Serial Mode Register (SCSMR)

SCSMR is a 16-bit register that specifies the SCIF serial communication format and selects the clock source for the baud rate generator.

The CPU can always read and write to SCSMR.



Bit	Bit Name	Initial value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Section 21 Pin Function Controller (PFC)

The pin function controller (PFC) is composed of registers that are used to select the functions of multiplexed pins and assign pins to be inputs or outputs. Tables 21.1 to 21.16 list the multiplexed pins of this LSI.

Tables 21.17 to 21.20 list the pin functions in each operating mode.

Table 21.1 SH7083 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA3 I/O (port)	A24 output (BSC)	RXD1 input (SCI)	—	—
	PA4 I/O (port)	A23 output (BSC)	TXD1 output (SCI)	—	—
	PA5 I/O (port)	A22 output (BSC)	DREQ1 input (DMAC)	IRQ1 input (INTC)	SCK1 I/O (SCI)
	PA7 I/O (port)	$\overline{\text{CS3}}$ output (BSC)	TCLKB input (MTU2)	—	—
	PA8 I/O (port)	RDWR output (BSC)	IRQ2 input (INTC)	TCLKC input (MTU2)	—
	PA9 I/O (port)	CKE output (BSC)	IRQ3 input (INTC)	TCLKD input (MTU2)	—
	PA10 I/O (port)	$\overline{\text{CS0}}$ output (BSC)	$\overline{\text{POE4}}$ input (POE)	—	—
	PA12 I/O (port)	$\overline{\text{WRL}}$/DQMLL output (BSC)	$\overline{\text{POE6}}$ input (POE)	—	—
	PA13 I/O (port)	$\overline{\text{WRH}}$/DQMLU output (BSC)	$\overline{\text{POE7}}$ input (POE)	—	—
	PA14 I/O (port)	$\overline{\text{RD}}$ output (BSC)	—	—	—
	PA15 I/O (port)	CK output (CPG)	—	—	—

Table 21.2 SH7084 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA0 I/O (port)	$\overline{\text{CS4}}$ output (BSC)	RXD0 input (SCI)	—	—
	PA1 I/O (port)	$\overline{\text{CS5}}$ output (BSC)	TXD0 output (SCI)	—	—
	PA2 I/O (port)	A25 output (BSC)	DREQ0 input (DMAC)	IRQ0 input (INTC)	SCK0 I/O (SCI)
	PA3 I/O (port)	A24 output (BSC)	RXD1 input (SCI)	—	—
	PA4 I/O (port)	A23 output (BSC)	TXD1 output (SCI)	—	—
	PA5 I/O (port)	A22 output (BSC)	DREQ1 input (DMAC)	IRQ1 input (INTC)	SCK1 I/O (SCI)
	PA6 I/O (port)	$\overline{\text{CS2}}$ output (BSC)	TCLKA input (MTU2)	—	—
	PA7 I/O (port)	$\overline{\text{CS3}}$ output (BSC)	TCLKB input (MTU2)	—	—

22.6 Port F

Port F in the SH7083, SH7084, and SH7085 is an input-only port with the 8 pins shown in figure 22.15.

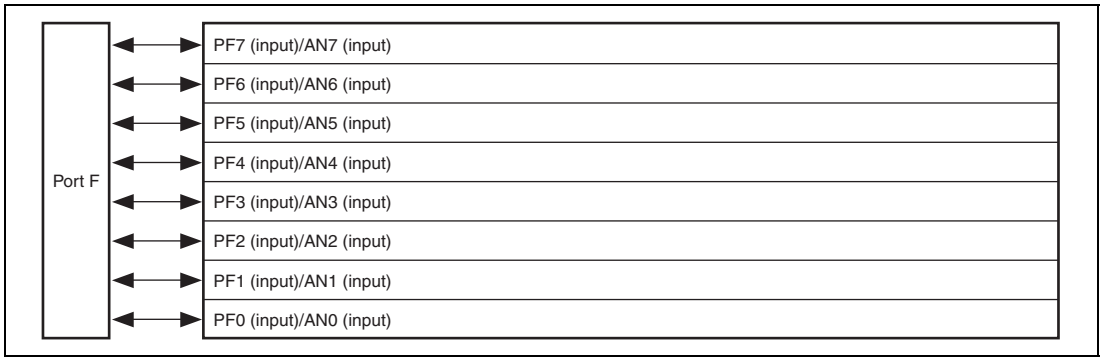


Figure 22.15 Port F (SH7083, SH7084, SH7085)

Port F in the SH7086 is an input-only port with the 16 pins shown in figure 22.16.

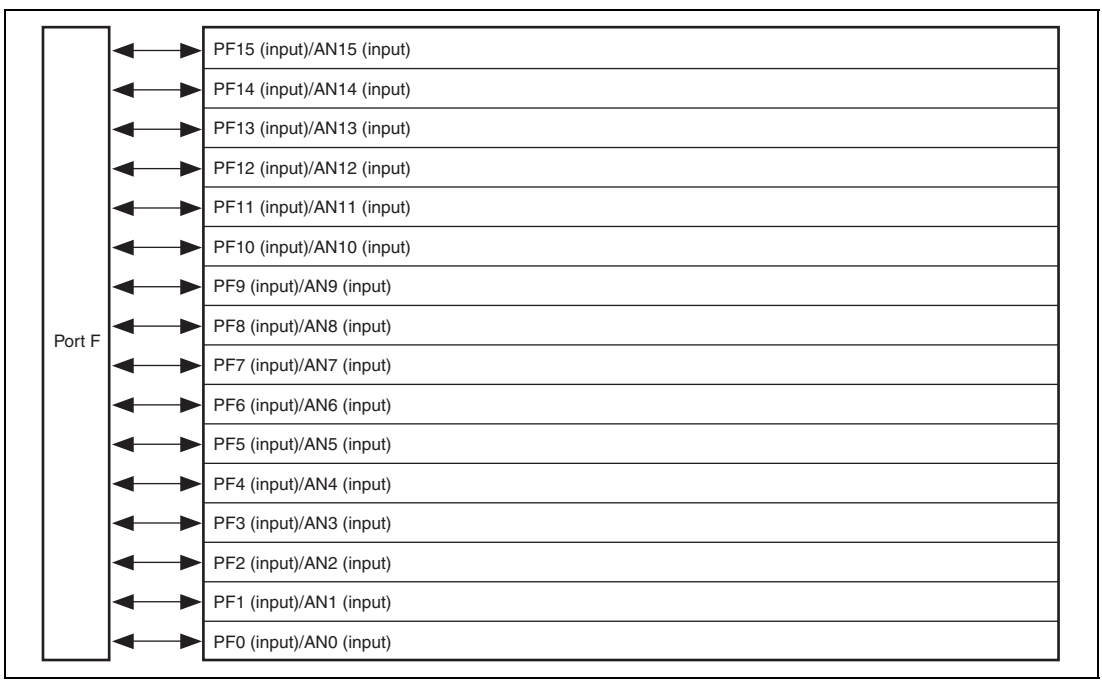


Figure 22.16 Port F (SH7086)

— During erase processing, ensure that no bus-mastership requests are issued by other than the interrupt and CPU bus masters. For details, see section 23.8.2, Interrupts during Programming/Erasing.

(3.4) The return value in the erasing program, FPFR (general register R0) is checked.

(3.5) Determine whether erasure of the necessary blocks has finished.

If more than one block is to be erased, update the FEBS parameter and repeat steps (3.2) to (3.5). Blocks that have already been erased can be erased again.

(3.6) After erasure finishes, clear FKEY and specify software protection.

If this LSI is restarted by a power-on reset immediately after user MAT erasing has finished, secure a reset period (period of $\overline{RES} = 0$) that is at least as long as the normal 100 μs.

(2) User MAT Programming in User Boot Mode

For programming the user MAT in user boot mode, additional processings made by setting FMATS are required: switching from user-boot-MAT selection state to user-MAT selection state, and switching back to user-boot-MAT selection state after programming completes.

Figure 23.14 shows the procedure for programming the user MAT in user boot mode.

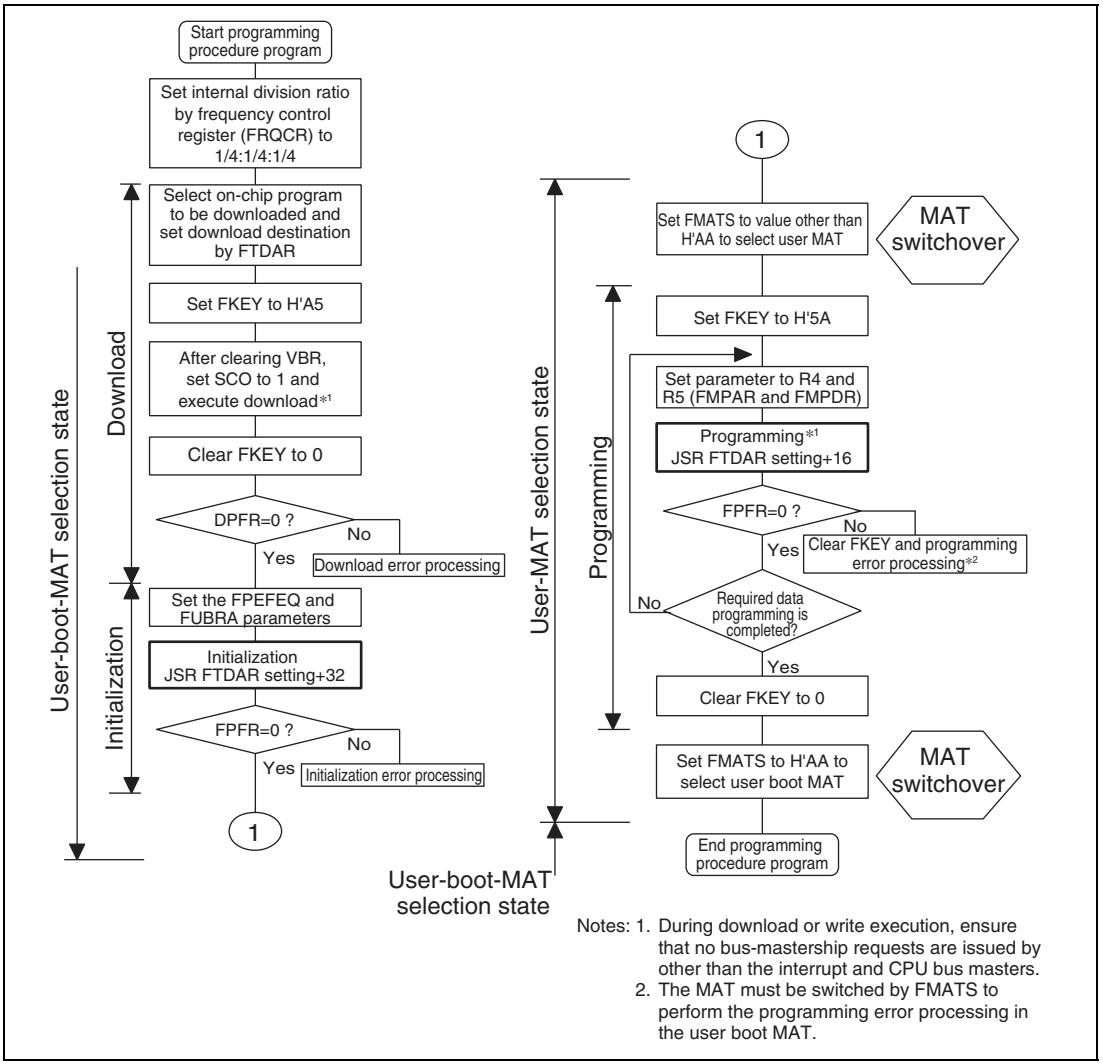
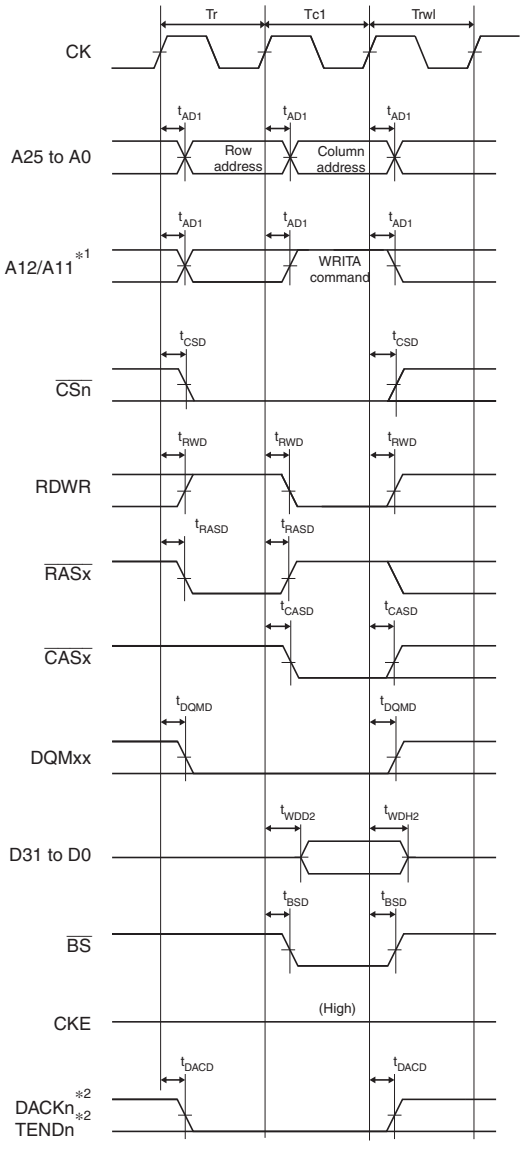
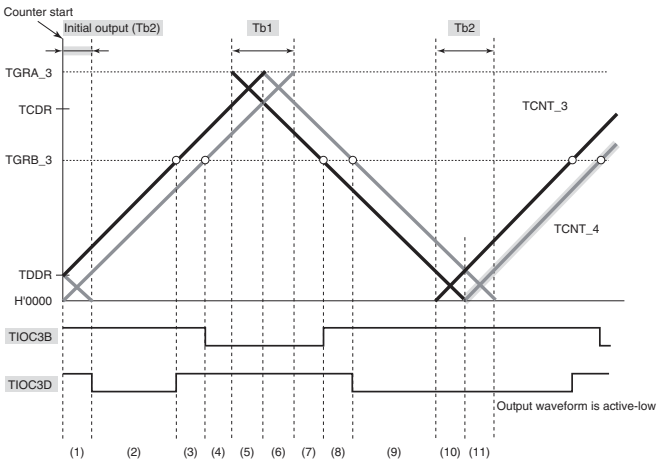


Figure 23.14 Procedure for Programming User MAT in User Boot Mode



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 28.28 Synchronous DRAM Single Write Bus Cycle (Auto Precharge, TRWL = 1 Cycle)

Item	Page	Revision (See Manual for Details)
11.4.8 Complementary PWM Mode (2) Outline of Complementary PWM Mode Operation (n) Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode	580	Description amended Setting the WRE bit in TWCR to 1 suppresses initial output when synchronous counter clearing occurs in the Tb2 interval in complementary PWM mode and controls abrupt change in duty cycle at synchronous counter clearing. Initial output suppression is applicable only when synchronous clearing occurs in the Tb2 interval as indicated by (10) or (11) in figure 11.56. When synchronous clearing occurs outside that interval, the initial value specified by the OLS bits in TOCR is output. Even in the Tb2 interval, if synchronous clearing occurs in the initial value output period (indicated by (1) in figure 11.56) immediately after the counters start operation, initial value output is not suppressed.
Figure 11.56 Timing for Synchronous Counter Clearing	581	Figure amended 
• Examples of Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode	582	Description amended In the MTU2S, these examples are equivalent to the cases when the MTU2S operates in complementary PWM mode and synchronous counter clearing is generated while the SCC bit is cleared to 0 and the WRE bit is set to 1 in TWCRS.