Renesas Electronics America Inc - DF70845AN80FPV Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70845an80fpv

Table 1.1 Features

Items	Specification
CPU	• Central processing unit with an internal 32-bit RISC (Reduced Instruction Set Computer) architecture • Instruction length: 16-bit fixed length for improved code efficiency • Load-store architecture (basic operations are executed between registers) • Sixteen 32-bit general registers • Five-stage pipeline • On-chip multiplier: Multiplication operations (32 bits × 32 bits → 64 bits) executed in two to five cycles • C language-oriented 62 basic instructions Note: Some specifications on slot illegal instruction exception handling in this LSI differ from those of the conventional SH-2. For details, see section 5.8.4, Notes on Slot Illegal Instruction Exception Handling.
Operating modes	• Operating modes — Single chip mode — Extended ROM enabled mode — Extended ROM disabled mode • Operating states — Program execution state — Exception handling state — Bus release state • Power-down modes — Sleep mode — Software standby mode — Deep software standby mode — Module standby mode
User break controller (UBC)	• Addresses, data values, type of access, and data size can all be set as break conditions • Supports a sequential break function • Two break channels
On-chip ROM	• 256 kbytes or 512 kbytes

5.1.2 Exception Handling Operations

The exceptions are detected and the exception handling starts according to the timing shown in table 5.2.

Table 5.2 Timing for Exception Detection and Start of Exception Handling

Exception		Timing of Source Detection and Start of Exception Handling
Reset	Power-on reset	Started when the $\overline{\text{RES}}$ pin changes from low to high or when the WDT overflows.
	Manual reset	Started when the $\overline{\text{MRES}}$ pin changes from low to high or when the WDT overflows.
Address error		Detected during the instruction decode stage and started after the execution of the current instruction is completed.
Interrupt		
Instruction	Trap instruction	Started by the execution of the TRAPA instruction.
	General illegal instructions	Started when an undefined code placed at other than a delay slot (immediately after a delayed branch instruction) is decoded.
	Illegal slot instructions	Started when an undefined code placed at a delay slot (immediately after a delayed branch instruction) or an instruction that changes the PC value is detected.

When exception handling starts, the CPU operates

Exception Handling Triggered by Reset: The initial values of the program counter (PC) and stack pointer (SP) are fetched from the exception handling vector table (PC from the address H'00000000 and SP from the address H'00000004 when a power-on reset. PC from the address H'00000008 and SP from the address H'0000000C when a manual reset.). For details, see section 5.1.3, Exception Handling Vector Table. H'00000000 is then written to the vector base register (VBR), and H'F (B'1111) is written to the interrupt mask bits (I3 to I0) in the status register (SR). The program starts from the PC address fetched from the exception handling vector table.

Exception Handling Triggered by Address Error, Interrupt, and Instruction: SR and PC are saved to the stack indicated by R15. For interrupt exception handling, the interrupt priority level is written to the interrupt mask bits (I3 to I0) in SR. For address error and instruction exception handling, bits I3 to I0 are not affected. The start address is then fetched from the exception handling vector table and the program starts from that address.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IPR[7:4]	0000	R/W	Set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
3 to 0	IPR[3:0]	0000	R/W	Set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)

Note: Name in the tables above is represented by a general name. Name in the list of register is, on the other hand, represented by a module name.

Bit	Bit Name	Initial Value	R/W	Description
15	SCMFCA	0	R/W	L Bus Cycle Condition Match Flag A When the L bus cycle condition in the break conditions set for channel A is satisfied, this flag is set to 1. In order to clear this flag, write 0 into this bit. 0: The L bus cycle condition for channel A does not match 1: The L bus cycle condition for channel A matches
14	SCMFCB	0	R/W	L Bus Cycle Condition Match Flag B When the L bus cycle condition in the break conditions set for channel B is satisfied, this flag is set to 1. In order to clear this flag, write 0 into this bit. 0: The L bus cycle condition for channel B does not match 1: The L bus cycle condition for channel B matches
13	SCMFDA	0	R/W	I Bus Cycle Condition Match Flag A When the I bus cycle condition in the break conditions set for channel A is satisfied, this flag is set to 1. In order to clear this flag, write 0 into this bit. 0: The I bus cycle condition for channel A does not match 1: The I bus cycle condition for channel A matches
12	SCMFDB	0	R/W	I Bus Cycle Condition Match Flag B When the I bus cycle condition in the break conditions set for channel B is satisfied, this flag is set to 1. In order to clear this flag, write 0 into this bit. 0: The I bus cycle condition for channel B does not match 1: The I bus cycle condition for channel B matches
11	PCTE	0	R/W	PC Trace Enable 0: Disables PC trace 1: Enables PC trace

The number of execution cycles is calculated from the formula below. Note that Σ means the sum of cycles for all transfers initiated by one activation event (the number of 1-valued CHNE bits in transfer information plus 1).

$$\text{Number of execution cycles} = I \bullet S_I + \Sigma (J \bullet S_J + K \bullet S_K + L \bullet S_L + M \bullet S_M) + N \bullet S_N$$

8.5.9 DTC Bus Release Timing

The DTC requests the bus mastership to the bus arbiter when an activation request occurs. The DTC releases the bus after a vector read, NOP cycle generation after a vector read, transfer information read, a single data transfer, or transfer information writeback. The DTC does not release the bus mastership during transfer information read, single data transfer, or transfer information writeback.
The bus release timing can be specified through the bus function extending register (BSCEHR). For details see section 9.4.8, Bus Function Extending Register (BSCEHR). The difference in bus release timing according to the register setting is summarized in table 8.11. Settings other than settings 1 to 5 are not allowed. The setting must not be changed while the DTC is active.

Figure 8.16 is a timing chart showing an example of bus release timing.

8.9.10 Conflict between NMI Interrupt and DTC Activation

When a conflict occurs between the generation of the NMI interrupt and the DTC activation, the NMI interrupt has priority. Thus the ERR bit is set to 1 and the DTC is not activated.

It takes 1 × Bcyc + 3 × Pcyc for determining DTC stop by NMI, 2 × Bcyc for determining DTC activation by IRQ, and 1 × Pcyc for determining DTC activation by peripheral modules.

8.9.11 Operation when a DTC Activation Request Is Cancelled While in Progress

Once the DTC has accepted an activation request, the DTC does not accept the next activation request until the sequence of DTC processing that ends with writeback has been completed.

As shown in figure 9.17, two sets of SDRAMs of 32 Mbytes or smaller can be connected to the same CS space by using $\overline{\text{RASU}}$, $\overline{\text{RASL}}$, $\overline{\text{CASU}}$, and $\overline{\text{CASL}}$. In this case, a total of 8 banks are assigned to the same CS space: 4 banks specified by $\overline{\text{RASL}}$ and $\overline{\text{CASL}}$, and 4 banks specified by $\overline{\text{RASU}}$ and $\overline{\text{CASU}}$. When accessing the address with A25 = 0, $\overline{\text{RASL}}$ and $\overline{\text{CASL}}$ are asserted. When accessing the address with A25 = 1, $\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ are asserted.

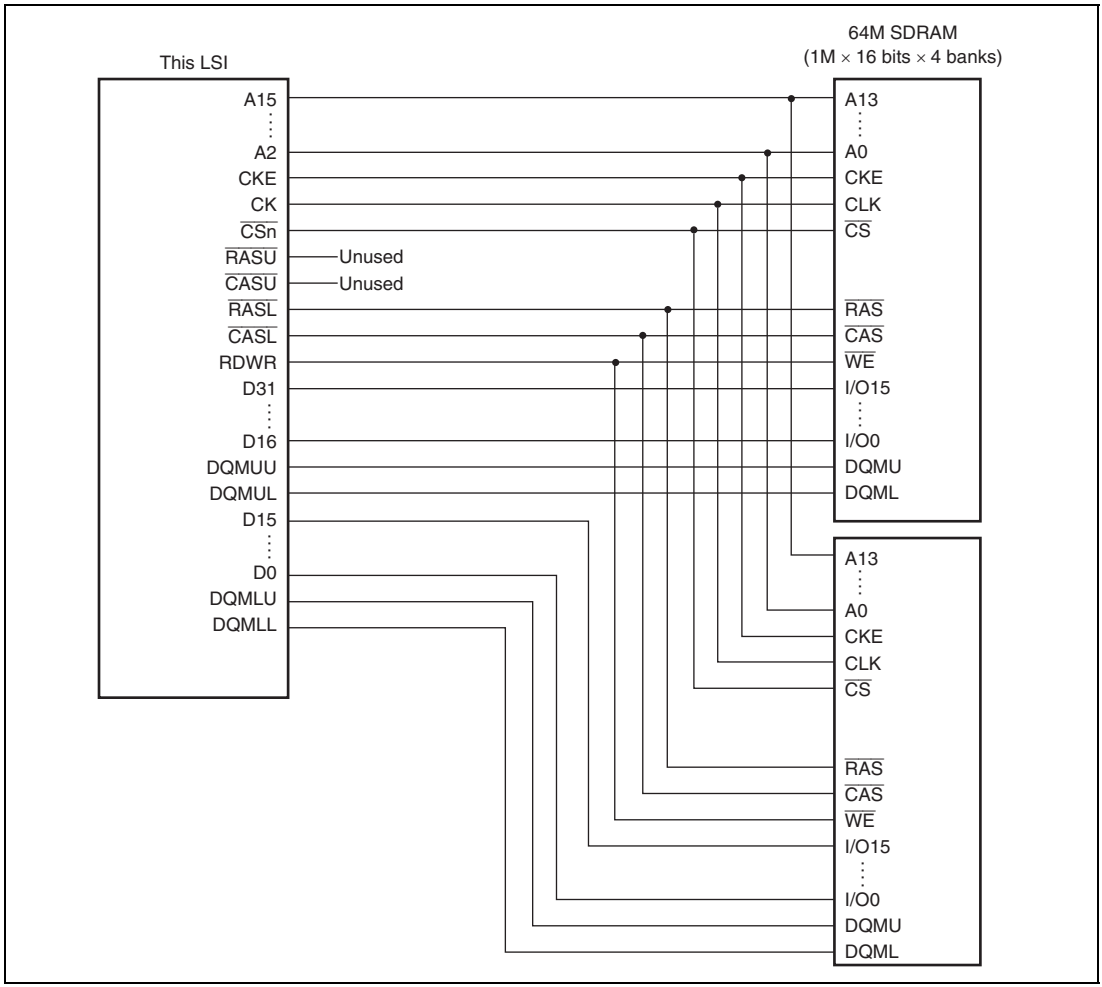
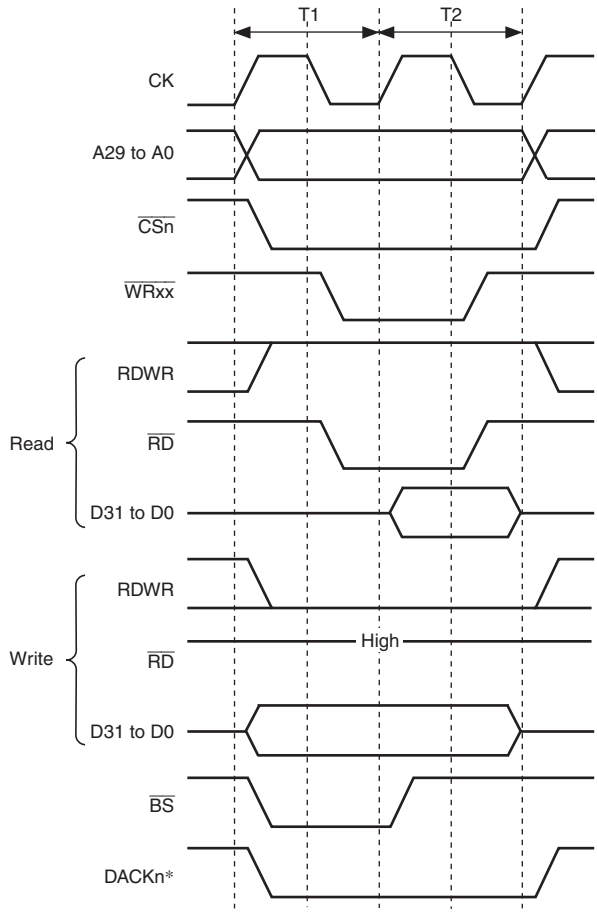


Figure 9.15 Example of 32-Bit Data Width SDRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ Are Not Used)



Note: * The waveform for DACKn is when active low is specified.

Figure 9.33 Basic Access Timing for SRAM with Byte Selection (BAS = 0)

10.4.5 Number of Bus Cycle States and DREQ Pin Sampling Timing

Number of Bus Cycle States: When the DMAC is the bus master, the number of bus cycle states is controlled by the bus state controller (BSC) in the same way as when the CPU is the bus master. For details, see section 9, Bus State Controller (BSC).

DREQ Pin Sampling Timing: Figures 10.14 to 10.17 show the sample timing of the DREQ input in each bus mode, respectively.
Determination of DMAC activation by DREQ takes 3 × Bcyc (Bcyc is the external clock (Bϕ = CK) cycle). Timing of the DACK output for the first DREQ acceptance differs depending on the internal bus state, the AM bit setting in CHCR, and the configuration of the BSC regarding the transfer source/destination areas, but the fastest case is 6 × Bcyc.

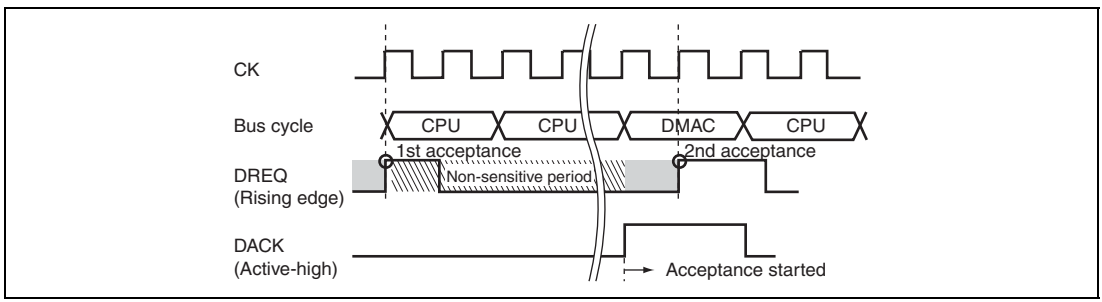


Figure 10.14 Example of DREQ Input Detection in Cycle Steal Mode Edge Detection

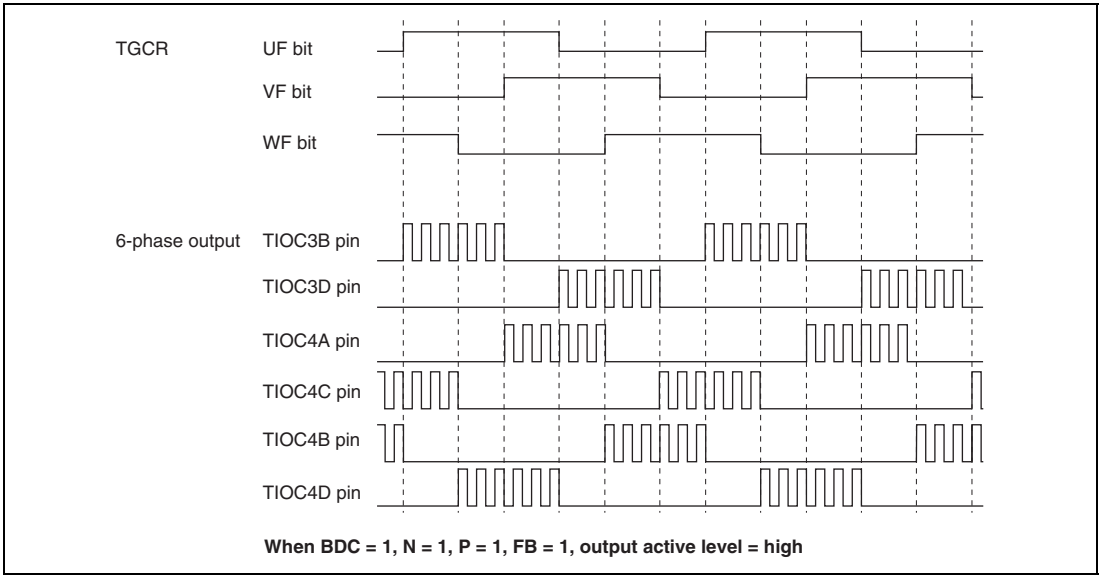


Figure 11.72 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings (2)

(r) A/D Converter Start Request Setting

In complementary PWM mode, an A/D converter start request can be issued using a TGRA_3 compare-match, or TCNT_4 underflow (trough).

When start requests using a TGRA_3 compare-match are specified, A/D conversion can be started at the crest of the TCNT_3 count.

A/D converter start requests can be set by setting the TTGE bit to 1 in the timer interrupt enable register (TIER). To issue an A/D converter start request at a TCNT_4 underflow (trough), set the TTGE2 bit in TIER_4 to 1.

For information on the A/D converter start request delaying function, see 11.4.9, A/D Converter Start Request Delaying Function.

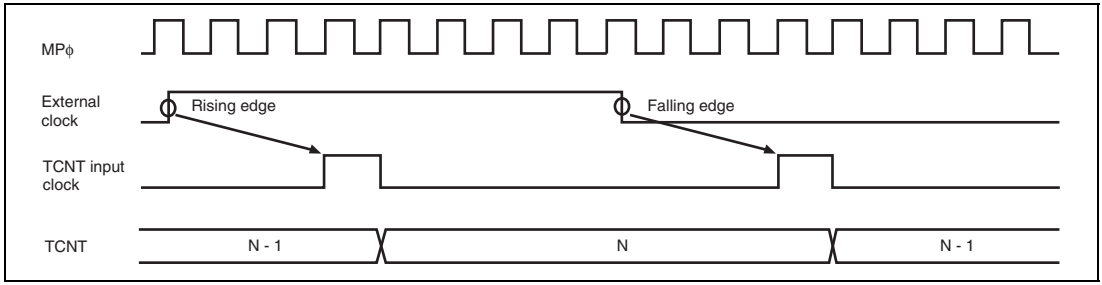


Figure 11.96 Count Timing in External Clock Operation (Phase Counting Mode)

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TIOR is output at the output compare output pin (TIOC pin). After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 11.97 shows output compare output timing (normal mode and PWM mode) and figure 11.98 shows output compare output timing (complementary PWM mode and reset synchronous PWM mode).

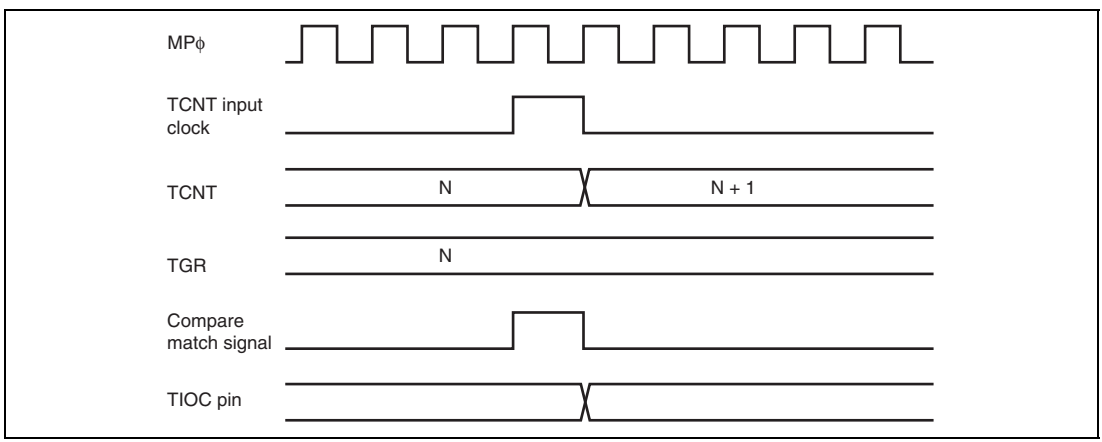


Figure 11.97 Output Compare Output Timing (Normal Mode/PWM Mode)

Bit	Bit Name	Initial value	R/W	Description
5, 4	POE2M[1:0]	00	R/W*[2]	POE2 mode 1, 0 These bits select the input mode of the $\overline{\text{POE2}}$ pin. 00: Accept request on falling edge of POE2 input 01: Accept request when POE2 input has been sampled for 16 Pϕ/8 clock pulses and all are low level. 10: Accept request when POE2 input has been sampled for 16 Pϕ/16 clock pulses and all are low level. 11: Accept request when POE2 input has been sampled for 16 Pϕ/128 clock pulses and all are low level.
3, 2	POE1M[1:0]	00	R/W*[2]	POE1 mode 1, 0 These bits select the input mode of the $\overline{\text{POE1}}$ pin. 00: Accept request on falling edge of POE1 input 01: Accept request when POE1 input has been sampled for 16 Pϕ/8 clock pulses and all are low level. 10: Accept request when POE1 input has been sampled for 16 Pϕ/16 clock pulses and all are low level. 11: Accept request when POE1 input has been sampled for 16 Pϕ/128 clock pulses and all are low level.
1, 0	POE0M[1:0]	00	R/W*[2]	POE0 mode 1, 0 These bits select the input mode of the $\overline{\text{POE0}}$ pin. 00: Accept request on falling edge of POE0 input 01: Accept request when POE0 input has been sampled for 16 Pϕ/8 clock pulses and all are low level. 10: Accept request when POE0 input has been sampled for 16 Pϕ/16 clock pulses and all are low level. 11: Accept request when POE0 input has been sampled for 16 Pϕ/128 clock pulses and all are low level.

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.
2. Can be modified only once after a power-on reset.

14.3 Register Descriptions

The WDT has the following two registers. Refer to section 27, List of Registers, for the details of the addresses of these registers and the state of registers in each operating mode.

Table 14.2 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Watchdog timer counter	WTCNT	R/W	H'00	H'FFFFE810	8, 16
Watchdog timer control/status register	WTCSR	R/W	H'00	H'FFFFE812	8, 16

14.3.1 Watchdog Timer Counter (WTCNT)

WTCNT is an 8-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a reset in watchdog timer mode and an interrupt in interval time mode. The WTCNT counter is not initialized by an internal reset due to the WDT overflow. The WTCNT counter is initialized to H'00 only by a power-on reset using the $\overline{\text{RES}}$ pin. Use a word access to write to the WTCNT counter, with H'5A in the upper byte. Use a byte access to read WTCNT.

Note: WTCNT differs from other registers in that it is more difficult to write to. See section 14.3.3, Notes on Register Access, for details.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

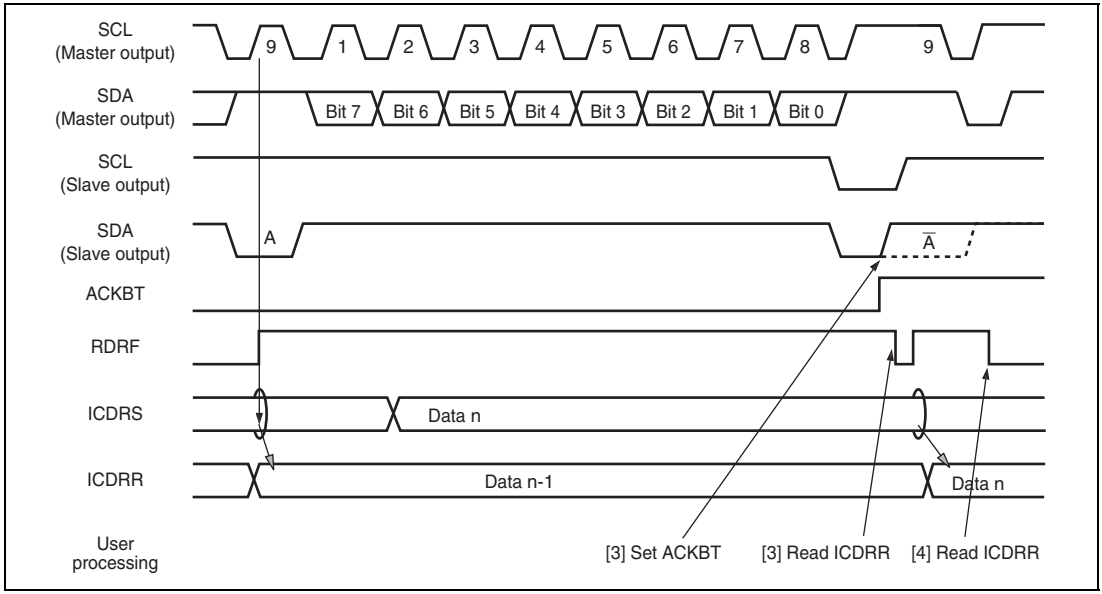


Figure 18.13 Slave Receive Mode Operation Timing (2)

18.4.6 Clock Synchronous Serial Format

This module can be operated with the clock synchronous serial format, by setting the FS bit in SAR to 1. When the MST bit in ICCR1 is 1, the transfer clock output from SCL is selected. When MST is 0, the external clock input is selected.

(1) Data Transfer Format

Figure 18.14 shows the clock synchronous serial transfer format.

The transfer data is output from the fall to the fall of the SCL clock, and the data at the rising edge of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in either the MSB first or LSB first. The output level of SDA can be changed during the transfer wait, by the SDAO bit in ICCR2.

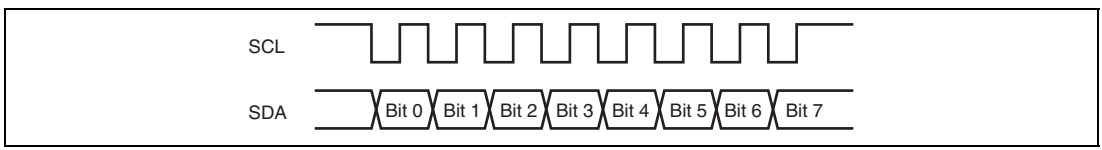


Figure 18.14 Clock Synchronous Serial Transfer Format (LSB-First Operation)

Bit	Bit Name	Initial Value	R/W	Description
4	PC5MD0	0*[1]	R/W	PC5 Mode Select the function of the PC5/A5 pin. 0: PC5 I/O (port) 1: A5 output (BSC)*[2]
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PC4MD0	0*[1]	R/W	PC4 Mode Select the function of the PC4/A4 pin. 0: PC4 I/O (port) 1: A4 output (BSC)*[2]

Notes: 1. The initial value is 1 in the on-chip ROM disabled external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

- Port C Control Register L1 (PCCRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	PC3MD0	-	-	-	PC2MD0	-	-	-	PC1MD0	-	-	-	PC0MD0
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	PC3MD0	0*[1]	R/W	PC3 Mode Select the function of the PC3/A3 pin. 0: PC3 I/O (port) 1: A3 output (BSC)*[2]
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- PEPRL (SH7083)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PE15PR	PE14PR	PE13PR	PE12PR	-	PE10PR	-	PE8PR	PE7PR	PE6PR	-	PE4PR	PE3PR	PE2PR	PE1PR	PE0PR
Initial value:	*	*	*	*	0	*	0	*	*	*	0	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	PE15PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
14	PE14PR	Pin state	R	
13	PE13PR	Pin state	R	
12	PE12PR	Pin state	R	
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PE10PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	PE8PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
7	PE7PR	Pin state	R	
6	PE6PR	Pin state	R	
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
4	PE4PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
3	PE3PR	Pin state	R	
2	PE2PR	Pin state	R	
1	PE1PR	Pin state	R	
0	PE0PR	Pin state	R	

The frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) is specified as ×1/4 (initial value) by the frequency control register (FRQCR).

After the programming/erasing program has been downloaded and the SCO bit is cleared to 0, the setting of the frequency control register (FRQCR) can be changed to the desired value.

For the downloaded on-chip program area, see the RAM map for programming/erasing in figure 23.10.

A single divided block is erased by one erasing processing. For block divisions, see figure 23.4. To erase two or more blocks, update the erase block number and perform the erasing processing for each block.

(3.1) Select the on-chip program to be downloaded

Set the EPVB bit in FECS to 1.

Several programming/erasing programs cannot be selected at one time. If several programs are set, download is not performed and a download error is returned to the source select error detect (SS) bit in the DPFR parameter.

Specify the start address of the download destination by FTDAR.

The procedures to be carried out after setting FKEY, e.g. download and initialization, are the same as those in the programming procedure. For details, see the description in section 23.5.2 (2), Programming Procedure in User Program Mode.

(3.2) Set the FEBS parameter necessary for erasure

Set the erase block number of the user MAT in the flash erase block select parameter (FEBS: general register R4). If a value other than an erase block number of the user MAT is set, no block is erased even though the erasing program is executed, and an error is returned to the return value parameter FPFR.

(3.3) Erasure

Similar to as in programming, there is an entry point of the erasing program in the area from (download start address set by FTDAR) + 16 bytes of on-chip RAM. The subroutine is called and erasing is executed by using the following steps.

```
MOV.L  #DLTOP+16,R1          ; Set entry address to R1
JSR    @R1                   ; Call erasing routine
NOP
```

— The general registers other than R0 are saved in the erasing program.

— R0 is a return value of the FPFR parameter.

— Since the stack area is used in the erasing program, a stack area of maximum 128 bytes must be reserved in RAM.

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Deep Software Standby	Module Standby	Sleep	Module
SSTDR3	Initialized	Retained	Initialized	Initialized	Initialized	Retained	SSU
SSRDR0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SSRDR1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SSRDR2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SSRDR3	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
CMSTR	Initialized	Retained	Initialized	Initialized	Initialized	Retained	CMT
CMCSR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
CMCNT_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
CMCOR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
CMCSR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
CMCNT_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
CMCOR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
ICSR1	Initialized	Retained	Retained	Initialized	—	Retained	POE
OCSR1	Initialized	Retained	Retained	Initialized	—	Retained	
ICSR2	Initialized	Retained	Retained	Initialized	—	Retained	
OCSR2	Initialized	Retained	Retained	Initialized	—	Retained	
ICSR3	Initialized	Retained	Retained	Initialized	—	Retained	
SPOER	Initialized	Retained	Retained	Initialized	—	Retained	
POECR1	Initialized	Retained	Retained	Initialized	—	Retained	
POECR2	Initialized	Retained	Retained	Initialized	—	Retained	
PADRH	Initialized	Retained	Retained	Initialized	—	Retained	I/O
PADRL	Initialized	Retained	Retained	Initialized	—	Retained	
PAIORH	Initialized	Retained	Retained	Initialized	—	Retained	PFC
PAIORL	Initialized	Retained	Retained	Initialized	—	Retained	
PACRH4	Initialized	Retained	Retained	Initialized	—	Retained	
PACRH3	Initialized	Retained	Retained	Initialized	—	Retained	
PACRH2	Initialized	Retained	Retained	Initialized	—	Retained	
PACRH1	Initialized	Retained	Retained	Initialized	—	Retained	
PACRL4	Initialized	Retained	Retained	Initialized	—	Retained	
PACRL3	Initialized	Retained	Retained	Initialized	—	Retained	

		External Space (SDRAM)		
		16-bit Space		
Pin Name		**Upper Byte**	**Lower Byte**	**Word/Longword**
$\overline{AH}$		L	L	L
$\overline{FRAME}$		H	H	H
RDWR	R	H	H	H
	W	L	L	L
$\overline{RD}$	R	H	H	H
	W	H	H	H
$\overline{ICIORD}$	R	H	H	H
	W	H	H	H
$\overline{WRHH}$	R	H	H	H
	W	H	H	H
$\overline{WRHL}$	R	H	H	H
	W	H	H	H
$\overline{WRH}$	R	H	H	H
	W	H	H	H
$\overline{WRL}$	R	H	H	H
	W	H	H	H
$\overline{WE}$	R	H	H	H
	W	H	H	H
$\overline{ICIOWR}$	R	H	H	H
	W	H	H	H
A29 to A0		Address	Address	Address
D31 to D24		Hi-Z	Hi-Z	Hi-Z
D23 to D16		Hi-Z	Hi-Z	Hi-Z
D15 to D8		Data	Hi-Z	Data
D7 to D0		Hi-Z	Data	Data

[Legend]

R: Read

W: Write

Notes: 1. Chip select signals corresponding to accessed areas = Low.
The other chip select signals = High.

2. $\overline{RASL}/\overline{CASL}$ = Low when address wherein A25 = 0 is accessed. $\overline{RASU}/\overline{CASU}$ = Low when address wherein A25 = 1 is accessed.