Renesas Electronics America Inc - DF70854AD80FPV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	100
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70854ad80fpv

5.6 Cases when Exceptions Are Accepted

When an exception other than resets occurs during decoding the instruction placed in a delay slot or immediately after an interrupt disabled instruction, it may not be accepted and be held shown in table 5.10. In this case, when an instruction which accepts an interrupt request is decoded, the exception is accepted.

Table 5.10 Delay Slot Instructions, Interrupt Disabled Instructions, and Exceptions

	Exception				
Occurrence Timing	**Address Error**	**General Illegal Instruction**	**Slot Illegal Instruction**	**Trap Instruction**	**Interrupt**
Instruction in delay slot	×*2	—	×*2	—	×*3
Immediately after interrupt disabled instruction*1	√	√	√	√	×*4

[Legend]

√: Accepted

×: Not accepted

—: Does not occur

Notes: 1. Interrupt disabled instructions: LDC, LDC.L, STC, STC.L, LDS, LDS.L, STS, and STS.L

2. An exception is accepted before the execution of a delayed branch instruction. However, when an address error or a slot illegal instruction exception occurs in the delay slot of the RTE instruction, correct operation is not guaranteed.

3. An exception is accepted after a delayed branch (between instructions in the delay slot and the branch destination).

4. An exception is accepted after the execution of the next instruction of an interrupt disabled instruction (before the execution two instructions after an interrupt disabled instruction).

Bit	Bit Name	Initial Value	R/W	Description
8	IRQ0L	*	R	Indicates the state of pin IRQ0. 0: State of pin IRQ0 is low 1: State of pin IRQ0 is high
7	IRQ7F	0	R/W	Indicates the status of an IRQ7 interrupt request. • When level detection mode is selected 0: An IRQ7 interrupt has not been detected [Clearing condition] Driving pin IRQ7 high 1: An IRQ7 interrupt has been detected [Setting condition] Driving pin IRQ7 low • When edge detection mode is selected 0: An IRQ7 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ7F = 1 — Accepting an IRQ7 interrupt 1: An IRQ7 interrupt request has been detected [Setting condition] Detecting the specified edge of pin IRQ7

9.4.1 Common Control Register (CMNCR)

CMNCR is a 32-bit register that controls the common items for each area.

Do not access external memory other than area 0 until the register initialization is complete.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	DMAIW[1:0]		DMAIWA	-	-	-	HIZMEM	HIZCNT
Initial value:	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7, 6	DMAIW[1:0]	00	R/W	Wait Specification between Access Cycles during DMA Single Address Transfer Specify the number of idle cycles to be inserted after data is output from an external device with DACK when DMA single address transfer is performed. The method of inserting idle cycles depends on the setting in the DMAIWA bit described later. 00: No idle cycle inserted 01: 1 idle cycle inserted 10: 2 idle cycles inserted 11: 4 idle cycled inserted

Bit	Bit Name	Initial Value	R/W	Description
9, 8	PR[1:0]	00	R/W	Priority Mode 1, 0 Select the priority level between channels when there are transfer requests for multiple channels simultaneously. 00: CH0 > CH1 > CH2 > CH3 01: CH0 > CH2 > CH3 > CH1 10: Setting prohibited 11: Round-robin mode
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error occurred during DMA transfer. If this bit is set, DMA transfer is disabled even if the DE bit in CHCR and the DME bit in DMAOR are set to 1. This bit can only be cleared by writing 0 after reading 1. 0: No DMAC address error [Clearing condition] • Writing AE = 0 after AE = 1 read 1: DMAC address error occurs

Bit	Bit Name	Initial Value	R/W	Description
1	NMIF	0	R/(W)*	NMI Flag Indicates that an NMI interrupt occurred. If this bit is set, DMA transfer is disabled even if the DE bit in CHCR and the DME bit in DMAOR are set to 1. This bit can only be cleared by writing 0 after reading 1. When the NMI is input, the DMA transfer in progress can be done in one transfer unit. When the DMAC is not in operational, the NMIF bit is set to 1 even if the NMI interrupt was input. 0: No NMI interrupt [Clearing condition] • Writing NMIF = 0 after NMIF = 1 read 1: NMI interrupt occurs Note: If the NMIF bit is read at the same point in time that it is set to 1, in some cases the read value will be 0 but the internal state will be as if it was read as 1. Therefore, subsequently writing 0 to NMIF will clear it to 0 in the same way as writing 0 to the flag after reading it as 1. To prevent the NMIF bit from being cleared to 0 inadvertently, always write 1 to the NMIF bit except in cases when explicitly clearing it. To explicitly clear the NMIF bit, write 0 to it after reading it as 1. Note that if the NMIF bit is not used, there is no problem with always writing 0 to it (and writing 0 to it after reading it as 1 explicitly to clear it).
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfers on all channels. If the DME bit and the DE bit in CHCR are set to 1, transfer is enabled. In this time, all of the bits TE in CHCR, NMIF, and AE in DMAOR must be 0. If this bit is cleared during transfer, transfers in all channels are terminated. 0: Disables DMA transfers on all channels 1: Enables DMA transfers on all channels

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

10.3.6 Bus Function Extending Register (BSCEHR)

BSCEHR is a 16-bit readable/writable register that specifies the timing of bus release. It also sets the function to perform transfer by the DMAC preferentially. For details, see section 9.4.8, Bus Function Extending Register (BSCEHR).

11.3.2 Timer Mode Register (TMDR)

The TMDR registers are 8-bit readable/writable registers that are used to set the operating mode of each channel. The MTU2 has five TMDR registers, one each for channels 0 to 4. TMDR register settings should be changed only when TCNT operation is stopped.

Bit:	7	6	5	4	3	2	1	0
	-	BFE	BFB	BFA	MD[3:0]			
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value should always be 0.
6	BFE	0	R/W	Buffer Operation E Specifies whether TGRE_0 and TGRF_0 are to operate in the normal way or to be used together for buffer operation. Compare match with TGRF occurs even when TGRF is used as a buffer register. In channels 1 to 4, this bit is reserved. It is always read as 0 and the write value should always be 0. 0: TGRE_0 and TGRF_0 operate normally 1: TGRE_0 and TGRF_0 used together for buffer operation
5	BFB	0	R/W	Buffer Operation B*[1]*[2] Specifies whether TGRB is to operate in the normal way, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare do not take place in modes other than complementary PWM mode, but compare match with TGRD occurs in complementary PWM mode. Since the TGFD flag will be set if a compare match occurs during Tb interval in complementary PWM mode, the TGIED bit in timer interrupt enable register 3/4 (TIER_3/4) should be cleared to 0. In channels 1 and 2, which have no TGRD, bit 5 is reserved. It is always read as 0 and cannot be modified. 0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation

11.8.4 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation, etc.

- When making a transition to a mode (Normal, PWM1, PWM2, PCM) in which the pin output level is selected by the timer I/O control register (TIOR) setting, initialize the pins by means of a TIOR setting.
- In PWM mode 1, since a waveform is not output to the TIOC*B (TIOC *D) pin, setting TIOR will not initialize the pins. If initialization is required, carry it out in normal mode, then switch to PWM mode 1.
- In PWM mode 2, since a waveform is not output to the cycle register pin, setting TIOR will not initialize the pins. If initialization is required, carry it out in normal mode, then switch to PWM mode 2.
- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, setting TIOR will not initialize the buffer register pins. If initialization is required, clear buffer mode, carry out initialization, then set buffer mode again.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, setting TIOR will not initialize the TGRC pin. To initialize the TGRC pin, clear buffer mode, carry out initialization, then set buffer mode again.
- When making a transition to a mode (CPWM, RPWM) in which the pin output level is selected by the timer output control register (TOCR) setting, switch to normal mode and perform initialization with TIOR, then restore TIOR to its initial value, and temporarily disable channel 3 and 4 output with the timer output master enable register (TOER). Then operate the unit in accordance with the mode setting procedure (TOCR setting, TMDR setting, TOER setting).

Note: Channel number is substituted for * indicated in this article.

Section 13 Port Output Enable (POE)

The port output enable (POE) can be used to place the high-current pins (pins multiplexed with TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D in the MTU2 and TIOC3BS, TIOC3DS, TIOC4AS, TIOC4BS, TIOC4CS, and TIOC4DS in the MTU2S) and the pins for channel 0 of the MTU2 (pins multiplexed with TIOC0A, TIOC0B, TIOC0C, and TIOC0D) in high-impedance state, depending on the change on $\overline{\text{POE0}}$ to $\overline{\text{POE8}}$ input pins and the output status of the high-current pins, or by modifying register settings. It can also simultaneously generate interrupt requests.

13.1 Features

- Each of the $\overline{\text{POE0}}$ to $\overline{\text{POE8}}$ input pins can be set for falling edge, Pϕ/8 × 16, Pϕ/16 × 16, or Pϕ/128 × 16 low-level sampling.
- High-current pins and the pins for channel 0 of the MTU2 can be placed in high-impedance state by $\overline{\text{POE0}}$ to $\overline{\text{POE8}}$ pin falling-edge or low-level sampling.
- High-current pins can be placed in high-impedance state when the high-current pin output levels are compared and simultaneous active-level output continues for one cycle or more.
- High-current pins and the pins for channel 0 of the MTU2 can be placed in high-impedance state by modifying the POE register settings.
- Interrupts can be generated by input-level sampling or output-level comparison results.

The POE has input level detection circuits, output level comparison circuits, and a high-impedance request/interrupt request generating circuit as shown in figure 13.1.

In addition to control by the POE, high-current pins can be placed in high-impedance state when the oscillator stops or in software standby state. For details, refer to section 21.1.11, High-Current Port Control Register (HCPCR), and appendix A, Pin States.

Figure 13.1 shows a block diagram of the POE.

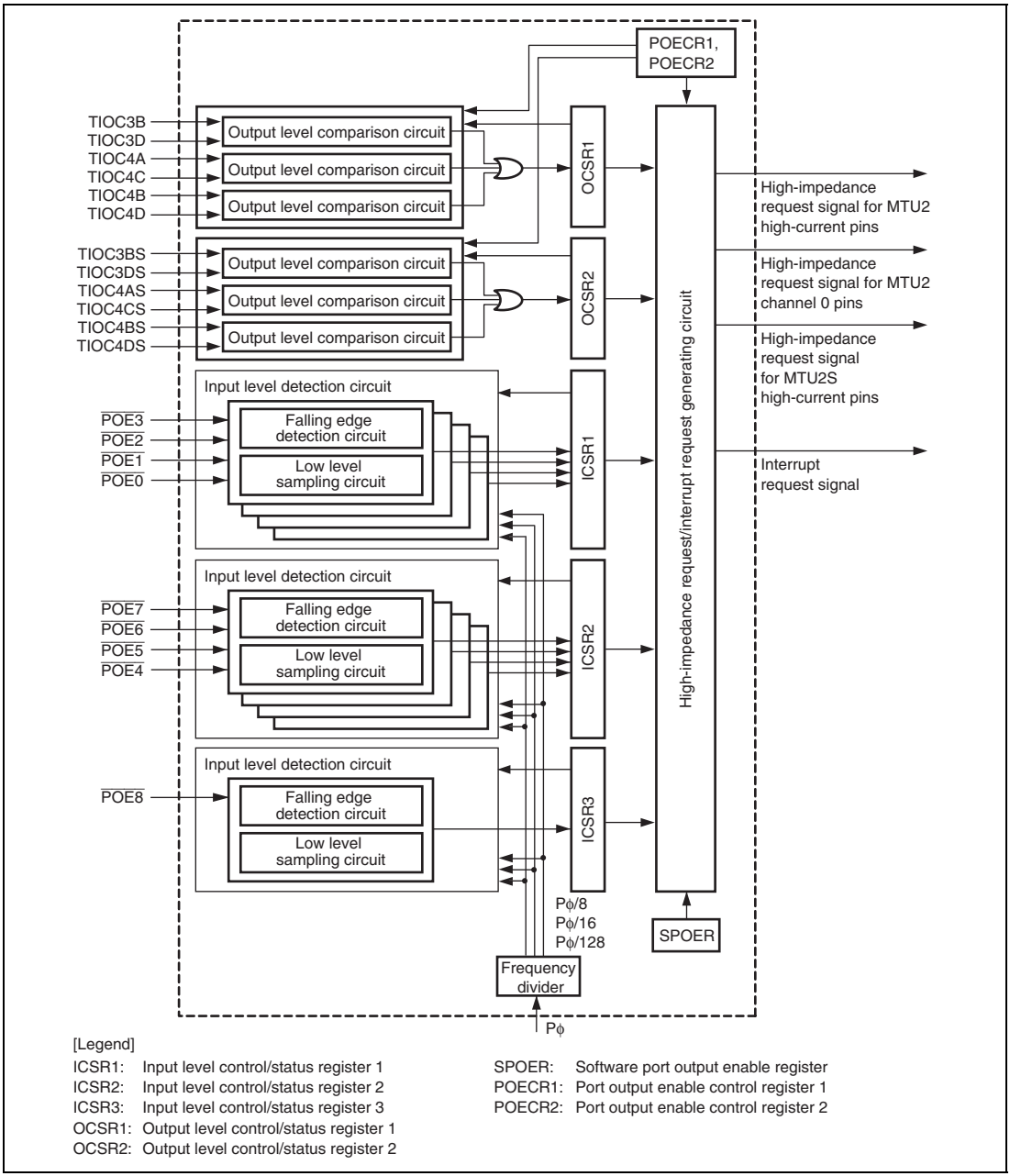


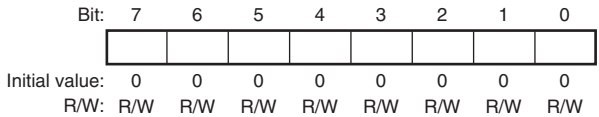
Figure 13.1 Block Diagram of POE

17.3.7 SS Transmit Data Registers 0 to 3 (SSTDR0 to SSTDR3)

SSTDR is an 8-bit register that stores transmit data. When 8-bit data length is selected by bits DATS1 and DATS0 in SSCRL, SSTDR0 is valid. When 16-bit data length is selected, SSTDR0 and SSTDR1 are valid. When 32-bit data length is selected, SSTDR0 to SSTDR3 are valid. Do not access SSTDR that is not valid.

When the SSU detects that SSTRSR is empty, it transfers the transmit data written in SSTDR to SSTRSR and starts serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, the SSU performs consecutive serial transmission.

Although SSTDR can always be read from or written to by the CPU and DTC, to achieve reliable serial transmission, write transmit data to SSTDR after confirming that the TDRE bit in SSSR is set to 1.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0		All 0	R/W	Serial transmit data

Table 17.3 Setting of DATS Bits in SSCRL and Corresponding SSTDR

	DATS[1:0] Setting			
	00	**01**	**10**	**11 (Invalid setting)**
SSTDR0	Valid	Valid	Valid	Invalid
SSTDR1	Invalid	Valid	Valid	Invalid
SSTDR2	Invalid	Invalid	Valid	Invalid
SSTDR3	Invalid	Invalid	Valid	Invalid

Caution is required because writing data for transmission to ICDRT automatically clears TDRE and TEND and reading from ICDRR automatically clears RDRF. In particular, if TDRE is again set at the same time as data for transmission are written to ICDRT, an extra byte may be transmitted when TDRE is then cleared.

Table 18.4 Interrupt Requests

Interrupt Request	Abbreviation	Interrupt Condition	I²C Bus Format	Clocked Synchronous Serial Format	DTC Activation	Priority
NACK detection	IINAKI*	{(NACKF = 1) + (AL/OVE = 1)} • (NAKIE = 1)	√	—	—	High
Arbitration lost/ overrun error			√	√	—	
Transmit end	IITEI	(TEND = 1) • (TEIE = 1)	√	√	—	
Stop condition detection	IISTPI	(STOP = 1) • (STIE = 1)	√	—	—	
Transmit data empty	IITXI	(TDRE = 1) • (TIE = 1)	√	√	√	
Receive data full	IIRXI	(RDRF = 1) • (RIE = 1)	√	√	√	Low

Note: * In the case of IINAKI, the IPR bit in the INTC, which determines the priority, is different. Depending on the setting of the IPR bit, the priority may be lower than that of IIRXI.

- Port A Control Register L3 (PACRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PA11 MD2	PA11 MD1	PA11 MD0	-	PA10 MD2	PA10 MD1	PA10 MD0	-	PA9 MD2	PA9 MD1	PA9 MD0	-	PA8 MD2	PA8 MD1	PA8 MD0
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PA11MD2	0	R/W	PA11 Mode
13	PA11MD1	0	R/W	Select the function of the PA11/$\overline{\text{CS1}}$/$\overline{\text{POE5}}$ pin.
12	PA11MD0	0*[1]	R/W	000: PA11 I/O (port) 001: $\overline{\text{CS1}}$ output (BSC)*[3] 011: $\overline{\text{POE5}}$ input (POE)*[2] Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PA10MD2	0	R/W	PA10 Mode
9	PA10MD1	0	R/W	Select the function of the PA10/$\overline{\text{CS0}}$/$\overline{\text{POE4}}$ pin.
8	PA10MD0	0*[1]	R/W	000: PA10 I/O (port) 001: $\overline{\text{CS0}}$ output (BSC)*[3] 011: $\overline{\text{POE4}}$ input (POE) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

- Port C Control Register H1 (PCCRH1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	PC19 MD0	-	-	-	PC18 MD0	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	PC19MD0	0*[1]	R/W	PC19 Mode Select the function of the PC19/A19 pin. 0: PC19 I/O (port) 1: A19 output (BSC)*[2]
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PC18MD0	0*[1]	R/W	PC18 Mode Select the function of the PC18/A18 pin. 0: PC18 I/O (port) 1: A18 output (BSC)*[2]
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. The initial value is 1 in the on-chip ROM disabled external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

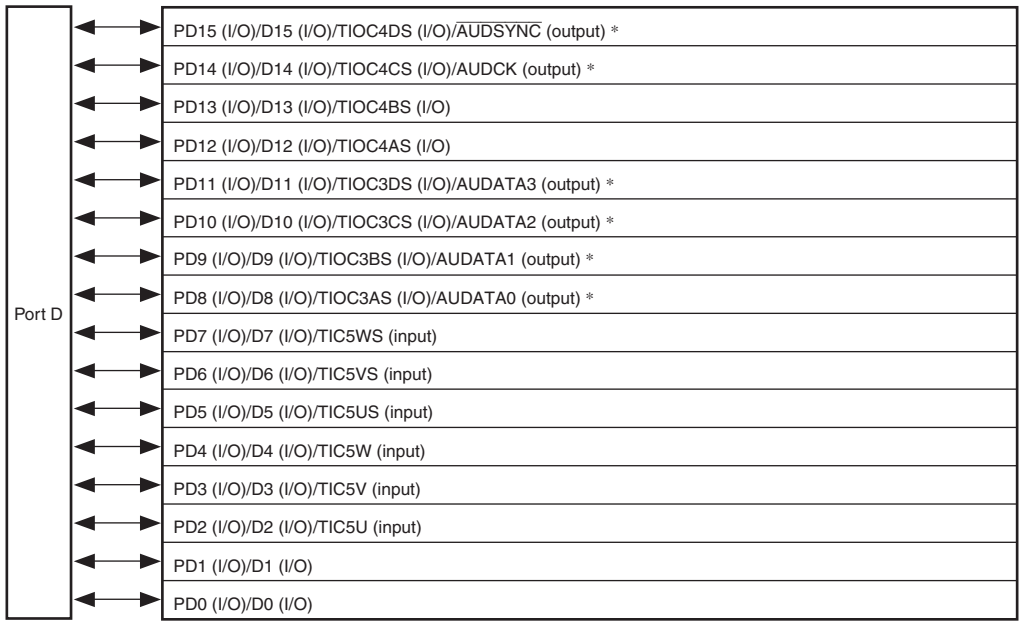
- Port C Control Register L4 (PCCRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	PC15 MD0	-	-	-	PC14 MD0	-	-	-	PC13 MD0	-	-	-	PC12 MD0
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

22.4 Port D

Port D in the SH7083 and SH7084 is an input/output port with the 16 pins shown in figure 22.9.



Note: * Only in F-ZTAT version supporting full functions of E10A.

Figure 22.9 Port D (SH7083, SH7084)

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	UA31 to UA0	Undefined	R/W	User Branch Destination Address When the user branch is not required, address 0 (H'00000000) must be set. The user branch destination must be an area other than the flash memory, an area other than the RAM area in which on-chip program has been transferred, or the external bus space. Note that the CPU must not branch to an area without the execution code and get out of control. The on-chip program download area and stack area must not be overwritten. If CPU runaway occurs or the download area or stack area is overwritten, the value of flash memory cannot be guaranteed. The download of the on-chip program, initialization, initiation of the programming/erasing program must not be executed in the processing of the user branch destination. Programming or erasing cannot be guaranteed when returning from the user branch destination. The program data which has already been prepared must not be programmed. Store general registers R8 to R15. General registers R0 to R7 are available without storing them. Moreover, the programming/erasing interface registers must not be written to or RAM emulation mode must not be entered in the processing of the user branch destination. After the processing of the user branch has ended, the programming/erasing program must be returned to by using the RTS instruction. For the execution intervals of the user branch processing, see note 2 (User branch processing intervals) in section 23.8.3, Other Notes.

(4) Erasure Execution

When flash memory is erased, the erase-block number on the user MAT must be passed to the erasing program which is downloaded. This is set to the FEBS parameter (general register R4).

One block is specified from the block number 0 to 15.

For details on the erasing procedure, see section 23.5.2, User Program Mode.

(4.1) Flash erase block select parameter (FEBS: general register R4 of CPU)

This parameter specifies the erase-block number. Several block numbers cannot be specified.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	EBS[7:0]							
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	Undefined	R/W	Unused Return 0.
7 to 0	EBS[7:0]	Undefined	R/W	• 512-kbyte flash memory Set the erase-block number in the range from 0 to 15. 0 corresponds to the EB0 block and 15 corresponds to the EB15 block. An error occurs when a number other than 0 to 15 (H'00 to H'0F) is set. • 256-kbyte flash memory Set the erase-block number in the range from 0 to 11. 0 corresponds to the EB0 block and 11 corresponds to the EB11 block. An error occurs when a number other than 0 to 11 (H'00 to H'0B) is set.

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP23	1	R/W	Module Stop Bit 23 When this bit is set to 1, the supply of the clock to the MTU2S is halted. 0: MTU2S operates 1: Clock supply to MTU2S halted
6	MSTP22	1	R/W	Module Stop Bit 22 When this bit is set to 1, the supply of the clock to the MTU2 is halted. 0: MTU2 operates 1: Clock supply to MTU2 halted
5	MSTP21	1	R/W	Module Stop Bit 21 When this bit is set to 1, the supply of the clock to the CMT is halted. 0: CMT operates 1: Clock supply to CMT halted
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
2	MSTP18	1	R/W	Module Stop Bit 18 When this bit is set to 1, the supply of the clock to the A/D_2 is halted. 0: A/D_2 operates 1: Clock supply to A/D_2 halted
1	MSTP17	1	R/W	Module Stop Bit 17 When this bit is set to 1, the supply of the clock to the A/D_1 is halted. 0: A/D_1 operates 1: Clock supply to A/D_1 halted
0	MSTP16	1	R/W	Module Stop Bit 16 When this bit is set to 1, the supply of the clock to the A/D_0 is halted. 0: A/D_0 operates 1: Clock supply to A/D_0 halted

26.3.6 Standby Control Register 6 (STBCR6)

STBCR6 is an 8-bit readable/writable register that specifies the state of the power-down modes.

Bit:	7	6	5	4	3	2	1	0
	AUD SRST	HIZ	-	-	-	-	STBY MD	-
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
7	AUDSRST	0	R/W	AUD Software Reset This bit controls the AUD reset by software. When 0 is written to AUDSRST, the AUD module shifts to the power-on reset state. 0: Shifts to the AUD reset state 1: Clears the AUD reset When setting this bit to 1, the MSTP25 bit in STBCR5 should be 0.
6	HIZ	0	R/W	Port High-Impedance In software standby mode, this bit selects whether the pin state is retained or changed to high-impedance. 0: In software standby mode, the pin state is retained 1: In software standby mode, the pin state is changed to high-impedance
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	STBYMD	0	R/W	Software Standby Mode Select This bit selects a transition to software standby mode or deep software standby mode by executing the SLEEP instruction when the STBY bit is 1 in STBCR1. 0: Transition to deep software standby mode 1: Transition to software standby mode
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
Break address register B	BARB	32	H'FFFFF320	UBC	32	Bϕ reference	16 bits
Break address mask register B	BAMRB	32	H'FFFFF324		32	W:3	
Break bus cycle register B	BBRB	16	H'FFFFF328		16	L:3	
Break data register B	BDRB	32	H'FFFFF330		32		
Break data mask register B	BDMRB	32	H'FFFFF334		32		
Break control register	BRCR	32	H'FFFFF3C0		32		
Branch source register	BRSR	32	H'FFFFF3D0		32		
Branch destination register	BRDR	32	H'FFFFF3D4		32		
Execution times break register	BETR	16	H'FFFFF3DC		16		

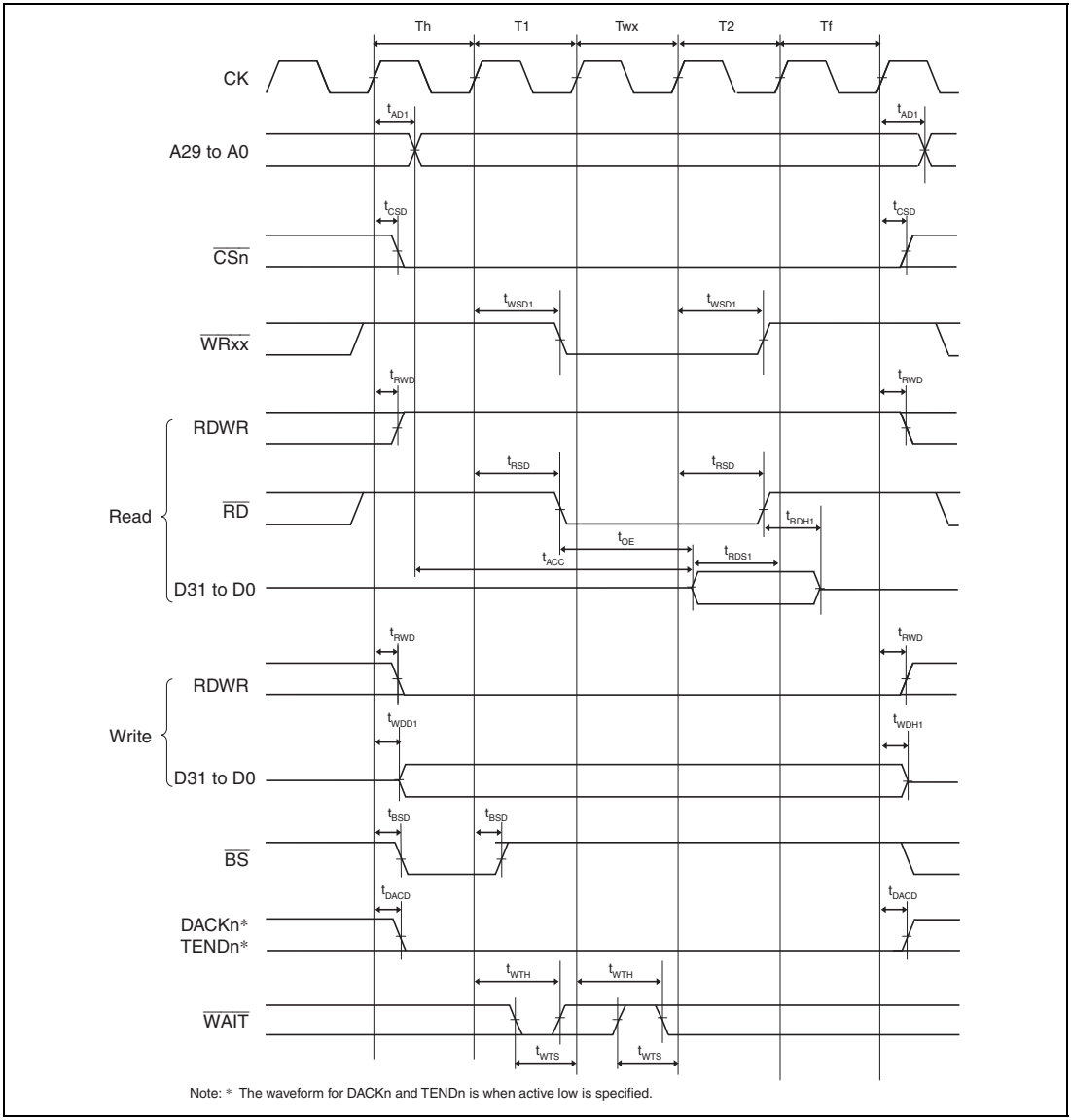


Figure 28.16 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One External Wait Cycle, BAS = 0 ($\overline{UB}$/$\overline{LB}$ in Write Cycle Controlled))