Renesas Electronics America Inc - DF70855AD80FPV Datasheet

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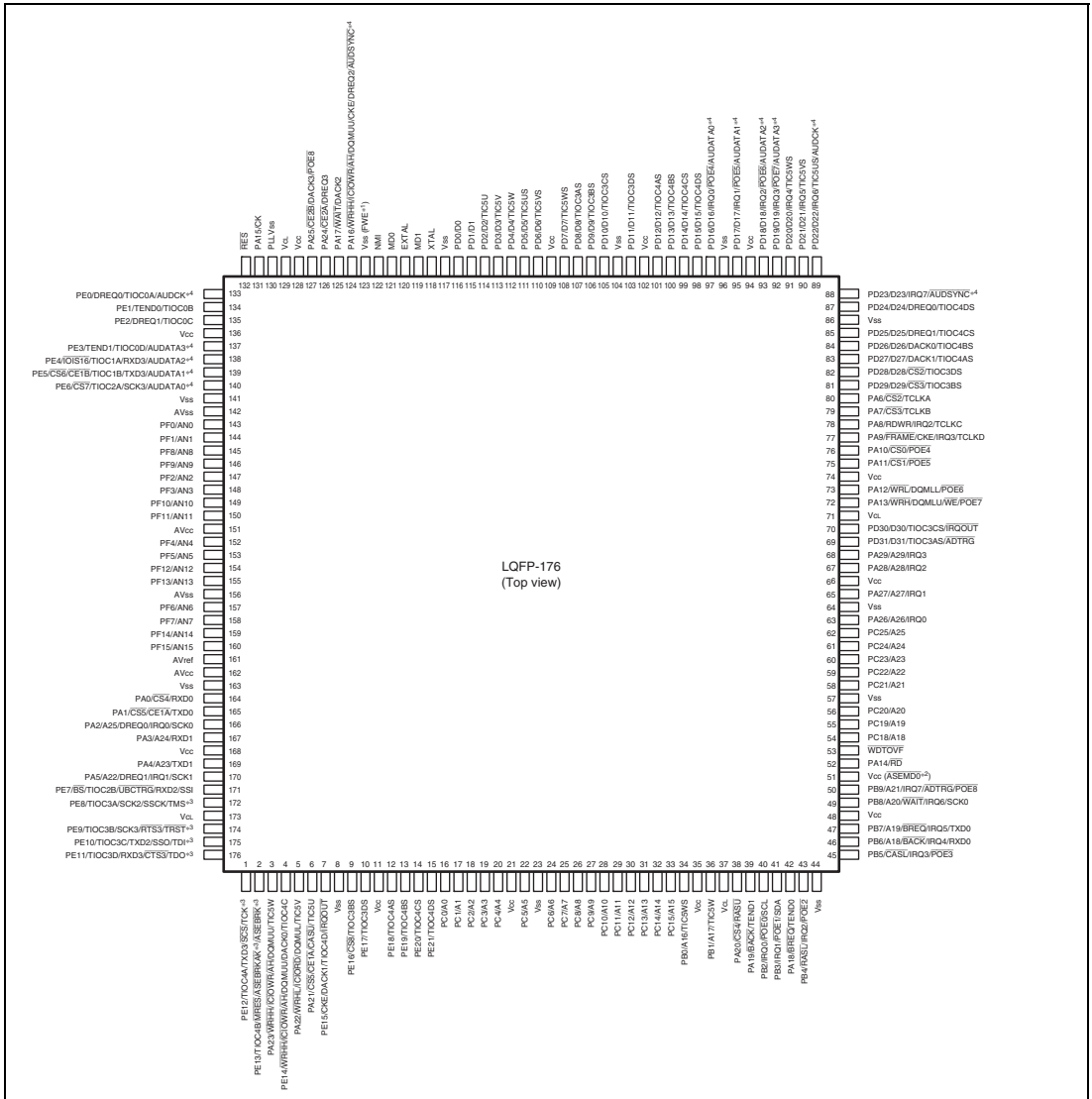
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70855ad80fpv



Notes: 1. This pin is fixed to Vss in the mask ROM and ROM-less versions and is used as the FWE input pin in the F-ZTAT version.
2. This pin is for the E10A emulator. It is fixed to Vcc in the mask ROM and ROM-less versions and is used as the $\overline{\text{ASEMD0}}$ input pin in the F-ZTAT version.
3. These pin functions are only available in the F-ZTAT version (i.e., they are not available in the mask ROM and ROM-less versions).
4. These pin functions are only available in the F-ZTAT version supporting full functions of E10A (not available in normal F-ZTAT version).

Figure 1.5 Pin Assignments of SH7086

4.3 Clock Operating Mode

Table 4.3 shows the clock operating mode of this LSI.

Table 4.3 Clock Operating Mode

Clock Operating Mode	Clock I/O		PLL Circuit	Input to Divider
	Source	Output		
1	EXTAL input or crystal resonator	CK*	ON (×8)	×8

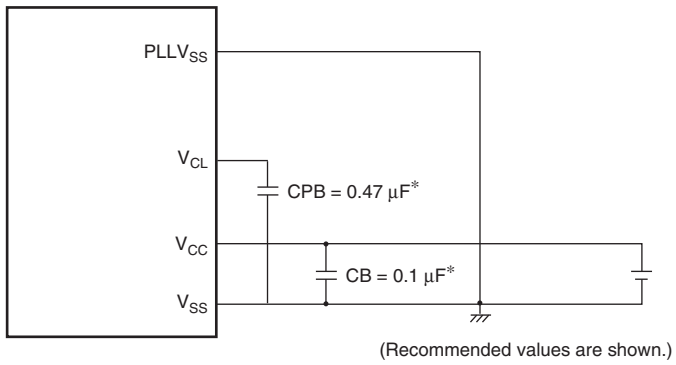
Note: * To output the clock through the clock output (CK) pin, appropriate settings should be made in the pin function controller (PFC). For details, refer to section 21, Pin Function Controller (PFC).

Mode 1: The frequency of the external clock input from the EXTAL pin is multiplied by 8 in the PLL circuit before being supplied to the on-chip modules in this LSI, which eliminates the need to generate a high-frequency clock outside the LSI. Since the input clock frequency ranging from 5 MHz to 12.5 MHz can be used, the internal clock (Iϕ) frequency ranges from 10 MHz to 80 MHz.

Maximum operating frequencies:
Iϕ = 80 MHz, Bϕ = 40 MHz, Pϕ = 40 MHz, MIϕ = 80 MHz, and MPϕ = 40 MHz

Table 4.4 shows the frequency division ratios that can be specified with FRQCR.

A circuitry shown in figure 4.6 is recommended as an external circuitry around the PLL. Separate the PLL power lines (PLLVss) and the system power lines (Vcc, Vss) at the board power supply source, and be sure to insert bypass capacitors CB and CPB close to the pins.



Note: * CB and CPB are laminated ceramic type.

Figure 4.6 Recommended External Circuitry around PLL

break occurs at a delayed branch instruction or its delay slot, the user break may not actually take place until the first instruction at the branch destination.

7.4.4 Sequential Break

1. By setting the SEQ bit in BRCR to 1, the sequential break is issued when a channel B break condition matches after a channel A break condition matches. A user break is not generated even if a channel B break condition matches before a channel A break condition matches. When channels A and B conditions match at the same time, the sequential break is not issued. To clear the channel A condition match when a channel A condition match has occurred but a channel B condition match has not yet occurred in a sequential break specification, clear the SEQ bit in BRCR to 0 and clear the condition match flag to 0 in channel A.
2. In sequential break specification, the L or I bus can be selected and the execution times break condition can be also specified. For example, when the execution times break condition is specified, the break condition is satisfied when a channel B condition matches with BETR = H'0001 after a channel A condition has matched.

7.4.5 Value of Saved Program Counter

When a user break occurs, the address of the instruction from where execution is to be resumed is saved in the stack, and the exception handling state is entered. If the L bus is specified as a break condition, the instruction at which the user break should occur can be clearly determined (except for when data is included in the break condition). If the I bus is specified as a break condition, the instruction at which the user break should occur cannot be clearly determined.

1. When instruction fetch (before instruction execution) is specified as a break condition:

   The address of the instruction that matched the break condition is saved in the stack. The instruction that matched the condition is not executed, and the user break occurs before it. However when a delay slot instruction matches the condition, the address of the delayed branch instruction is saved in the stack.
2. When instruction fetch (after instruction execution) is specified as a break condition:

   The address of the instruction following the instruction that matched the break condition is saved in the stack. The instruction that matches the condition is executed, and the user break occurs before the next instruction is executed. However when a delayed branch instruction or delay slot matches the condition, these instructions are executed, and the branch destination address is saved in the stack.

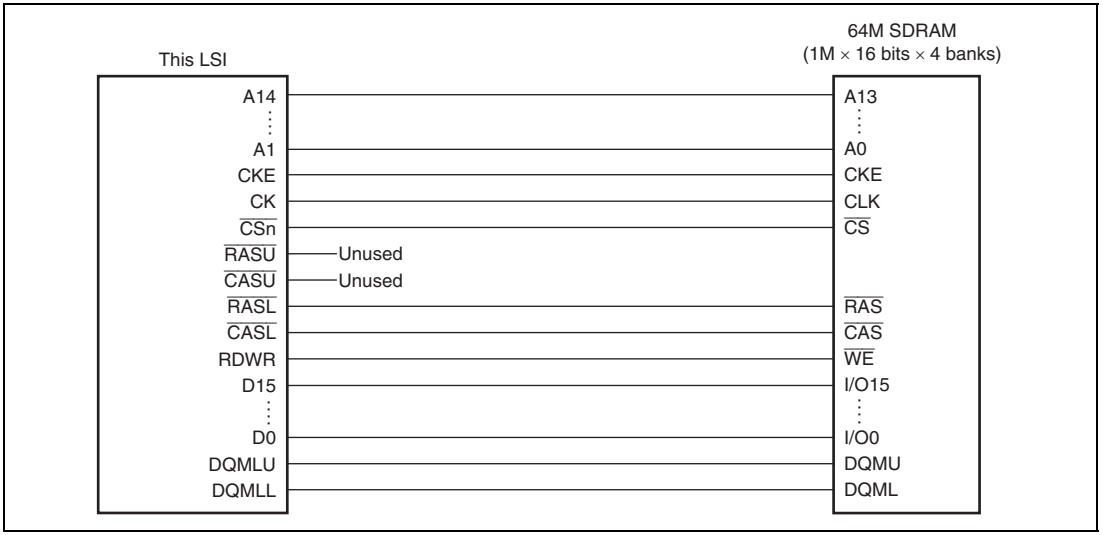


Figure 9.16 Example of 16-Bit Data Width SDRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ Are Not Used)

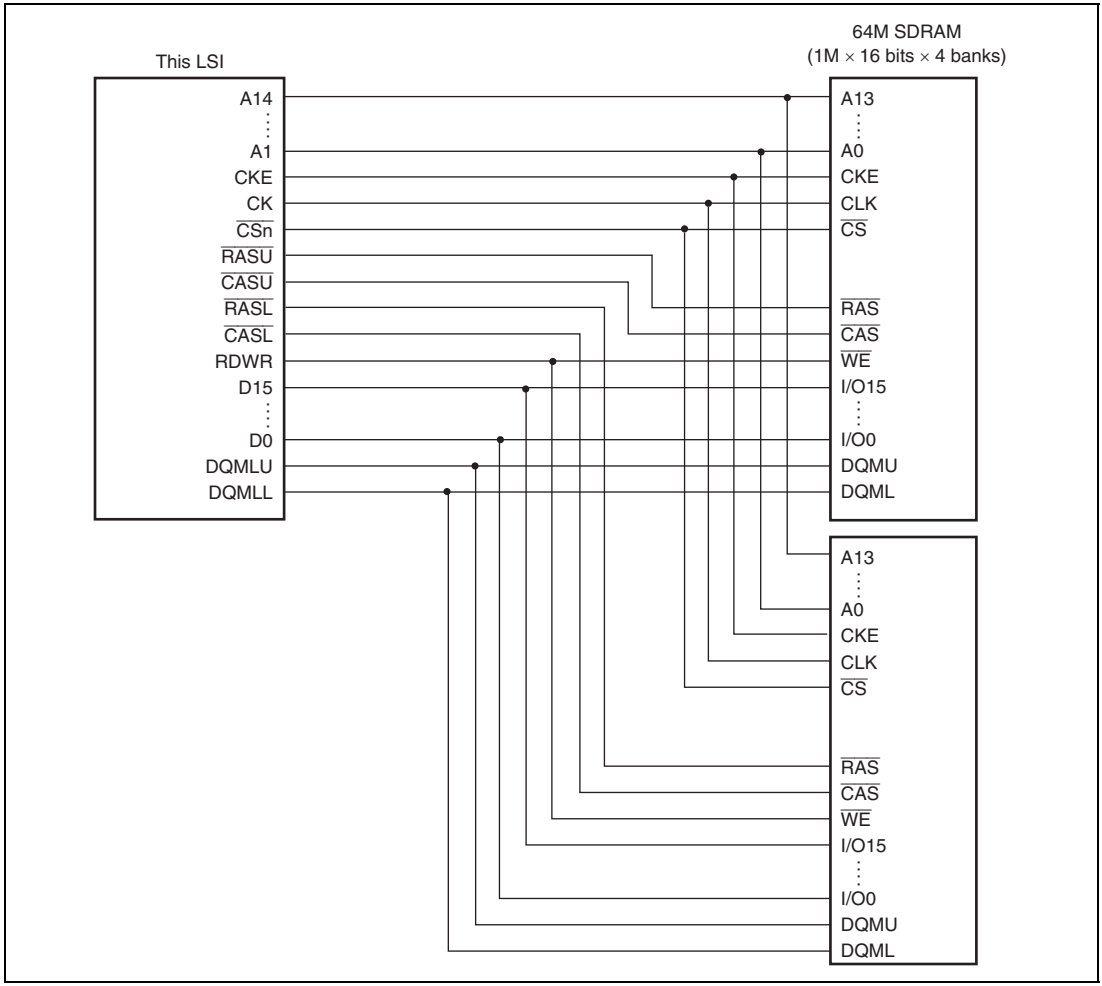
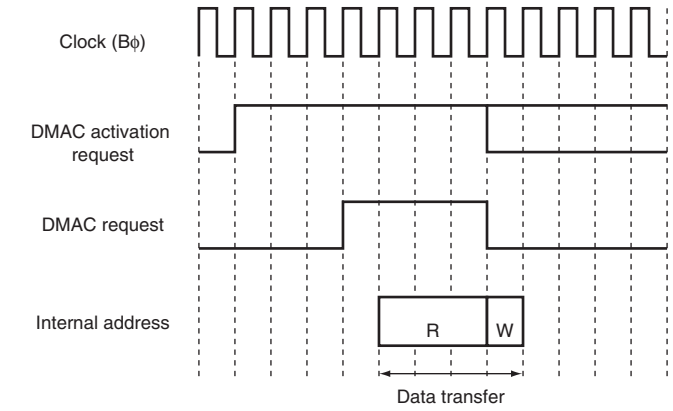


Figure 9.17 Example of 16-Bit Data Width SDRAM Connection ($\overline{\text{RASU}}$ and $\overline{\text{CASU}}$ Are Used)



Note: The DMAC request indicates the state of an internal bus request after determination of the source for DMAC activation.

Figure 10.21 Example of DMAC Operation Timing—Activation by an On-Chip Peripheral Module (in the Case of Cycle Stealing Transfer, Dual Address Mode, Low-Level Detection, Iϕ:Bϕ:Pϕ = 1:1/2:1/2, and Data Transfer from On-Chip Peripheral Module to On-Chip RAM)

(c) Initialization

In complementary PWM mode, there are nine registers that must be initialized. In addition, there is a register that specifies whether to generate dead time (it should be used only when dead time generation should be disabled).

Before setting complementary PWM mode with bits MD[3:0] in the timer mode register (TMDR), the following initial register values must be set.

TGRC_3 operates as the buffer register for TGRA_3, and should be set with 1/2 the PWM carrier cycle + dead time Td. The timer cycle buffer register (TCBR) operates as the buffer register for the timer cycle data register (TCDR), and should be set with 1/2 the PWM carrier cycle. Set dead time Td in the timer dead time data register (TDDR).

When dead time is not needed, the TDER bit in the timer dead time enable register (TDER) should be cleared to 0, TGRC_3 and TGRA_3 should be set to 1/2 the PWM carrier cycle + 1, and TDDR should be set to 1.

Set the respective initial PWM duty values in buffer registers TGRD_3, TGRC_4, and TGRD_4.

The values set in the five buffer registers excluding TDDR are transferred simultaneously to the corresponding compare registers when complementary PWM mode is set.

Set TCNT_4 to H'0000 before setting complementary PWM mode.

Table 11.56 Registers and Counters Requiring Initialization

Register/Counter	Set Value
TGRC_3	1/2 PWM cycle + dead time Td (1/2 PWM cycle + 1 when dead time generation is disabled by TDER)
TDDR	Dead time Td (1 when dead time generation is disabled by TDER)
TCBR	1/2 PWM carrier cycle
TGRD_3, TGRC_4, TGRD_4	Initial PWM duty value for each phase
TCNT_4	H'0000
TOCR1, TOCR2	PWM output level setting

Note: The TGRC_3 set value must be the sum of 1/2 the PWM cycle set in TCBR and dead time Td set in TDDR. When dead time generation is disabled by TDER, TGRC_3 must be set to 1/2 the PWM cycle + 1.

14.6.3 System Reset by $\overline{\text{WDTOVF}}$ Signal

If the $\overline{\text{WDTOVF}}$ signal is input to the $\overline{\text{RES}}$ pin of this LSI, this LSI cannot be initialized correctly.

Avoid input of the $\overline{\text{WDTOVF}}$ signal to the $\overline{\text{RES}}$ pin of this LSI through glue logic circuits. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in figure 14.5.

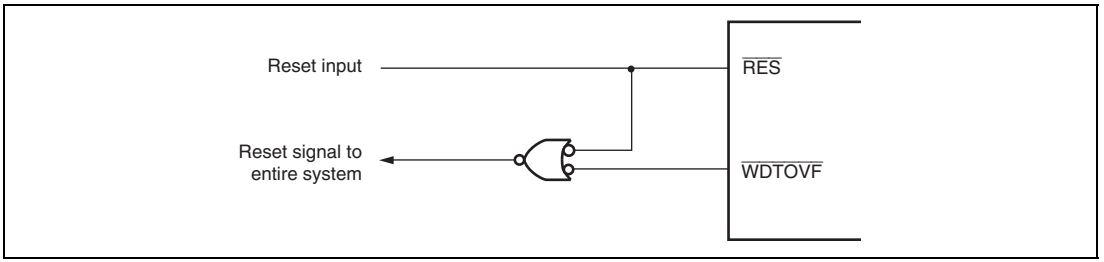


Figure 14.5 Example of System Reset Circuit Using $\overline{\text{WDTOVF}}$ Signal

14.6.4 Manual Reset in Watchdog Timer Mode

When a manual reset occurs in watchdog timer mode, the current bus cycle is continued. If a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception handling will be pended until the CPU acquires the bus mastership.

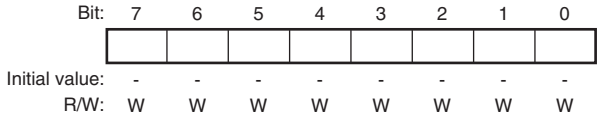
14.6.5 Internal Reset in Watchdog Timer Mode

When an internal reset is generated by an overflow of the watchdog timer counter (WTCNT) in watchdog timer mode, the watchdog timer control/status register (WTCSR) is not initialized and its value is maintained.

16.3.4 Transmit FIFO Data Register (SCFTDR)

SCFTDR is a 16-stage 8-bit FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves transmit data written in the SCFTDR into SCTSR and starts serial transmission. Continuous serial transmission is performed until there is no transmit data left in SCFTDR. SCFTDR can always be written to by the CPU.

When SCFTDR is full of transmit data (16 bytes), no more data can be written. If writing of new data is attempted, the data is ignored.

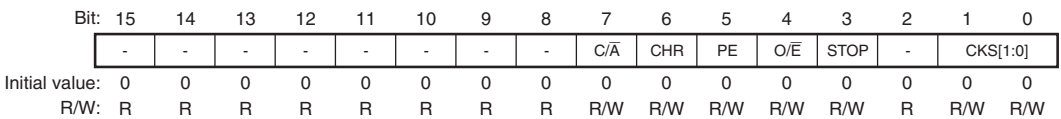


Bit	Bit Name	Initial value	R/W	Description
7 to 0		Undefined	W	FIFO for transmits serial data

16.3.5 Serial Mode Register (SCSMR)

SCSMR is a 16-bit register that specifies the SCIF serial communication format and selects the clock source for the baud rate generator.

The CPU can always read and write to SCSMR.



Bit	Bit Name	Initial value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	TEND	0	R/(W)*1	Transmit End [Clearing conditions] • When 0 is written to TEND after reading TEND = 1 • When data is written to ICDRT • DTC is activated by IITXI interrupt and the DISEL bit in MRB of DTC is 0. [Setting conditions] • When the ninth clock of SCL rises with the I²C bus format while the TDRE flag is 1 • When the final bit of transmit frame is sent with the clock synchronous serial format
5	RDRF	0	R/(W)*1	Receive Data Register Full [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When ICDRR is read • DTC is activated by IIRXI interrupt and the DISEL bit in MRB of DTC is 0. [Setting condition] • When a receive data is transferred from ICDRS to ICDRR
4	NACKF	0	R/(W)*1	No Acknowledge Detection Flag*2 [Clearing condition] • When 0 is written to NACKF after reading NACKF = 1 [Setting condition] • When no acknowledge is detected from the receive device in transmission while the ACKE bit in ICIER is 1

— Number of multipliers (1 byte): The number of selectable frequency multipliers and divisors for the device.
This is normally 2, which indicates the main operating frequency and the operating frequency of the peripheral modules.

— Multiplier 1 (1 byte): Multiplier or divisor for the main operating frequency
Multiplier: Numerical value of the frequency multiplier (e.g. H'04 for ×4)
Divisor: Two's complement negative numerical value in the case of frequency division (e.g. H'FE [-2] for ×1/2)

— Multiplier 2 (1 byte): Multiplier or divisor for the peripheral operating frequency
Multiplier: Numerical value of the frequency multiplier (e.g. H'04 for ×4)
Divisor: Two's complement negative numerical value in the case of frequency division (e.g. H'FE [-2] for ×1/2)

— SUM (1 byte): Checksum

Response	H'06

— Response H'06 (1 byte): Response to the new-bit-rate selection command
The ACK code is returned if the specified bit rate was selectable.

Error response	H'BF	ERROR

— Error response H'BF (1 byte): Error response to new bit rate selection

— ERROR (1 byte): Error code

H'11: Sum-check error

H'24: Bit rate selection error (the specified bit rate is not selectable).

H'25: Input frequency error (the specified input frequency is not within the range from the minimum to the maximum value).

H'26: Frequency multiplier error (the specified multiplier does not match an available one).

H'27: Operating frequency error (the specified operating frequency is not within the range from the minimum to the maximum value).

is not accessible, such as single-chip mode, the required procedure programs, interrupt vector table, interrupt processing routine, and user branch program should be transferred to on-chip RAM before programming/erasing of the flash memory starts.

5. The flash memory is not accessible during programming/erasing operations. Therefore, the programming/erasing program must be downloaded to on-chip RAM in advance. Areas for executing each procedure program for initiating programming/erasing and the user program at the user branch destination for programming/erasing must be located in on-chip memory other than flash memory or the external address space.
6. After programming/erasing, access to flash memory is inhibited until FKEY is cleared.

   A reset state ($\overline{RES}$ = 0) for more than at least 100 μs must be taken when the LSI mode is changed to reset on completion of a programming/erasing operation.

   Transitions to the reset state during programming/erasing are inhibited. When the reset signal is accidentally input to the LSI, a longer period in the reset state than usual (100 μs) is needed before the reset signal is released.
7. Switching of the MATs by FMATS is needed for programming/erasing of the user MAT in user boot mode. The program which switches the MATs should be executed from the on-chip RAM. For details, see section 23.8.1, Switching between User MAT and User Boot MAT. Please make sure you know which MAT is selected when switching the MATs.
8. When the program data storage area indicated by the FMPDR parameter in the programming processing is within the flash memory area, an error will occur. Therefore, temporarily transfer the program data to on-chip RAM to change the address set in FMPDR to an address other than flash memory.

Based on these conditions, tables 23.17 and 23.18 show the areas in which the program data can be stored and executed according to the operation type and mode.

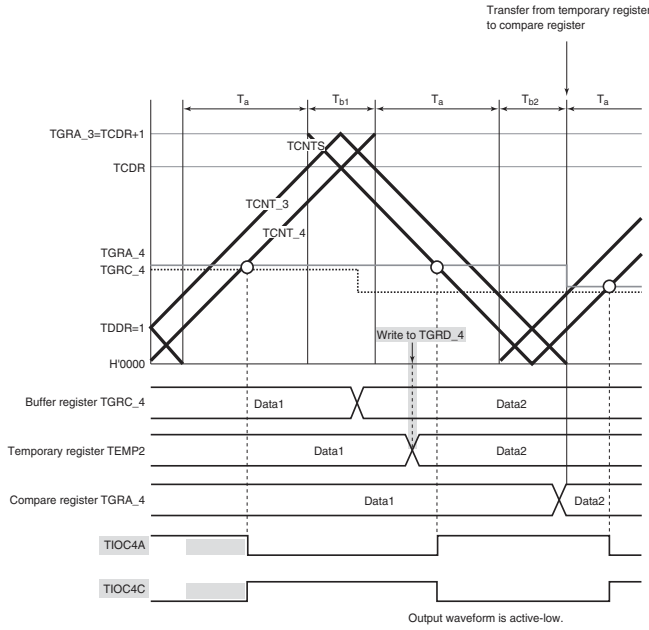
Table 23.17 Executable MAT

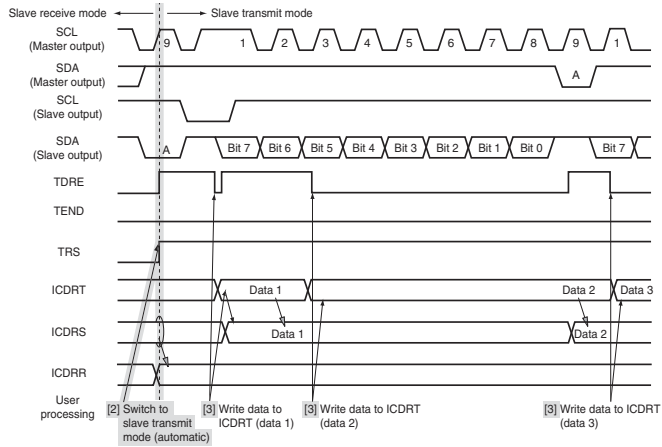
	Initiated Mode	
Operation	**User Program Mode**	**User Boot Mode***
Programming	Table 23.18 (1)	Table 23.18 (3)
Erasing	Table 23.18 (2)	Table 23.18 (4)

Note: * Programming/Erasing is possible to user MATs.

Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
A/D control/status register_0	ADCSR_0	16	H'FFFFC910	A/D	16	Pϕ reference	16 bits
A/D control register_0	ADCR_0	16	H'FFFFC912	(Channel 0)	16	B:2	
A/D data register 4	ADDR4	16	H'FFFFC980	A/D	16	W:2	
A/D data register 5	ADDR5	16	H'FFFFC982	(Channel 1)	16		
A/D data register 6	ADDR6	16	H'FFFFC984		16		
A/D data register 7	ADDR7	16	H'FFFFC986		16		
A/D control/status register_1	ADCSR_1	16	H'FFFFC990		16, 8, 32		
A/D control register_1	ADCR_1	16	H'FFFFC992		16		
A/D data register 8	ADDR8	16	H'FFFFCA00	A/D	16		
A/D data register 9	ADDR9	16	H'FFFFCA02	(Channel 2)	16		
A/D data register 10	ADDR10	16	H'FFFFCA04		16		
A/D data register 11	ADDR11	16	H'FFFFCA06		16		
A/D data register 12	ADDR12	16	H'FFFFCA08		16		
A/D data register 13	ADDR13	16	H'FFFFCA0A		16		
A/D data register 14	ADDR14	16	H'FFFFCA0C		16		
A/D data register 15	ADDR15	16	H'FFFFCA0E		16		
A/D control/status register_2	ADCSR_2	16	H'FFFFCA10		16		
A/D control register_2	ADCR_2	16	H'FFFFCA12		16		
Flash code control/status register	FCCS	8	H'FFFFCC00	FLASH	8	Pϕ reference	16 bits
Flash program code select register	FPCS	8	H'FFFFCC01		8	B:5	
Flash erase code select register	FECS	8	H'FFFFCC02		8		
Flash key code register	FKEY	8	H'FFFFCC04		8		
Flash MAT select register	FMATS	8	H'FFFFCC05		8		
Flash transfer destination address register	FTDAR	8	H'FFFFCC06		8		
DTC enable register A	DTCERA	16	H'FFFFCC80	DTC	8, 16	Pϕ reference	16 bits
DTC enable register B	DTCERB	16	H'FFFFCC82		8, 16	B:2	
DTC enable register C	DTCERC	16	H'FFFFCC84		8, 16	W:2	
DTC enable register D	DTCERD	16	H'FFFFCC86		8, 16	L:4	
DTC enable register E	DTCERE	16	H'FFFFCC88		8, 16		
DTC control register	DTCCR	8	H'FFFFCC90		8		
DTC vector base register	DTCVBR	32	H'FFFFCC94		8, 16, 32		

Item	Page	Revision (See Manual for Details)
11.4.8 Complementary PWM Mode (2) Outline of Complementary PWM Mode Operation (b) Register Operation	560, 561	Description amended In complementary PWM mode, nine registers, comprising compare registers, buffer registers, and temporary registers, are used to control the PWM duty. Figure 11.40 shows an example of complementary PWM mode operation. The registers which are constantly compared with the counters to perform PWM output are TGRB_3, TGRA_4, and TGRB_4. When one of these registers matches the counter, the level set in the corresponding timer output control register (TOCR1 or TOCR2) is output on the PWM pin. The buffer registers for these compare registers are TGRD_3, TGRC_4, and TGRD_4. Between a buffer register and compare register there is a temporary register. The temporary registers cannot be accessed by the CPU. Data in a compare register is changed by writing the new data to the corresponding buffer register. The buffer registers can be read or written at any time. When overwriting the data in the buffer registers, always write to TGRD_4 last to enable data transfer from the buffer registers to the temporary registers. At this time, transfer is also enabled from the timer cycle register buffer registers (TGRA_3 and TCBR) to the temporary registers. All five temporary registers can be used simultaneously for transfers. When transfer is enabled during the Ta interval, data written to the buffer register is transferred immediately to the temporary register. Transfer to the temporary register does not take place in the Tb1 or Tb2 interval. Data for which transfer is enabled during either of these intervals is transferred to the temporary register after the interval ends. The value transferred to a temporary register is transferred to the compare register either when the Tb1 interval ends (when TGRA_3 is matched if TCNTS is counting up) or when the Tb2 interval ends (when H'0000 is matched if TCNTS is counting down). The timing for transfer from the temporary register to the compare register can be selected with bits MD[3:0] in the timer mode register (TMDR). Figure 11.40 shows an example in which the mode is selected in which the change is made in the trough.

Item	Page	Revision (See Manual for Details)
11.4.8 Complementary PWM Mode (2) Outline of Complementary PWM Mode Operation (f) Dead Time Suppressing Figure 11.41 Example of Operation without Dead Time	565	Figure amended 
(g) PWM Cycle Setting	566	Description amended With dead time: TGRA_3 set value = TCDR set value + TDDR set value TCDR set value > Double the TDDR set value + 2 Without dead time: TGRA_3 set value = TCDR set value + 1 TCDR set value > 4 The TGRA_3 and TCDR settings are made by setting the values in buffer registers TGRC_3 and TCBR. When a write is performed to TGRD_4 and transfer is enabled, the values set in TGRC_3 and TCBR are transferred simultaneously to TGRA_3 and TCDR in accordance with the transfer timing selected by bits MD[3:0] in the timer mode register.
Figure 11.42 Example of PWM Cycle Updating	567	Figure replaced

Item	Page	Revision (See Manual for Details)
18.4.4 Slave Transmit Operation Figure 18.10 Slave Transmit Mode Operation Timing (1)	948	Figure amended 
Figure 18.11 Slave Transmit Mode Operation Timing (2)	949	Figure amended