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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

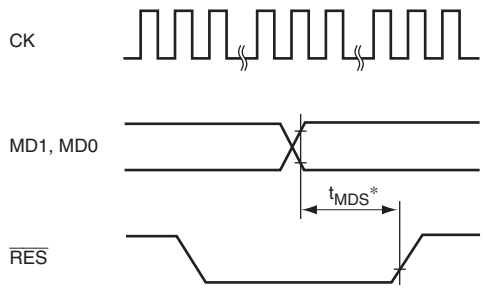
Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70855an80fpv

3.5 Initial State in This LSI

In the initial state of this LSI, some of on-chip modules are set in module standby state for saving power. When operating these modules, clear module standby state according to the procedure in section 26, Power-Down Modes.

3.6 Note on Changing Operating Mode

When changing operating mode while power is applied to this LSI, make sure to do it in the power-on reset state (that is, the low level is applied to the $\overline{\text{RES}}$ pin).



Note: * See section 28.3.2, Control Signal Timing.

Figure 3.8 Reset Input Timing when Changing Operating Mode

5.4.2 Interrupt Priority

The interrupt priority is predetermined. When multiple interrupts occur simultaneously (overlapped interruptions), the interrupt controller (INTC) determines their relative priorities and starts the exception handling according to the results.

The priority of interrupts is expressed as priority levels 0 to 16, with priority 0 the lowest and priority 16 the highest. The NMI interrupt has priority 16 and cannot be masked, so it is always accepted. The priority level of the user break interrupt is 15. IRQ interrupt and on-chip peripheral module interrupt priority levels can be set freely using the interrupt priority registers A to F and H to M (IPRA to IPRF and IPRH to IPRM) of the INTC as shown in table 5.8. The priority levels that can be set are 0 to 15. Level 16 cannot be set. For details on IPRA to IPRF, see section 6.3.4, Interrupt Priority Registers A to F and H to M (IPRA to IPRF and IPRH to IPRM).

Table 5.8 Interrupt Priority

Type	Priority Level	Comment
NMI	16	Fixed priority level. Cannot be masked.
User break	15	Fixed priority level. Can be masked.
IRQ	0 to 15	Set with interrupt priority registers A to F and H to M (IPRA to IPRF and IPRH to IPRM).
On-chip peripheral module		

5.4.3 Interrupt Exception Handling

When an interrupt occurs, the interrupt controller (INTC) ascertains its priority level. NMI is always accepted, but other interrupts are only accepted if they have a priority level higher than the priority level set in the interrupt mask bits (I3 to I0) of the status register (SR).

When an interrupt is accepted, exception handling begins. In interrupt exception handling, the CPU saves SR and the program counter (PC) to the stack. The priority level of the accepted interrupt is written to bits I3 to I0 in SR. Although the priority level of the NMI is 16, the value set in bits I3 to I0 is H'F (level 15). Next, the start address of the exception handling routine is fetched from the exception handling vector table for the accepted interrupt, and program execution branches to that address and the program starts. For details on the interrupt exception handling, see section 6.6, Interrupt Operation.

Bus cycle: L bus/instruction fetch (after instruction execution)/read (operand size is not included in the condition)

<Channel B>

Address: H'00008010, Address mask: H'00000006

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read (operand size is not included in the condition)

A user break occurs after an instruction with addresses H'00008000 to H'00008FFE is executed or before an instruction with addresses H'00008010 to H'00008016 are executed.

Break Condition Specified for L Bus Data Access Cycle:

(Example 2-1)

- Register specifications

  BARA = H'00123456, BAMRA = H'00000000, BBRA = H'0064, BDRA = H'12345678, BDMRA = H'FFFFFFFF, BARB = H'000ABCDE, BAMRB = H'000000FF, BBRB = H'006A, BDRB = H'0000A512, BDMRB = H'00000000, BRCR = H'00000080

  Specified conditions: Channel A/channel B independent mode

  <Channel A>

  Address: H'00123456, Address mask: H'00000000

  Data: H'12345678, Data mask: H'FFFFFFFF

  Bus cycle: L bus/data access/read (operand size is not included in the condition)

  <Channel B>

  Address: H'000ABCDE, Address mask: H'000000FF

  Data: H'0000A512, Data mask: H'00000000

  Bus cycle: L bus/data access/write/word

  On channel A, a user break occurs with longword read from address H'00123454, word read from address H'00123456, or byte read from address H'00123456. On channel B, a user break occurs when word H'A512 is written in addresses H'000ABC00 to H'000ABCFE.

Bit	Bit Name	Initial Value	R/W	Description
21	SZSEL	0	R/W	MPX-I/O Interface Bus Width Specification Specifies the address bit to select the bus width when the BSZ1 and BSZ0 bits in CS5BCR are set to 11. This setting is valid only when MPX-I/O is selected for area 5. 0: Address A14 selects the bus width 1: Address A21 selects the bus width The following shows bus width selection through the SZSEL bit and A14 or A21.

SZSEL	A14	A21	Bus Width
0	0	No effect	8 bits
0	1	No effect	16 bits
1	No effect	0	8 bits
1	No effect	1	16 bits

Bit	Bit Name	Initial Value	R/W	Description
20	MPXW	0	R/W	MPX-I/O Interface Address Wait This setting is valid only when MPX-I/O is selected for area 5. This bit specifies insertion of a wait cycle into the address cycle in MPX-I/O interface. 0: No wait 1: Inserts one wait cycle
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Table 11.28 TIORU_5, TIORV_5, and TIORW_5 (Channel 5)

					Description	
Bit 4 IOC4	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	TGRU_5, TGRV_5, and TGRW_5 Function	TIC5U, TIC5V, and TIC5W Pin Function
0	0	0	0	0	Compare match register	Compare match
				1		Setting prohibited
			1	x		Setting prohibited
		1	x	x		Setting prohibited
	1	x	x	x		Setting prohibited
1	0	0	0	0	Input capture register	Setting prohibited
				1		Input capture at rising edge
			1	0		Input capture at falling edge
				1		Input capture at both edges
		1	x	x		Setting prohibited
	1	0	0	0		Setting prohibited
				1		Measurement of low pulse width of external input signal Capture at trough of complementary PWM mode
			1	0		Measurement of low pulse width of external input signal Capture at crest of complementary PWM mode
				1		Measurement of low pulse width of external input signal Capture at crest and trough of complementary PWM mode
		1	0	0		Setting prohibited
				1		Measurement of high pulse width of external input signal Capture at trough of complementary PWM mode
			1	0		Measurement of high pulse width of external input signal Capture at crest of complementary PWM mode
				1		Measurement of high pulse width of external input signal Capture at crest and trough of complementary PWM mode

[Legend]

x: Don't care

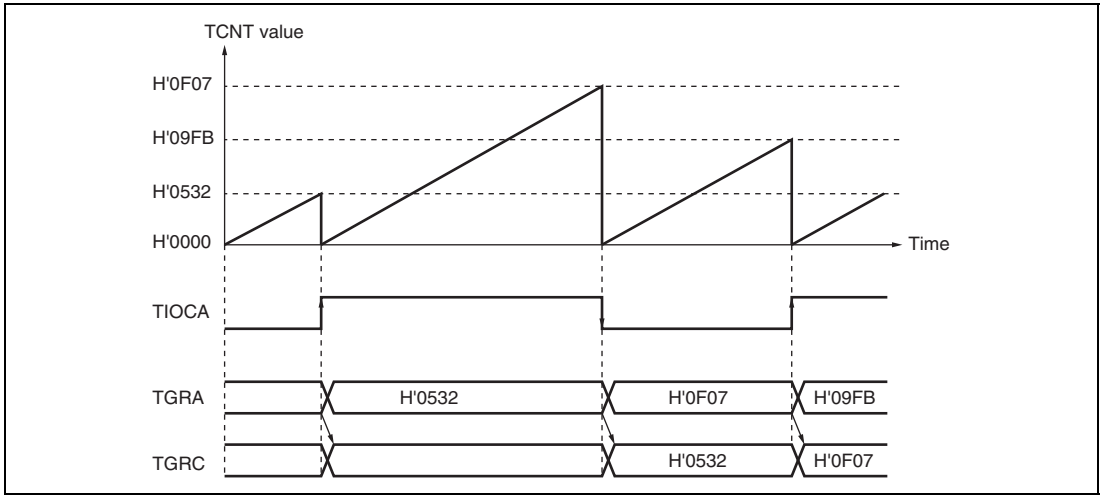


Figure 11.18 Example of Buffer Operation (2)

Selecting Timing for Transfer from Buffer Registers to Timer General Registers in Buffer Operation: The timing for transfer from buffer registers to timer general registers can be selected in PWM mode 1 or 2 for channel 0 or in PWM mode 1 for channels 3 and 4 by setting the buffer operation transfer mode registers (TBTM_0, TBTM_3, and TBTM_4). Either compare match (initial setting) or TCNT clearing can be selected for the transfer timing. TCNT clearing as transfer timing is one of the following cases.

- When TCNT overflows (H'FFFF to H'0000)
- When H'0000 is written to TCNT during counting
- When TCNT is cleared to H'0000 under the condition specified in the CCLR[2:0] bits in TCR

Note: TBTM must be modified only while TCNT stops.

Figure 11.19 shows an operation example in which PWM mode 1 is designated for channel 0 and buffer operation is designated for TGRA_0 and TGRC_0. The settings used in this example are TCNT_0 clearing by compare match B, 1 output at compare match A, and 0 output at compare match B. The TTSA bit in TBTM_0 is set to 1.

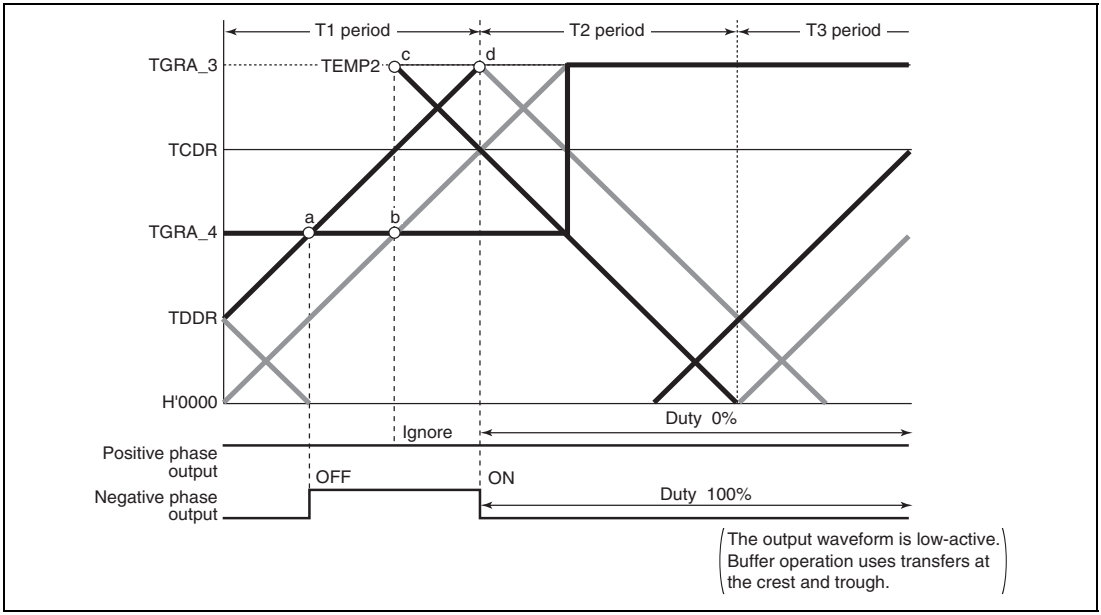


Figure 11.51 Example of Complementary PWM Mode 0% and 100% Waveform Output (3)

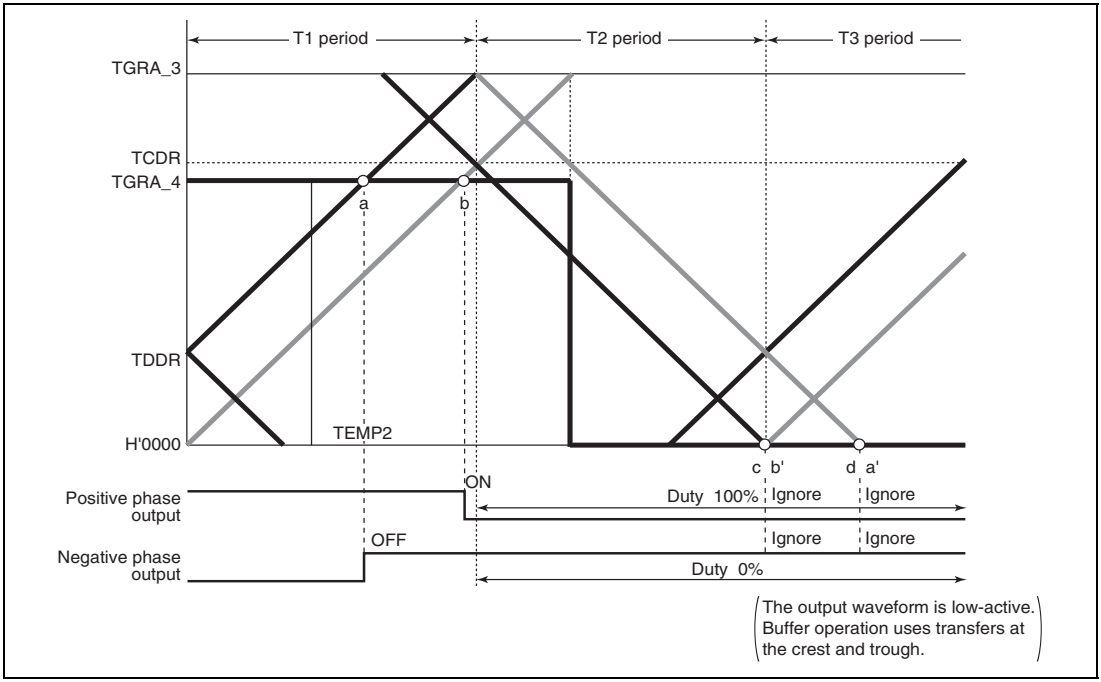


Figure 11.52 Example of Complementary PWM Mode 0% and 100% Waveform Output (4)

(b) Basic Operation Example of A/D Converter Start Request Delaying Function

Figure 11.80 shows a basic example of A/D converter request signal (TRG4AN) operation when the trough of TCNT_4 is specified for the buffer transfer timing and an A/D converter start request signal is output during TCNT_4 down-counting.

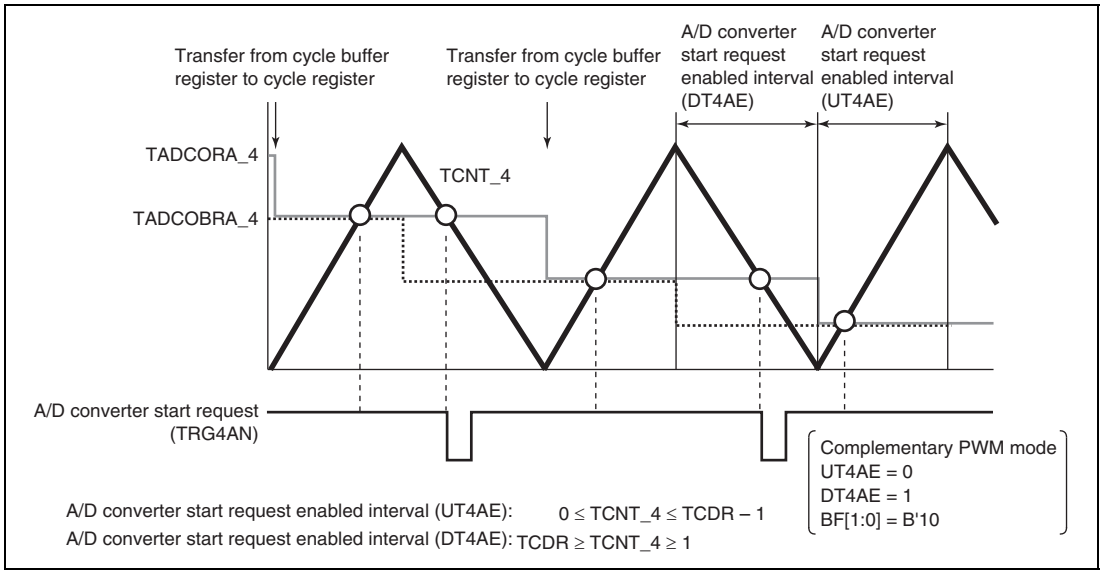


Figure 11.80 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation

(c) A/D Converter Start Request Enabled Interval

When TCNT_4 and TADCORA_4/TADCORB_4 match during the interval enabled by the UT4AE, DT4AE, UT4BE, or DT4BE bit in TADCR, a start request is issued for the corresponding A/D converter (TRG4AN or TRG4BN).

If the UT4AE or UT4BE bit is set to 1 in complementary PWM mode, A/D converter start requests are enabled during the TCNT_4 up-counting interval (0 ≤ TCNT_4 ≤ TCDR−1). A/D converter start requests are enabled during the TCNT_4 down-counting interval (TCDR ≥ TCNT_4 ≥ 1) if the DT4AE or DT4BE bit is set to 1 (figure 11.80).

Clear the DT4AE and DT4BE bits to 0 when not in complementary PWM mode. Setting the UT4AE or UT4BE bit to 1 causes an A/D converter start request to be generated at a compare match between TCNT_4 and TADCORA_4/TADCORB_4, regardless of whether TCNT_4 is counting up or down.

11.7.17 Contention between Overflow/Underflow and Counter Clearing

If overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence.

Figure 11.135 shows the operation timing when a TGR compare match is specified as the clearing source, and when H'FFFF is set in TGR.

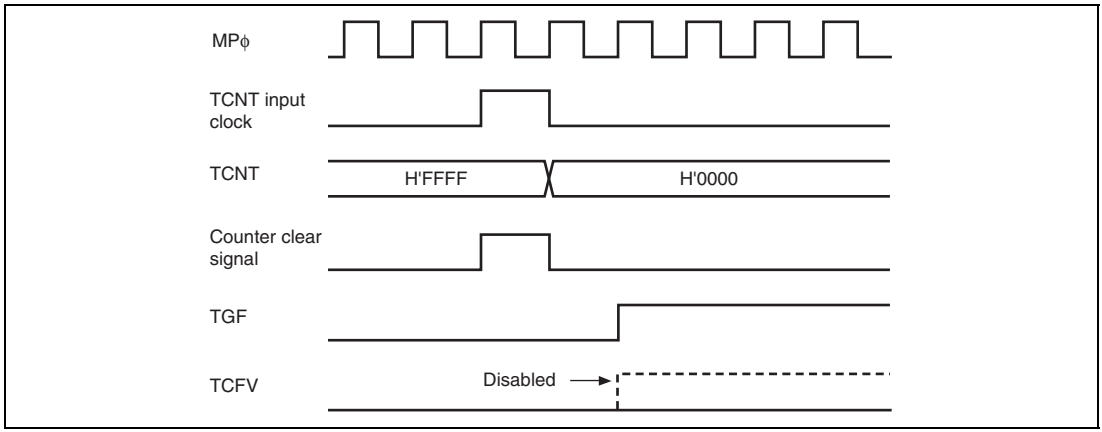


Figure 11.135 Contention between Overflow and Counter Clearing

11.7.18 Contention between TCNT Write and Overflow/Underflow

If there is an up-count or down-count in the T2 state of a TCNT write cycle, and overflow/underflow occurs, the TCNT write takes precedence and the TCFV/TCFU flag in TSR is not set.

Figure 11.136 shows the operation timing when there is contention between TCNT write and overflow.

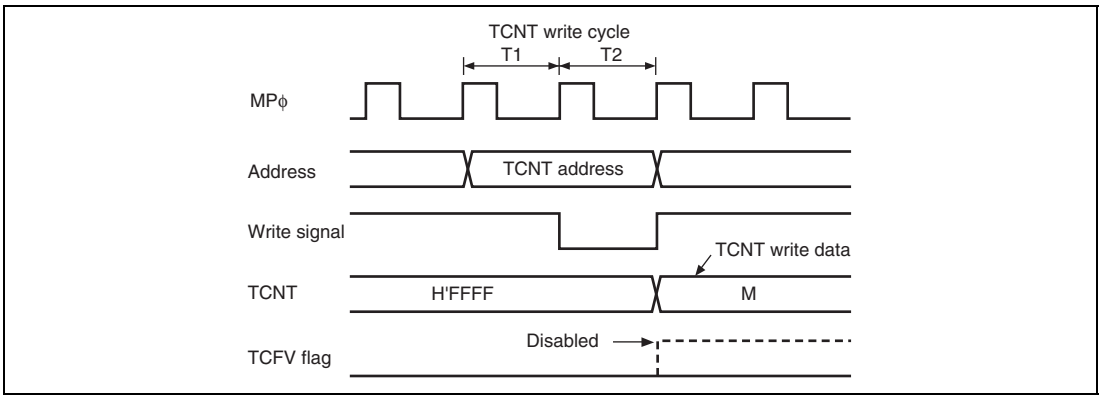


Figure 11.136 Contention between TCNT Write and Overflow

11.7.19 Cautions on Transition from Normal Operation or PWM Mode 1 to Reset-Synchronized PWM Mode

When making a transition from channel 3 or 4 normal operation or PWM mode 1 to reset-synchronized PWM mode, if the counter is halted with the output pins (TIOC3B, TIOC3D, TIOC4A, TIOC4C, TIOC4B, TIOC4D) in the high-level state, followed by the transition to reset-synchronized PWM mode and operation in that mode, the initial pin output will not be correct.

When making a transition from normal operation to reset-synchronized PWM mode, write H'11 to registers TIORH_3, TIORL_3, TIORH_4, and TIORL_4 to initialize the output pins to low level output, then set an initial register value of H'00 before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronized PWM mode, first switch to normal operation, then initialize the output pins to low level output and set an initial register value of H'00 before making the transition to reset-synchronized PWM mode.

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Reset-Synchronized PWM Mode: Figure 11.146 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in reset-synchronized PWM mode after re-setting.

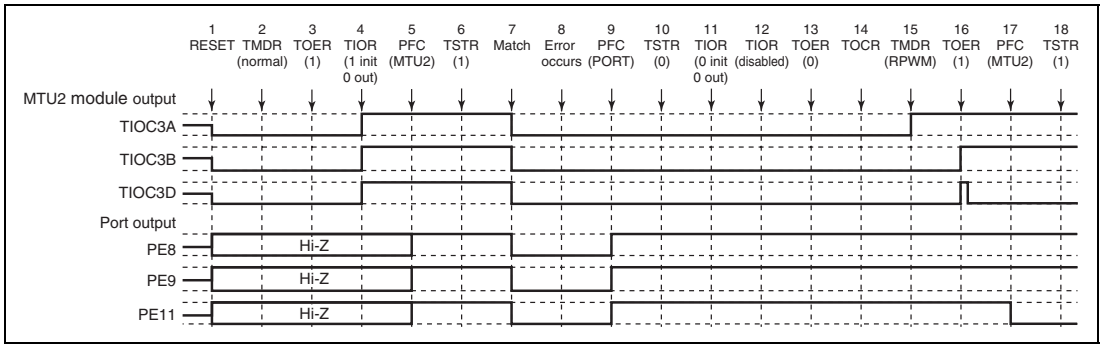


Figure 11.146 Error Occurrence in Normal Mode, Recovery in Reset-Synchronized PWM Mode

1 to 13 are the same as in figure 11.141.

14. Select the reset-synchronized PWM output level and cyclic output enabling/disabling with TOCR.
15. Set reset-synchronized PWM.
16. Enable channel 3 and 4 output with TOER.
17. Set MTU2 output with the PFC.
18. Operation is restarted by TSTR.

Bit	Bit Name	Initial value	R/W	Description
2	SPB1DT	Undefined	W	Clock Port Data in Serial Port Controls the SCK pin in combination with the SPB1IO bit, the C/$\overline{A}$ bit in SCSMR, and the CKE[1:0] bits in SCSCR. Note that the SCK pin function needs to have been selected with the pin function controller (PFC). Also, this bit is write-only. When read its value is undefined.

C/$\overline{A}$	CKE1	CKE0	SPB 1IO	SPB 1DT	SCK pin state
0	0	0	0	×	SCK pin functions as input pin.
0	0	0	1	0	Low-level output
0	0	0	1	1	High-level output
0	0	1	×	×	SCK pin functions as clock output.
0	1	0	×	×	SCK pin functions as clock input.
0	1	1	×	×	SCK pin functions as clock input.
1	0	0	×	×	SCK pin functions as sync clock output.
1	0	1	×	×	SCK pin functions as sync clock output.
1	1	0	×	×	SCK pin functions as sync clock input.
1	1	1	×	×	SCK pin functions as sync clock input.

Note: ×: Don't care

1	SPB0IO	0	R/W	Serial Port Break Output Together with the SPB0DT bit and the TE bit in SCSCR, controls the TXD pin.

Tables 15.4 shows examples of SCBRR settings in asynchronous mode, and tables 15.5 shows examples of SCBRR settings in clock synchronous mode.

Table 15.4 Bit Rates and SCBRR Settings in Asynchronous Mode (1)

	Pϕ (MHz)																	
Bit Rate (bits/s)	10			12			14			16			18			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	177	-0.25	2	212	0.03	2	248	-0.17	3	70	0.03	3	79	-0.12	3	88	-0.25
150	2	129	0.16	2	155	0.16	2	181	0.16	2	207	0.16	2	233	0.16	3	64	0.16
300	2	64	0.16	2	77	0.16	2	90	0.16	2	103	0.16	2	116	0.16	2	129	0.16
600	1	129	0.16	1	155	0.16	1	181	0.16	1	207	0.16	1	233	0.16	2	64	0.16
1200	1	64	0.16	1	77	0.16	1	90	0.16	1	103	0.16	1	116	0.16	1	129	0.16
2400	0	129	0.16	0	155	0.16	0	181	0.16	0	207	0.16	0	233	0.16	1	64	0.16
4800	0	64	0.16	0	77	0.16	0	90	0.16	0	103	0.16	0	116	0.16	0	129	0.16
9600	0	32	-1.36	0	38	0.16	0	45	-0.93	0	51	0.16	0	58	-0.69	0	64	0.16
14400	0	21	-1.36	0	25	0.16	0	29	1.27	0	34	-0.79	0	38	0.16	0	42	0.94
19200	0	15	1.73	0	19	-2.34	0	22	-0.93	0	25	0.16	0	28	1.02	0	32	-1.36
28800	0	10	-1.36	0	12	0.16	0	14	1.27	0	16	2.12	0	19	-2.34	0	21	-1.36
31250	0	9	0.00	0	11	0.00	0	13	0.00	0	15	0.00	0	17	0.00	0	19	0.00
38400	0	7	1.73	0	9	-2.34	0	10	3.57	0	12	0.16	0	14	-2.34	0	15	1.73
115200	0	2	-9.58	0	2	8.51	0	3	-5.06	0	3	8.51	0	4	-2.34	0	4	8.51
500000	0	0*	-37.5	0	0*	-25.0	0	0*	-12.5	0	0*	0.00	0	0*	12.5	0	0*	25.0

16.4.2 Operation in Asynchronous Mode

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCIF are independent, so full duplex communication is possible. The transmitter and receiver are 16-byte FIFO buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving. Figure 16.2 shows the general format of asynchronous serial communication.

In asynchronous serial communication, the communication line is normally held in the mark (high) state. The SCIF monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCIF synchronizes at the falling edge of the start bit. The SCIF samples each data bit on the eighth pulse of a clock with a frequency 16 times the bit rate. Receive data is latched at the center of each bit.

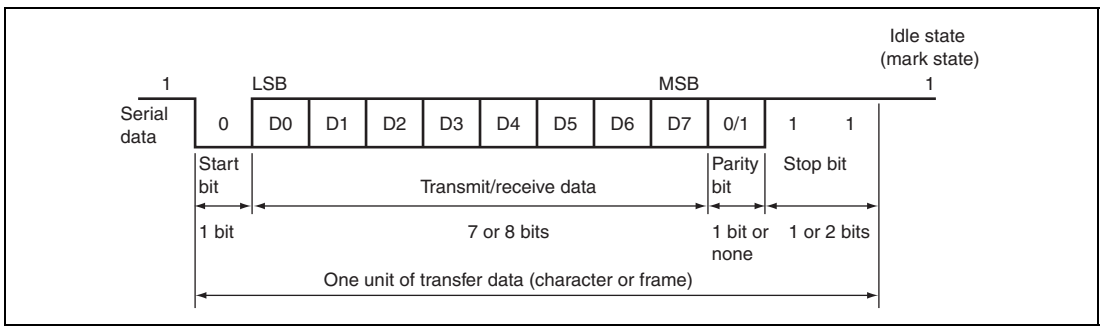


Figure 16.2 Example of Data Format in Asynchronous Communication (8-Bit Data with Parity and Two Stop Bits)

Figure 18.1 shows a block diagram of the I²C bus interface.

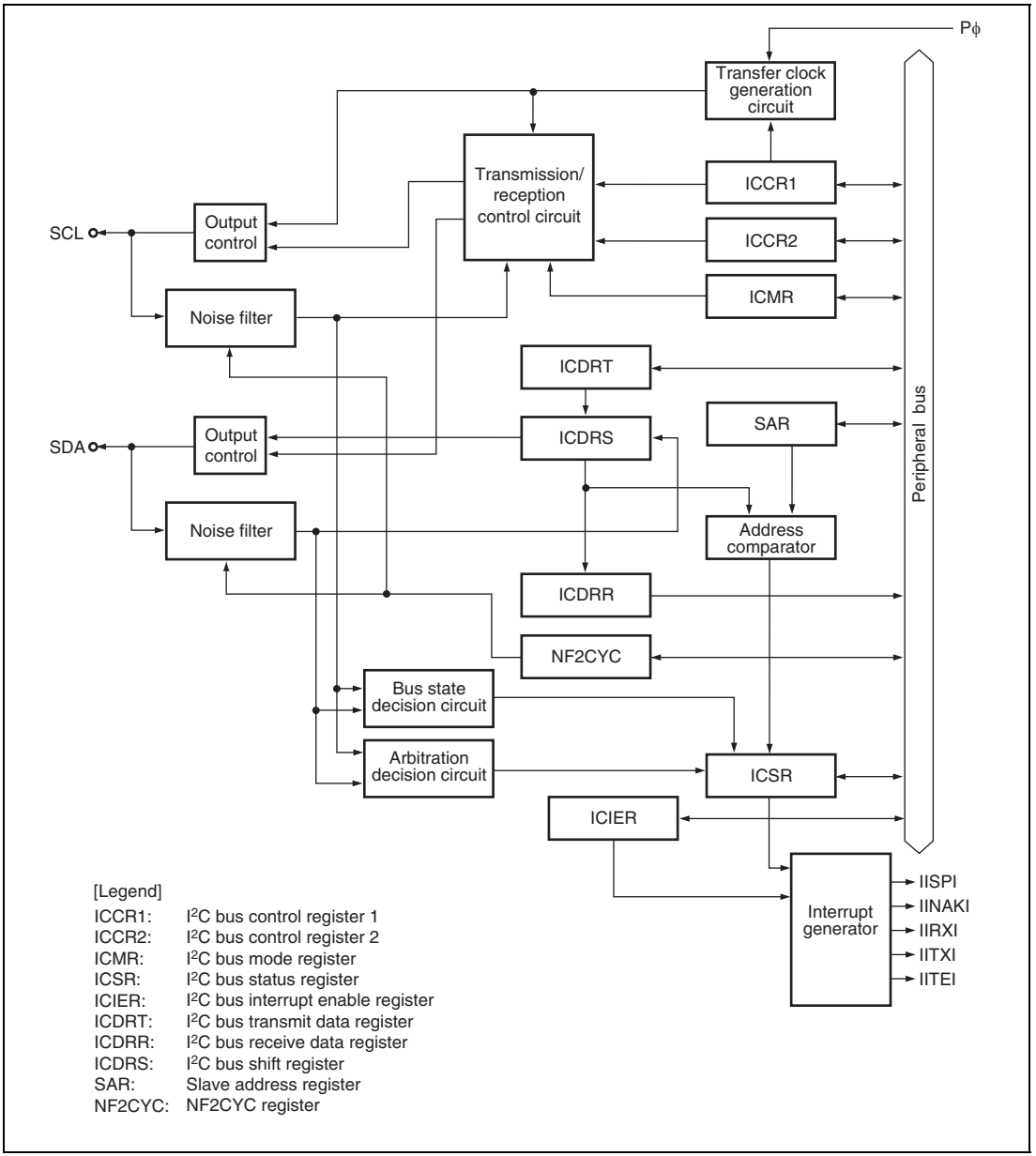


Figure 18.1 Block Diagram of I²C Bus Interface 2

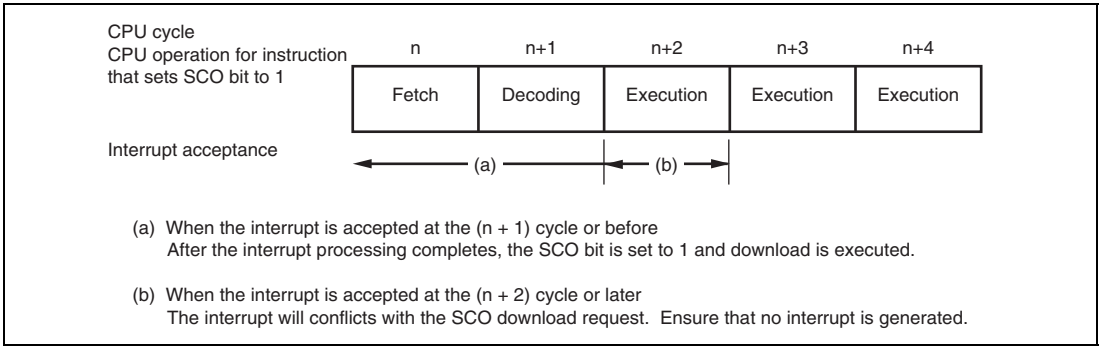
	Pin Name			
	On-Chip ROM Disabled (MCU Mode 0)		On-Chip ROM Disabled (MCU Mode 1)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
113	PE3/(AUDATA3*2)	PE3/TEND1/TIOC0D	PE3/(AUDATA3*2)	PE3/TEND1/TIOC0D
114	PE4/(AUDATA2*2)	PE4/$\overline{\text{IOIS16}}$/TIOC1A/RXD3	PE4/(AUDATA2*2)	PE4/$\overline{\text{IOIS16}}$/TIOC1A/RXD3
115	PE5/(AUDATA1*2)	PE5/$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$/TIOC1B/TXD3	PE5/(AUDATA1*2)	PE5/$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$/TIOC1B/TXD3
116	PE6/(AUDATA0*2)	PE6/$\overline{\text{CS7}}$/TIOC2A/SCK3	PE6/(AUDATA0*2)	PE6/$\overline{\text{CS7}}$/TIOC2A/SCK3
137	PE7	PE7/$\overline{\text{BS}}$/TIOC2B/$\overline{\text{UBCTRG}}$ /RXD2/SSI	PE7	PE7/$\overline{\text{BS}}$/TIOC2B/$\overline{\text{UBCTRG}}$ /RXD2/SSI
138	PE8/(TMS*1)	PE8/TIOC3A/SCK2/SSCK	PE8/(TMS*1)	PE8/TIOC3A/SCK2/SSCK
139	PE9/($\overline{\text{TRST}}$*1)	PE9/TIOC3B/SCK3/$\overline{\text{RTS3}}$	PE9/($\overline{\text{TRST}}$*1)	PE9/TIOC3B/SCK3/$\overline{\text{RTS3}}$
140	PE10/(TDI*1)	PE10/TIOC3C/TXD2/SSO	PE10/(TDI*1)	PE10/TIOC3C/TXD2/SSO
142	PE11/(TDO*1)	PE11/TIOC3D/RXD3/$\overline{\text{CTS3}}$	PE11/(TDO*1)	PE11/TIOC3D/RXD3/$\overline{\text{CTS3}}$
143	PE12/(TCK*1)	PE12/TIOC4A/TXD3/$\overline{\text{SCS}}$	PE12/(TCK*1)	PE12/TIOC4A/TXD3/$\overline{\text{SCS}}$
144	PE13/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE13/TIOC4B/$\overline{\text{MRES}}$	PE13/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE13/TIOC4B/$\overline{\text{MRES}}$
2	PE14	PE14/$\overline{\text{WRHH}}$/$\overline{\text{ICIOWR}}$/$\overline{\text{AH}}$ /DQMUU/DACK0/TIOC4C	PE14	PE14/$\overline{\text{WRHH}}$/$\overline{\text{ICIOWR}}$/$\overline{\text{AH}}$ /DQMUU/DACK0/TIOC4C
5	PE15	PE15/CKE/DACK1/TIOC4D /$\overline{\text{IRQOUT}}$	PE15	PE15/CKE/DACK1/TIOC4D /$\overline{\text{IRQOUT}}$
118	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0
119	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1
120	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2
121	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3
122	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4
123	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5
125	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6
126	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7

Notes: 1. Fixed to TMS, $\overline{\text{TRST}}$, TDI, TDO, TCK, and $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ when using the E10A (in $\overline{\text{ASEMD0}}$ = low).

2. Only in F-ZTAT version supporting full functions of E10A. Fixed as AUD pins when using the AUD function of the E10A.

Bit	Bit Name	Initial Value	R/W	Description
10	PD22MD2	0	R/W	PD22 Mode
9	PD22MD1	0	R/W	Select the function of the
8	PD22MD0	0*1	R/W	PD22/D22/IRQ6/TIC5US/AUDCK pin. Fixed to AUDCK output when using the AUD function of the E10A. 000: PD22 I/O (port) 001: D22 I/O (BSC)*2 010: IRQ6 input (INTC) 100: TIC5US I/O (MTU2S) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PD21MD2	0	R/W	PD21 Mode
5	PD21MD1	0	R/W	Select the function of the PD21/D21/IRQ5/TIC5VS
4	PD21MD0	0*1	R/W	pin. 000: PD21 I/O (port) 001: D21 I/O (BSC)*2 010: IRQ5 input (INTC) 100: TIC5VS I/O (MTU2S) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PD20MD2	0	R/W	PD20 Mode
1	PD20MD1	0	R/W	Select the function of the PD20/D20/IRQ4/TIC5WS
0	PD20MD0	0*1	R/W	pin. 000: PD20 I/O (port) 001: D20 I/O (BSC)*2 010: IRQ4 input (INTC) 100: TIC5WS I/O (MTU2S) Other than above: Setting prohibited

Notes: 1. The initial value is 1 in the on-chip ROM disabled 32-bit external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.



(a) When the interrupt is accepted at the (n + 1) cycle or before
After the interrupt processing completes, the SCO bit is set to 1 and download is executed.

(b) When the interrupt is accepted at the (n + 2) cycle or later
The interrupt will conflicts with the SCO download request. Ensure that no interrupt is generated.

Figure 23.21 Timing of Contention between SCO Download Request and Interrupt Request

2. Generation of interrupt requests during downloading
Securing of bus-mastership by other than the interrupt and CPU bus masters (DMA transfer, DTC transfer, SDRAM refresh) is prohibited during SCO download execution.

(2) Interrupts during programming/erasing

Securing of bus-mastership by other than the interrupt and CPU bus masters (DMA transfer, DTC transfer, SDRAM refresh) is prohibited during programming or erase execution by a downloaded on-chip program.

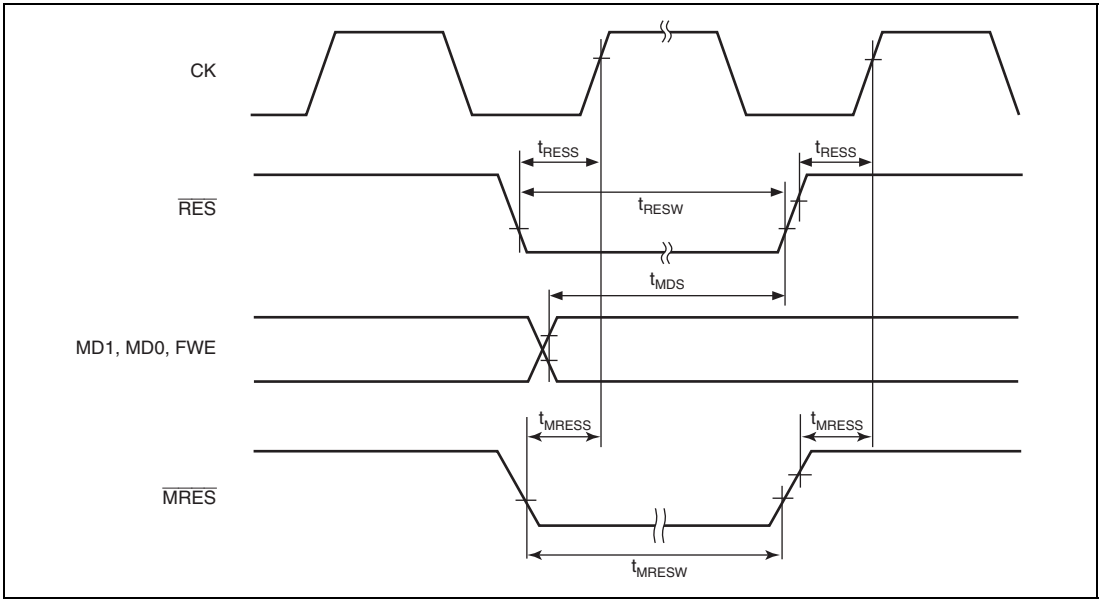


Figure 28.6 Reset Input Timing

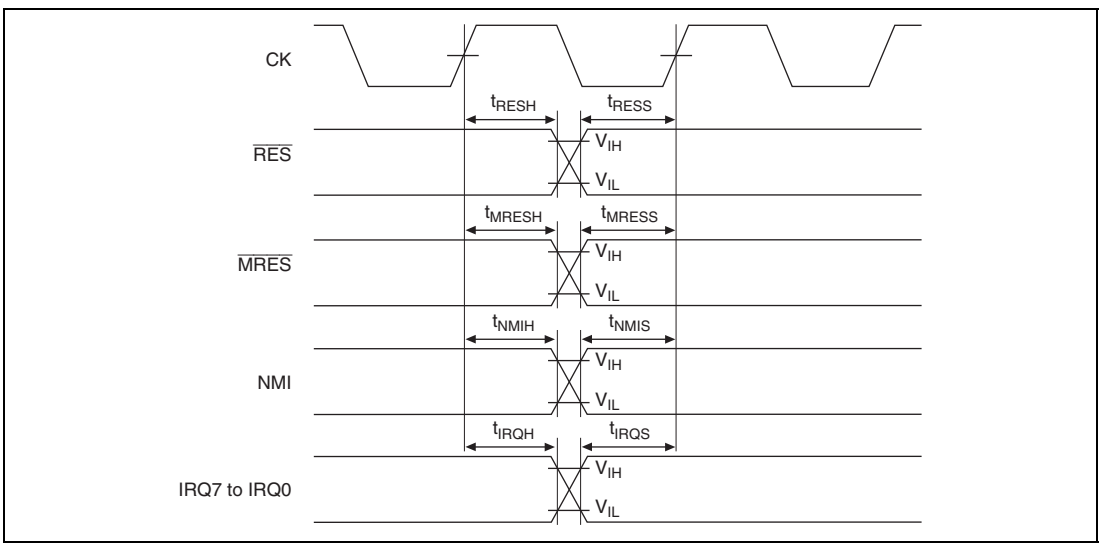


Figure 28.7 Interrupt Signal Input Timing

28.3.7 I/O Port Timing

Table 28.12 I/O Port Timing

Conditions: V_{CC} = 3.0 V to 3.6 V or 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +85°C (consumer applications), T_a = –40°C to +85°C (industrial applications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
Port output data delay time	t_{PWD}	—	50	ns	Figure 28.49
Port input hold time	t_{PRH}	20	—	ns	
Port input setup time	t_{PRS}	20	—	ns	

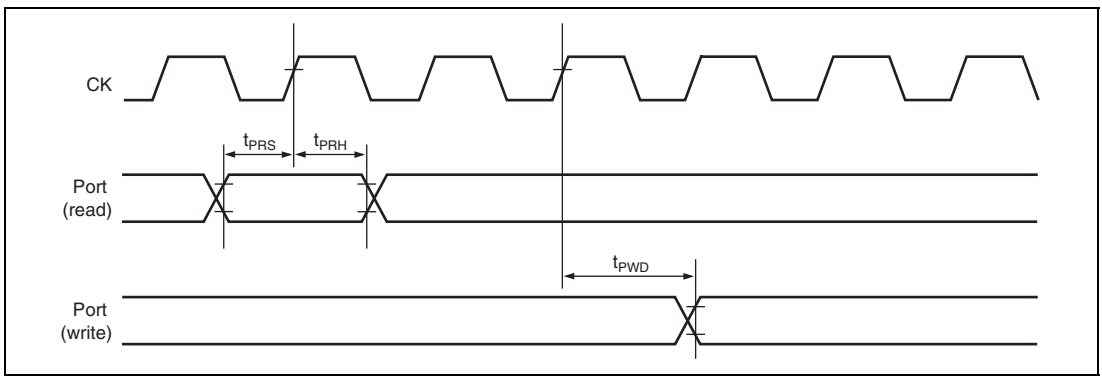


Figure 28.49 I/O Port Input/Output Timing