Renesas Electronics America Inc - DF70865AN80FPV Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df70865an80fpv

Address	Area	Memory Type	Capacity	Bus Width
H'18000000 to H'1BFFFFFF	CS6 space	Normal space SRAM with byte selection PCMCIA Burst MPX-I/O	64 Mbytes	8, 16, or 32 bits*[2]
H'1C000000 to H'1FFFFFFF	CS7 space	Normal space SRAM with byte selection	64 Mbytes	8, 16, or 32 bits*[2]
H'20000000 to H'FFF7FFFF	Reserved			
H'FFF80000 to H'FFF9FFFF	SDRAM mode setting space			
H'FFFA0000 to H'FFFF3FFF	Reserved			
H'FFFF4000 to H'FFFFBFFF	On-chip RAM		32 Kbytes	32 bits
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral modules		16 Kbytes	8 or 16 bits

Notes: Do not access the reserved area. If the reserved area is accessed, the correct operation cannot be guaranteed.

1. The bus width is selected by the mode pins.
2. The bus width is selected by the register setting.

Table 9.14 Address Map: SH7086 in On-Chip ROM-Enabled Mode

Address	Area	Memory Type	Capacity	Bus Width
H'00000000 to H'0007FFFF	On-chip ROM		512 Kbytes	32 bits
H'00080000 to H'01FFFFFF	Reserved			
H'02000000 to H'03FFFFFF	CS0 space	Normal space SRAM with byte selection Burst ROM (asynchronous) Burst ROM (synchronous)	32 Mbytes	8, 16, or 32 bits*
H'04000000 to H'07FFFFFF	CS1 space	Normal space SRAM with byte selection	64 Mbytes	8, 16, or 32 bits*

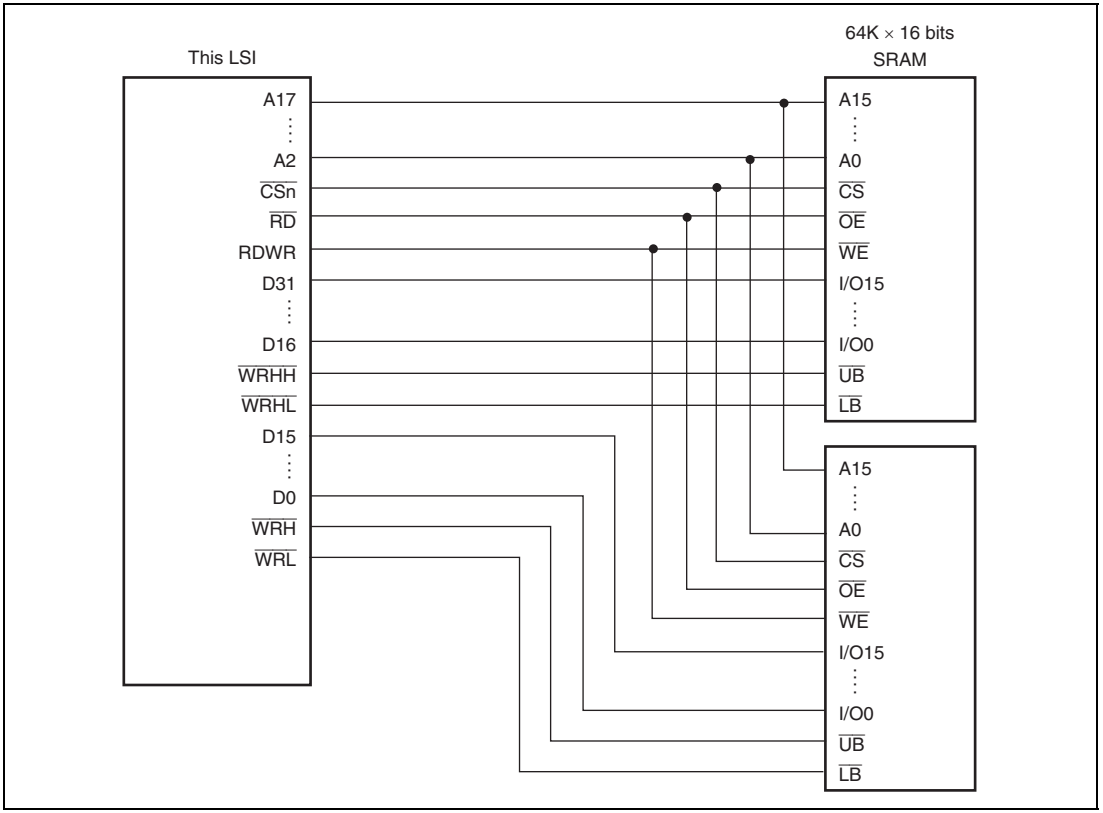


Figure 9.36 Example of Connection with 32-Bit Data Width Byte-Selection SRAM

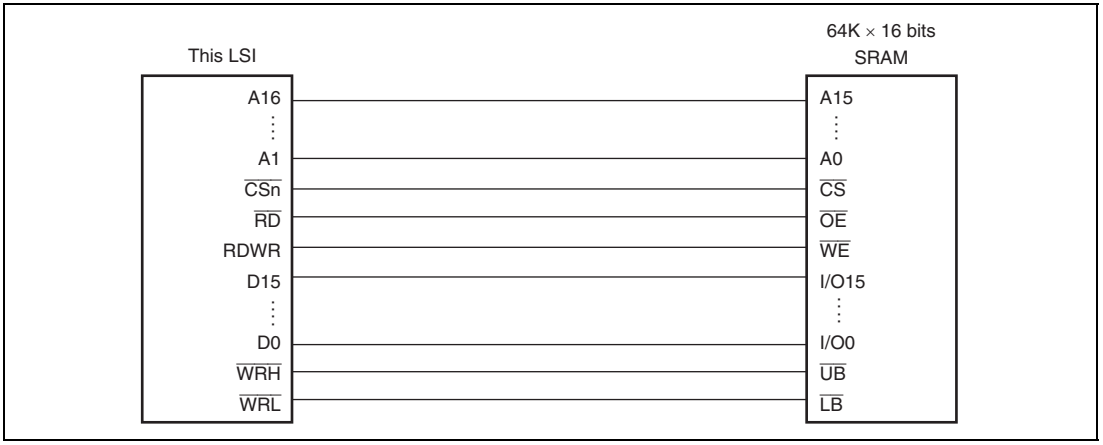


Figure 9.37 Example of Connection with 16-Bit Data Width Byte-Selection SRAM

11.3.31 Timer Dead Time Enable Register (TDER)

TDER is an 8-bit readable/writable register that controls dead time generation in complementary PWM mode. The MTU2 has one TDER in channel 3. TDER must be modified only while TCNT stops.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	TDER
Initial value:	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/(W)

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TDER	1	R/(W)	Dead Time Enable Specifies whether to generate dead time. 0: Does not generate dead time 1: Generates dead time* [Clearing condition] • When 0 is written to TDER after reading TDER = 1

Note: * TDDR must be set to 1 or a larger value.

Example of Synchronous Operation: Figure 11.13 shows an example of synchronous operation.

In this example, synchronous operation and PWM mode 1 have been designated for channels 0 to 2, TGRB_0 compare match has been set as the channel 0 counter clearing source, and synchronous clearing has been set for the channel 1 and 2 counter clearing source.

Three-phase PWM waveforms are output from pins TIOC0A, TIOC1A, and TIOC2A. At this time, synchronous presetting, and synchronous clearing by TGRB_0 compare match, are performed for channel 0 to 2 TCNT counters, and the data set in TGRB_0 is used as the PWM cycle.

For details of PWM modes, see section 11.4.5, PWM Modes.

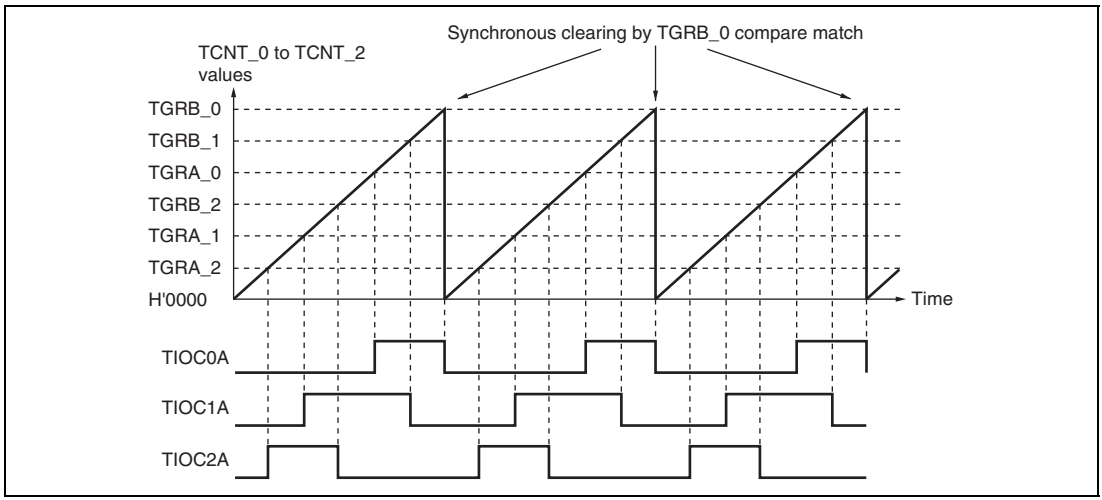


Figure 11.13 Example of Synchronous Operation

Table 11.57 MTU2 Interrupts

Channel	Name	Interrupt Source	Interrupt Flag	DMAC Activation	DTC Activation	Priority
0	TGIA_0	TGRA_0 input capture/compare match	TGFA_0	Possible	Possible	High
	TGIB_0	TGRB_0 input capture/compare match	TGFB_0	Not possible	Possible	
	TGIC_0	TGRC_0 input capture/compare match	TGFC_0	Not possible	Possible	
	TGID_0	TGRD_0 input capture/compare match	TGFD_0	Not possible	Possible	
	TCIV_0	TCNT_0 overflow	TCFV_0	Not possible	Not possible	
	TGIE_0	TGRE_0 compare match	TGFE_0	Not possible	Not possible	
	TGIF_0	TGRF_0 compare match	TGFF_0	Not possible	Not possible	
1	TGIA_1	TGRA_1 input capture/compare match	TGFA_1	Possible	Possible	
	TGIB_1	TGRB_1 input capture/compare match	TGFB_1	Not possible	Possible	
	TCIV_1	TCNT_1 overflow	TCFV_1	Not possible	Not possible	
	TCIU_1	TCNT_1 underflow	TCFU_1	Not possible	Not possible	
2	TGIA_2	TGRA_2 input capture/compare match	TGFA_2	Possible	Possible	
	TGIB_2	TGRB_2 input capture/compare match	TGFB_2	Not possible	Possible	
	TCIV_2	TCNT_2 overflow	TCFV_2	Not possible	Not possible	
	TCIU_2	TCNT_2 underflow	TCFU_2	Not possible	Not possible	
3	TGIA_3	TGRA_3 input capture/compare match	TGFA_3	Possible	Possible	
	TGIB_3	TGRB_3 input capture/compare match	TGFB_3	Not possible	Possible	
	TGIC_3	TGRC_3 input capture/compare match	TGFC_3	Not possible	Possible	
	TGID_3	TGRD_3 input capture/compare match	TGFD_3	Not possible	Possible	
	TCIV_3	TCNT_3 overflow	TCFV_3	Not possible	Not possible	
4	TGIA_4	TGRA_4 input capture/compare match	TGFA_4	Possible	Possible	
	TGIB_4	TGRB_4 input capture/compare match	TGFB_4	Not possible	Possible	
	TGIC_4	TGRC_4 input capture/compare match	TGFC_4	Not possible	Possible	
	TGID_4	TGRD_4 input capture/compare match	TGFD_4	Not possible	Possible	
	TCIV_4	TCNT_4 overflow/underflow	TCFV_4	Not possible	Possible	
5	TGIU_5	TGRU_5 input capture/compare match	TGFU_5	Not possible	Possible	
	TGIV_5	TGRV_5 input capture/compare match	TGFV_5	Not possible	Possible	
	TGIW_5	TGRW_5 input capture/compare match	TGFW_5	Not possible	Possible	Low

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

13.5 Interrupts

The POE issues a request to generate an interrupt when the specified condition is satisfied during input level detection or output level comparison. Table 13.5 shows the interrupt sources and their conditions.

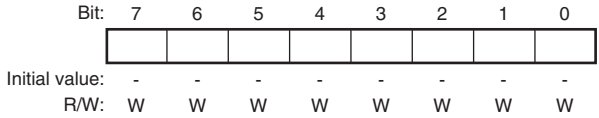
Table 13.5 Interrupt Sources and Conditions

Name	Interrupt Source	Interrupt Flag	Condition
OEI1	Output enable interrupt 1	POE3F, POE2F, POE1F, POE0F, and OSF1	PIE1 • (POE3F + POE2F + POE1F + POE0F) + OIE1 • OSF1
OEI3	Output enable interrupt 3	POE8F	PIE3 • POE8F
OEI2	Output enable interrupt 2	POE4F, POE5F, POE6F, POE7F, and OSF2	PIE2 • (POE4F + POE5F + POE6F + POE7F) + OIE2 • OSF2

16.3.4 Transmit FIFO Data Register (SCFTDR)

SCFTDR is a 16-stage 8-bit FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves transmit data written in the SCFTDR into SCTSR and starts serial transmission. Continuous serial transmission is performed until there is no transmit data left in SCFTDR. SCFTDR can always be written to by the CPU.

When SCFTDR is full of transmit data (16 bytes), no more data can be written. If writing of new data is attempted, the data is ignored.

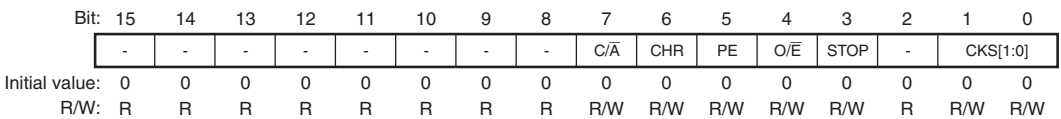


Bit	Bit Name	Initial value	R/W	Description
7 to 0		Undefined	W	FIFO for transmits serial data

16.3.5 Serial Mode Register (SCSMR)

SCSMR is a 16-bit register that specifies the SCIF serial communication format and selects the clock source for the baud rate generator.

The CPU can always read and write to SCSMR.



Bit	Bit Name	Initial value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

18.3.2 I²C Bus Control Register 2 (ICCR2)

ICCR2 is an 8-bit readable/writable register that issues start/stop conditions, manipulates the SDA pin, monitors the SCL pin, and controls reset in the control part of the I²C bus interface 2.

ICCR2 is initialized to H'7D by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	BBSY	SCP	SDAO	SDAOP	SCLO	-	IICRST	-
Initial value:	0	1	1	1	1	1	0	1
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
7	BBSY	0	R/W	Bus Busy This bit enables to confirm whether the I²C bus is occupied or released and to issue start/stop conditions in master mode. With the clock synchronous serial format, this bit is always read as 0. With the I²C bus format, this bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. This bit is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. To issue a start condition, simultaneously write 1 to BBSY and 0 to SCP. Follow this procedure also when transmitting a repeated start condition. To issue a stop condition, simultaneously write 0 to BBSY and 0 to SCP.
6	SCP	1	R/W	Start/Stop Issue Condition Disable The SCP bit controls the issue of start/stop conditions in master mode. To issue a start condition, simultaneously write 1 to BBSY and 0 to SCP. A repeated start condition is issued in the same way. To issue a stop condition, simultaneously write 0 to BBSY and 0 to SCP. This bit is always read as 1. Even if 1 is written to this bit, the data will not be stored.

18.4.7 Noise Filter

The logic levels at the SCL and SDA pins are routed through noise filters before being latched internally. Figure 18.18 shows a block diagram of the noise filter circuit.

The noise filter consists of three cascaded latches and a match detector. The SCL (or SDA) input signal is sampled on the peripheral clock. When NF2CYC is set to 0, this signal is not passed forward to the next circuit unless the outputs of both latches agree. When NF2CYC is set to 1, this signal is not passed forward to the next circuit unless the outputs of three latches agree. If they do not agree, the previous value is held.

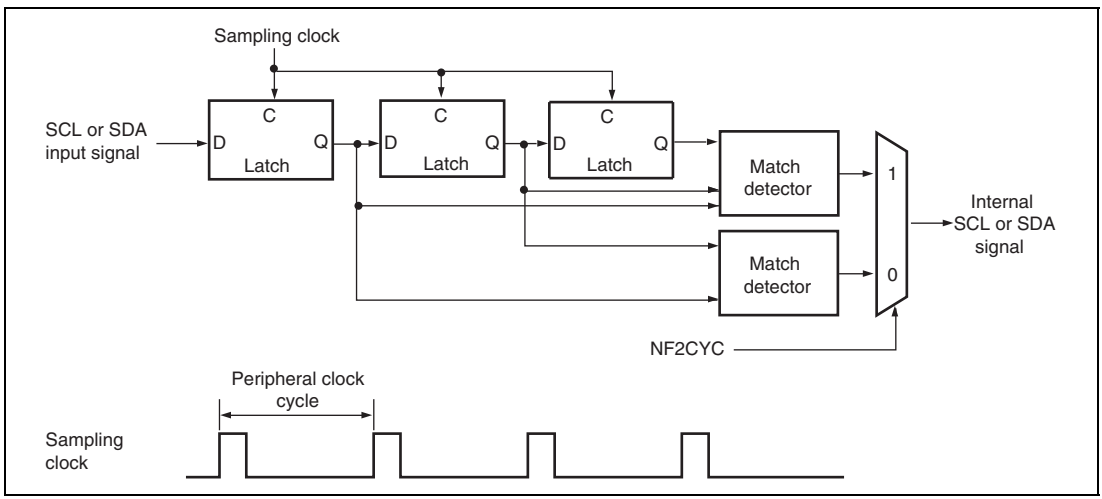


Figure 18.18 Block Diagram of Noise Filter

Table 21.13 SH7085 Multiplexed Pins (Port E)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)
E	PE0 I/O (port)	DREQ0 input (DMAC)	TIOC0A I/O (MTU2)	AUDCK output (AUD)*1	—	—
	PE1 I/O (port)	TEND0 output (DMAC)	TIOC0B I/O (MTU2)	—	—	—
	PE2 I/O (port)	DREQ1 input (DMAC)	TIOC0C I/O (MTU2)	—	—	—
	PE3 I/O (port)	TEND1 output (DMAC)	TIOC0D I/O (MTU2)	AUDATA3 output (AUD)*1	—	—
	PE4 I/O (port)	$\overline{\text{IOIS16}}$ input (BSC)	TIOC1A I/O (MTU2)	RXD3 input (SCIF)	AUDATA2 output (AUD)*1	—
	PE5 I/O (port)	$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$ output (BSC)	TIOC1B I/O (MTU2)	TXD3 output (SCIF)	AUDATA1 output (AUD)*1	—
	PE6 I/O (port)	$\overline{\text{CS7}}$ output (BSC)	TIOC2A I/O (MTU2)	SCK3 I/O (SCIF)	AUDATA0 output (AUD)*1	—
	PE7 I/O (port)	$\overline{\text{BS}}$ output (BSC)	TIOC2B I/O (MTU2)	$\overline{\text{UBCTRG}}$ output (UBC)	RXD2 input (SCI)	SSI I/O (SSU)
	PE8 I/O (port)	TIOC3A I/O (MTU2)	SCK2 I/O (SCI)	SSCK I/O (SSU)	TMS input (H-UDI)*2	—
	PE9 I/O (port)	TIOC3B I/O (MTU2)	SCK3 I/O (SCIF)	$\overline{\text{RTS3}}$ output (SCIF)	$\overline{\text{TRST}}$ input (H-UDI)*2	—
	PE10 I/O (port)	TIOC3C I/O (MTU2)	TXD2 output (SCI)	SSO I/O (SSU)	TDI input (H-UDI)*2	—
	PE11 I/O (port)	TIOC3D I/O (MTU2)	RXD3 input (SCIF)	$\overline{\text{CTS3}}$ input (SCIF)	TDO output (H-UDI)*2	—
	PE12 I/O (port)	TIOC4A I/O (MTU2)	TXD3 output (SCIF)	$\overline{\text{SCS}}$ I/O (SSU)	TCK input (H-UDI)*2	—
	PE13 I/O (port)	TIOC4B I/O (MTU2)	$\overline{\text{MRES}}$ input (INTC)	$\overline{\text{ASEBRKAK}}$ output (E10A)*2	$\overline{\text{ASEBRK}}$ input (E10A)*2	—
	PE14 I/O (port)	$\overline{\text{WRHH}}$/$\overline{\text{ICIOWR}}$/$\overline{\text{AH}}$ /DQMUU output (BSC)	DACK0 output (DMAC)	TIOC4C I/O (MTU2)	—	—
	PE15 I/O (port)	CKE output (BSC)	DACK1 output (DMAC)	TIOC4D I/O (MTU2)	$\overline{\text{IRQOUT}}$ output (INTC)	—

Notes: 1. Only in F-ZTAT version supporting full functions of E10A.
2. Only in F-ZTAT version.

	Pin Name			
	On-Chip ROM Enabled (MCU Mode 2)		Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities	Initial Function	PFC Selected Function Possibilities
111	PE2	PE2/DREQ1/TIOC0C	PE2	PE2/DREQ1/TIOC0C
113	PE3/(AUDATA3*2)	PE3/TEND1/TIOC0D	PE3/(AUDATA3*2)	PE3/TIOC0D
114	PE4/(AUDATA2*2)	PE4/$\overline{\text{IOIS16}}$/TIOC1A/RXD3	PE4/(AUDATA2*2)	PE4/TIOC1A/RXD3
115	PE5/(AUDATA1*2)	PE5/$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$/TIOC1B/TXD3	PE5/(AUDATA1*2)	PE5/TIOC1B/TXD3
116	PE6/(AUDATA0*2)	PE6/$\overline{\text{CS7}}$/TIOC2A/SCK3	PE6/(AUDATA0*2)	PE6/TIOC2A/SCK3
137	PE7	PE7/$\overline{\text{BS}}$/TIOC2B/$\overline{\text{UBCTRG}}$ /RXD2/SSI	PE7	PE7/TIOC2B/$\overline{\text{UBCTRG}}$ /RXD2/SSI
138	PE8/(TMS*1)	PE8/TIOC3A/SCK2/SSCK	PE8/(TMS*1)	PE8/TIOC3A/SCK2/SSCK
139	PE9/($\overline{\text{TRST}}$*1)	PE9/TIOC3B/SCK3/$\overline{\text{RTS3}}$	PE9/($\overline{\text{TRST}}$*1)	PE9/TIOC3B/SCK3/$\overline{\text{RTS3}}$
140	PE10/(TDI*1)	PE10/TIOC3C/TXD2/SSO	PE10/(TDI*1)	PE10/TIOC3C/TXD2/SSO
142	PE11/(TDO*1)	PE11/TIOC3D/RXD3/$\overline{\text{CTS3}}$	PE11/(TDO*1)	PE11/TIOC3D/RXD3/$\overline{\text{CTS3}}$
143	PE12/(TCK*1)	PE12/TIOC4A/TXD3/$\overline{\text{SCS}}$	PE12/(TCK*1)	PE12/TIOC4A/TXD3/$\overline{\text{SCS}}$
144	PE13/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE13/TIOC4B/$\overline{\text{MRES}}$	PE13/($\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$*1)	PE13/TIOC4B/$\overline{\text{MRES}}$
2	PE14	PE14/$\overline{\text{WRHH}}$/$\overline{\text{ICIOWR}}$/$\overline{\text{AH}}$ /DQMUU/DACK0/TIOC4C	PE14	PE14/TIOC4C
5	PE15	PE15/CKE/DACK1/TIOC4D /$\overline{\text{IRQOUT}}$	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
118	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0
119	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1
120	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2
121	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3
122	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4
123	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5
125	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6
126	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7

Notes: 1. Fixed to TMS, $\overline{\text{TRST}}$, TDI, TDO, TCK, and $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ when using the E10A (in $\overline{\text{ASEMD0}}$ = low).

2. Only in F-ZTAT version supporting full functions of E10A. Fixed as AUD pins when using the AUD function of the E10A.

23.5.2 User Program Mode

The user MAT can be programmed/erased in user program mode. (The user boot MAT cannot be programmed/erased.)

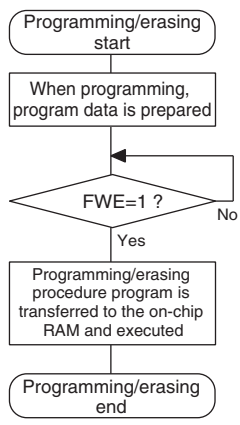
Programming/erasing is executed by downloading the program in the microcomputer.

The overview flow is shown in figure 23.9.

High voltage is applied to internal flash memory during the programming/erasing processing. Therefore, transition to reset must not be executed. Doing so may cause damage or destroy flash memory. If reset is executed accidentally, the reset signal must be released after the reset input period, which is longer than the normal 100 μs.

For details on the programming procedure, see the description in section 23.5.2 (2), Programming Procedure in User Program Mode. For details on the erasing procedure, see the description in section 23.5.2 (3), Erasing Procedure in User Program Mode.

For the overview of a processing that repeats erasing and programming by downloading the programming program and the erasing program in separate on-chip ROM areas using FTDAR, see the description in section 23.5.2 (4), Erasing and Programming Procedure in User Program Mode.



1. RAM emulation mode must be canceled in advance. Download cannot be executed in emulation mode.
2. When the program data is made by means of emulation, the download destination must be changed by FTDAR.
3. Inputting high level to the FWE pin sets the FWE bit to 1.
4. Programming/erasing is executed only in the on-chip RAM. However, if the program data is in a consecutive area and can be accessed by the MOV.B instruction of the CPU like SRAM/ROM, the program data can be in an external space.
5. After programming/erasing is finished, low level must be input to the FWE pin for protection.

Figure 23.9 Programming/Erasing Overview Flow

(1) Select erasure

In response to the erasure selection command, the boot program transfers the program that performs erasure, i.e. erases data in the user MAT.

Command	H'48	

— Command H'48 (1 byte): Selects erasure.

Response	H'06	

— Response H'06 (1 byte): Response to selection of erasure
This ACK code is returned after transfer of the program that performs erasure.

Error response	H'C8	ERROR

— Error response H'C8 (1 byte): Error response to selection of erasure
— ERROR (1 byte): Error code
H'54: Error in selection processing (processing was not completed because of a transfer error.)

(2) Block erasure

In response to the block erasure command, the boot program erases the data in a specified block of the user MAT.

Command	H'58	Size	Block number	SUM

— Command H'58 (1 byte): Erasure of a block
— Size (1 byte): The number of characters in the block number field (fixed at 1)
— Block number (1 byte): Block number of the block to be erased
— SUM (1 byte): Checksum

Response	H'06	

— Response H'06 (1 byte): Response to the block erasure command
This ACK code is returned when the block has been erased.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
SCSMR_3	—	—	—	—	—	—	—	—	SCIF
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	—	CKS[1:0]		(Channel 3)
SCBRR_3									
SCSCR_3	—	—	—	—	—	—	—	—	
	TIE	RIE	TE	RE	REIE	—	CKE[1:0]		
SCFTDR_3									
SCFSR_3	PER[3:0]				FER[3:0]				
	ER	TEND	TDFE	BRK	FER	PER	RDF	DR	
SCFRDR_3									
SCFCR_3	—	—	—	—	—	RSTRG[2:0]			
	RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RFRST	LOOP	
SCFDR_3	—	—	—	T[4:0]					
	—	—	—	R[4:0]					
SCSPTR_3	—	—	—	—	—	—	—	—	
	RTSIO	RTSDT	CTSIO	CTSDT	SCKIO	SCKDT	SPBIO	SPBDT	
SCLSR_3	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	ORER	
TCR_3	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]			MTU2
TCR_4	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]			
TMDR_3	—	—	BFB	BFA	MD[3:0]				
TMDR_4	—	—	BFB	BFA	MD[3:0]				
TIORH_3	IOB[3:0]				IOA[3:0]				
TIORL_3	IOD[3:0]				IOC[3:0]				
TIORH_4	IOB[3:0]				IOA[3:0]				
TIORL_4	IOD[3:0]				IOC[3:0]				
TIER_3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TIER_4	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TOER	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B	
TGCR	—	BDC	N	P	FB	WF	VF	UF	
TOCR1	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP	
TOCR2	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P	

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
ADDR2	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D (Channel 0)
	AD1	AD0	—	—	—	—	—	—	
ADDR3	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADCSR_0	ADF	ADIE	—	—	TRGE	—	CONADF	STC	
	CKSL[1:0]		ADM[1:0]		ADCS	CH[2:0]			
ADCR_0	—	—	ADST	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
ADDR4	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D (Channel 1)
	AD1	AD0	—	—	—	—	—	—	
ADDR5	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR6	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR7	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADCSR_1	ADF	ADIE	—	—	TRGE	—	CONADF	STC	
	CKSL[1:0]		ADM[1:0]		ADCS	CH[2:0]			
ADCR_1	—	—	ADST	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
ADDR8	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D (Channel 2)
	AD1	AD0	—	—	—	—	—	—	
ADDR9	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR11	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR12	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
ADDR13	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D (Channel 2)
	AD1	AD0	—	—	—	—	—	—	
ADDR14	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR15	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADCSR_2	ADF	ADIE	—	—	TRGE	—	CONADF	STC	
	CKSL[1:0]		ADM[1:0]		ADCS	CH[2:0]			
ADCR_2	—	—	ADST	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
FCCS	FWE	MAT	—	FLER	—	—	—	SCO	FLASH
FPCS	—	—	—	—	—	—	—	PPVS	
FECS	—	—	—	—	—	—	—	EPVB	
FKEY	K[7:0]								
FMATS	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0	
FTDAR	TDER	TDA[6:0]							
DTCERA	DTCERA15	DTCERA14	DTCERA13	DTCERA12	DTCERA11	DTCERA10	DTCERA9	DTCERA8	DTC
	—	—	—	—	—	—	—	—	
DTCERB	DTCERB15	DTCERB14	DTCERB13	DTCERB12	DTCERB11	DTCERB10	DTCERB9	DTCERB8	
	DTCERB7	DTCERB6	DTCERB5	DTCERB4	DTCERB3	DTCERB2	DTCERB1	DTCERB0	
DTCERC	DTCERC15	DTCERC14	DTCERC13	DTCERC12	—	—	—	—	
	—	—	—	—	DTCERC3	DTCERC2	DTCERC1	DTCERC0	
DTCERD	DTCERD15	DTCERD14	DTCERD13	DTCERD12	DTCERD11	DTCERD10	DTCERD9	DTCERD8	
	DTCERD7	DTCERD6	DTCERD5	DTCERD4	DTCERD3	—	—	—	
DTCERE	DTCERE15	DTCERE14	DTCERE13	DTCERE12	DTCERE11	DTCERE10	DTCERE9	DTCERE8	
	DTCERE7	DTCERE6	DTCERE5	DTCERE4	—	—	—	—	
DTCCR	—	—	—	RRS	RCHNE	—	—	ERR	
DTCVBR									
					—	—	—	—	
	—	—	—	—	—	—	—	—	

Pin Function		Pin State										
		Reset State				Power-Down State						
		Power-On										
Type	Pin Name	Expansion without ROM 16 bits	Expansion without ROM 32 bits	Expansion with ROM	Single-chip	Manual	Deep Software Standby	Software Standby	Sleep	Bus Master-ship Release	Oscillation Stop Detected	POE Function Used
MTU2	TCLKA to TCLKD	Z				I	Z	Z	I	I	I	I
	TIOC0A to TIOC0D	Z				I/O	Z	K*1	I/O	I/O	I/O	Z
	TIOC1A, TIOC1B	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	TIOC2A, TIOC2B	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	TIOC3A, TIOC3C	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	TIOC3B, TIOC3D	Z				I/O	Z	Z (MZIZEL in HCPCR = 0) K*1 (MZIZEL in HCPCR = 1)	I/O	I/O	I/O*7	Z
	TIOC4A to TIOC4D	Z				I/O	Z	Z (MZIZEL in HCPCR = 0) K*1 (MZIZEL in HCPCR = 1)	I/O	I/O	I/O*7	Z
	TIC5U, TIC5V, TIC5W	Z				I	Z	Z	I	I	I	I
MTU2S	TIOC3AS, TIOC3CS	Z				I/O	Z	K*1	I/O	I/O	I/O	I/O
	TIOC3BS (PD9), TIOC3DS (PD11)	Z				I/O	Z	Z (MZIZDL in HCPCR = 0) K*1 (MZIZDL in HCPCR = 1)	I/O	I/O	I/O*5	Z

		External Space (SDRAM)		
		16-bit Space		
Pin Name		**Upper Byte**	**Lower Byte**	**Word/Longword**
$\overline{AH}$		L	L	L
$\overline{FRAME}$		H	H	H
RDWR	R	H	H	H
	W	L	L	L
$\overline{RD}$	R	H	H	H
	W	H	H	H
$\overline{ICIORD}$	R	H	H	H
	W	H	H	H
$\overline{WRHH}$	R	H	H	H
	W	H	H	H
$\overline{WRHL}$	R	H	H	H
	W	H	H	H
$\overline{WRH}$	R	H	H	H
	W	H	H	H
$\overline{WRL}$	R	H	H	H
	W	H	H	H
$\overline{WE}$	R	H	H	H
	W	H	H	H
$\overline{ICIOWR}$	R	H	H	H
	W	H	H	H
A29 to A0		Address	Address	Address
D31 to D24		Hi-Z	Hi-Z	Hi-Z
D23 to D16		Hi-Z	Hi-Z	Hi-Z
D15 to D8		Data	Hi-Z	Data
D7 to D0		Hi-Z	Data	Data

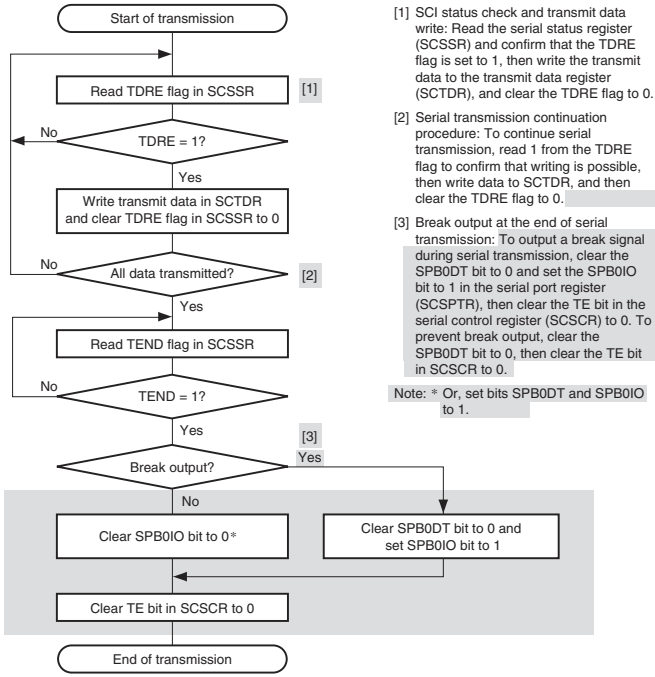
[Legend]

R: Read

W: Write

Notes: 1. Chip select signals corresponding to accessed areas = Low.
The other chip select signals = High.

2. $\overline{RASL}/\overline{CASL}$ = Low when address wherein A25 = 0 is accessed. $\overline{RASU}/\overline{CASU}$ = Low when address wherein A25 = 1 is accessed.

Item	Page	Revision (See Manual for Details)
15.4.2 Operation in Asynchronous Mode (3) Transmitting and Receiving Data Figure 15.4 Sample Flowchart for Transmitting Serial Data (Asynchronous Mode)	778	Figure and title amended 
	779	Description amended B. Transmit data: 8-bit or 7-bit data is output in LSB-first order (when LSB-first transfer is selected).
Figure 15.5 Example of Transmission in Asynchronous Mode (8-Bit Data with Parity and One Stop Bit when LSB-First Transfer is Selected)	780	Figure title amended
Figure 15.6 Sample Flowchart for Receiving Serial Data (Asynchronous Mode) (1)	781	Figure and title amended [3] Serial reception continuation procedure: To continue serial reception, clear the RDRF flag to 0 before the stop bit for the current frame is received.
Figure 15.6 Sample Flowchart for Receiving Serial Data (Asynchronous Mode) (2)	782	Figure title amended