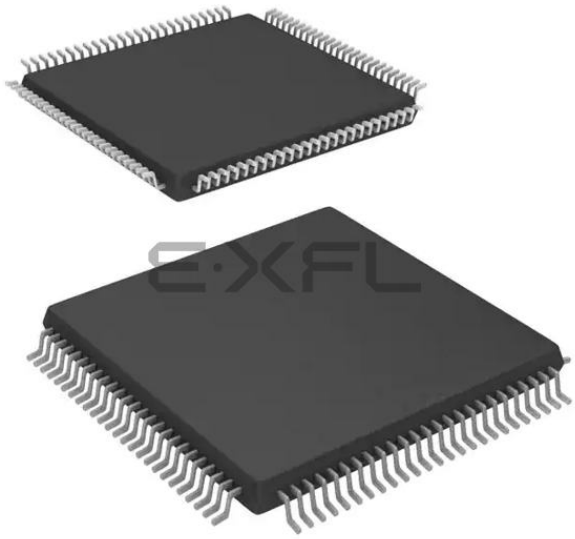

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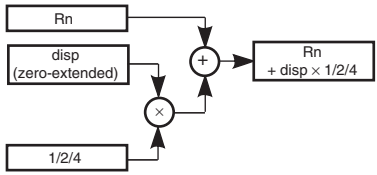
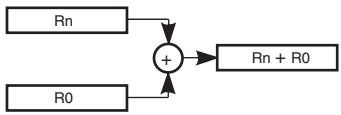
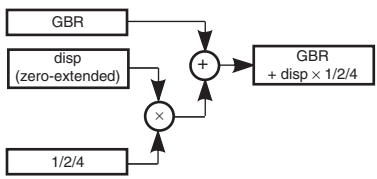
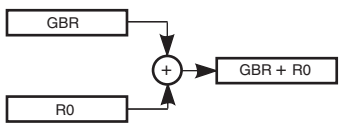
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	65
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds70830an80ftv

Tables

Classification	Symbol	I/O	Name	Function
Multi function timer-pulse unit 2 (MTU2)	TCLKA, TCLKB, TCLKC, TCLKD	I	MTU2 timer clock input	External clock input pins for the timer. Only TCLKB, TCLKC, and TCLKD are available in the SH7083.
	TIOC0A, TIOC0B, TIOC0C, TIOC0D	I/O	MTU2 input capture/output compare (channel 0)	The TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins.
	TIOC1A, TIOC1B	I/O	MTU2 input capture/output compare (channel 1)	The TGRA_1 to TGRB_1 input capture input/output compare output/PWM output pins. Only TIOC1A is available in the SH7083.
	TIOC2A, TIOC2B	I/O	MTU2 input capture/output compare (channel 2)	The TGRA_2 to TGRB_2 input capture input/output compare output/PWM output pins.
	TIOC3A, TIOC3B, TIOC3C, TIOC3D	I/O	MTU2 input capture/output compare (channel 3)	The TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins. Only TIOC3A and TIOC3C are available in the SH7083.
	TIOC4A, TIOC4B, TIOC4C, TIOC4D	I/O	MTU2 input capture/output compare (channel 4)	The TGRA_4 to TGRD_4 input capture input/output compare output/PWM output pins.
	TIC5U, TIC5V, TIC5W	I	MTU2 input capture (channel 5)	The TGRU_5, TGRV_5, and TGRW_5 input capture input pins.
Multi function timer-pulse unit 2S (MTU2S)	TIOC3AS, TIOC3BS, TIOC3CS, TIOC3DS	I/O	MTU2S input capture/output compare (channel 3)	The TGRA_3S to TGRD_3S input capture input/output compare output/PWM output pins.
	TIOC4AS, TIOC4BS, TIOC4CS, TIOC4DS	I/O	MTU2S input capture/output compare (channel 4)	The TGRA_4S to TGRD_4S input capture input/output compare output/PWM output pins.

Addressing Mode	Instruction Format	Effective Address Calculation Method	Calculation Formula
Register indirect with displacement	@(disp:4, Rn)	Effective address is register Rn contents with 4-bit displacement disp added. After disp is zero-extended, it is multiplied by 1 (byte), 2 (word), or 4 (longword), according to the operand size. 	Byte: Rn + disp Word: Rn + disp × 2 Longword: Rn + disp × 4
Index register indirect	@(R0, Rn)	Effective address is sum of register Rn and R0 contents. 	Rn + R0
GBR indirect with displacement	@(disp:8, GBR)	Effective address is register GBR contents with 8-bit displacement disp added. After disp is zero-extended, it is multiplied by 1 (byte), 2 (word), or 4 (longword), according to the operand size. 	Byte: GBR + disp Word: GBR + disp × 2 Longword: GBR + disp × 4
Index GBR indirect	@(R0, GBR)	Effective address is sum of register GBR and R0 contents. 	GBR + R0

Bit	Bit Name	Initial Value	R/W	Description
4	IRQ4F	0	R/W	Indicates the status of an IRQ4 interrupt request. • When level detection mode is selected 0: An IRQ4 interrupt has not been detected [Clearing condition] Driving pin IRQ4 high 1: An IRQ4 interrupt has been detected [Setting condition] Driving pin IRQ4 low • When edge detection mode is selected 0: An IRQ4 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ4F = 1 — Accepting an IRQ4 interrupt 1: An IRQ4 interrupt request has been detected [Setting condition] Detecting the specified edge of pin IRQ4
3	IRQ3F	0	R/W	Indicates the status of an IRQ3 interrupt request. • When level detection mode is selected 0: An IRQ3 interrupt has not been detected [Clearing condition] Driving pin IRQ3 high 1: An IRQ3 interrupt has been detected [Setting condition] Driving pin IRQ3 low • When edge detection mode is selected 0: An IRQ3 interrupt has not been detected [Clearing conditions] — Writing 0 after reading IRQ3F = 1 — Accepting an IRQ3 interrupt 1: An IRQ3 interrupt request has been detected [Setting condition] Detecting the specified edge of pin IRQ3

7. PCMCIA direct interface
   - Supports the IC memory card and I/O card interface defined in JEIDA specifications Ver. 4.2 (PCMCIA2.1 Rev. 2.1)
   - Wait-cycle insertion controllable by program
8. Burst MPX-I/O interface
   - Directly connects peripheral LSIs with address/data multiplexing
   - Supports burst transfer
9. Burst ROM (clock synchronous) interface
   - Directly connects clock-synchronous burst ROM
10. Refresh function
   - Supports the auto-refresh and self-refresh functions
   - Specifies the refresh interval using the refresh counter and clock selection
   - Can execute concentrated refresh by specifying the refresh counts (1, 2, 4, 6, or 8)
11. Usage as interval timer for refresh counter
   - Generates an interrupt request at compare match

Bit	Bit Name	Initial Value	R/W	Description
1, 0	HW[1:0]	00	R/W	Delay Cycles from $\overline{RD}$ and $\overline{WRxx}$ Negation to $\overline{CSn}$ Negation Specify the number of delay cycles from $\overline{RD}$ and $\overline{WRxx}$ negation to $\overline{CSn}$ negation. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

(3) Burst ROM (Asynchronous)

- CS0WCR, CS4WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	BEN	-	-	BW[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	SW[1:0]		W[3:0]				WM	-	-	-	-	HW[1:0]	
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Table 9.28 Relationship between Bus Width, Access Size, and Number of Bursts

Bus Width	BEN Bit	Access Size	Number of Bursts	Number of Accesses
8 bits	Not affected	8 bits	1	1
	Not affected	16 bits	2	1
	Not affected	32 bits	4	1
	0	16 bytes	16	1
	1		4	4
16 bits	Not affected	8 bits	1	1
	Not affected	16 bits	1	1
	Not affected	32 bits	2	1
	0	16 bytes	8	1
	1		2	4
32 bits	Not affected	8 bits	1	1
	Not affected	16 bits	1	1
	Not affected	32 bits	1	1
	Not affected	16 bytes	4	1

Table 9.33 Minimum Number of Idle Cycles between Access Cycles of the DMAC Single Address Mode for the SDRAM Interface (1)

Transfer from the external device with DACK to the SDRAM interface:

BSC Register Setting*1			
CMNCR.DMAIW Setting	**CS3WCR.WTRP Setting**	**CS3WCR.TRWL Setting**	**Minimum Number of Idle Cycles**
0	1	0	1*2
0	1	1	1
0	1	2	2
0	1	3	3
0	2	0	1
0	2	1	2
0	2	2	3
0	2	3	4
0	3	0	2
0	3	1	3
0	3	2	4
0	3	3	5
0	4	0	3
0	4	1	4
0	4	2	5
0	4	3	6
1	1	0	1
1	1	1	1
1	1	2	2
1	1	3	3
1	2	0	1
1	2	1	2
1	2	2	3
1	2	3	4
1	3	0	2
1	3	1	3
1	3	2	4
1	3	3	5
1	4	0	3

11.4.2 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing).

Synchronous operation enables TGR to be incremented with respect to a single time base.

Channels 0 to 4 can all be designated for synchronous operation. Channel 5 cannot be used for synchronous operation.

Example of Synchronous Operation Setting Procedure:

Figure 11.12 shows an example of the synchronous operation setting procedure.

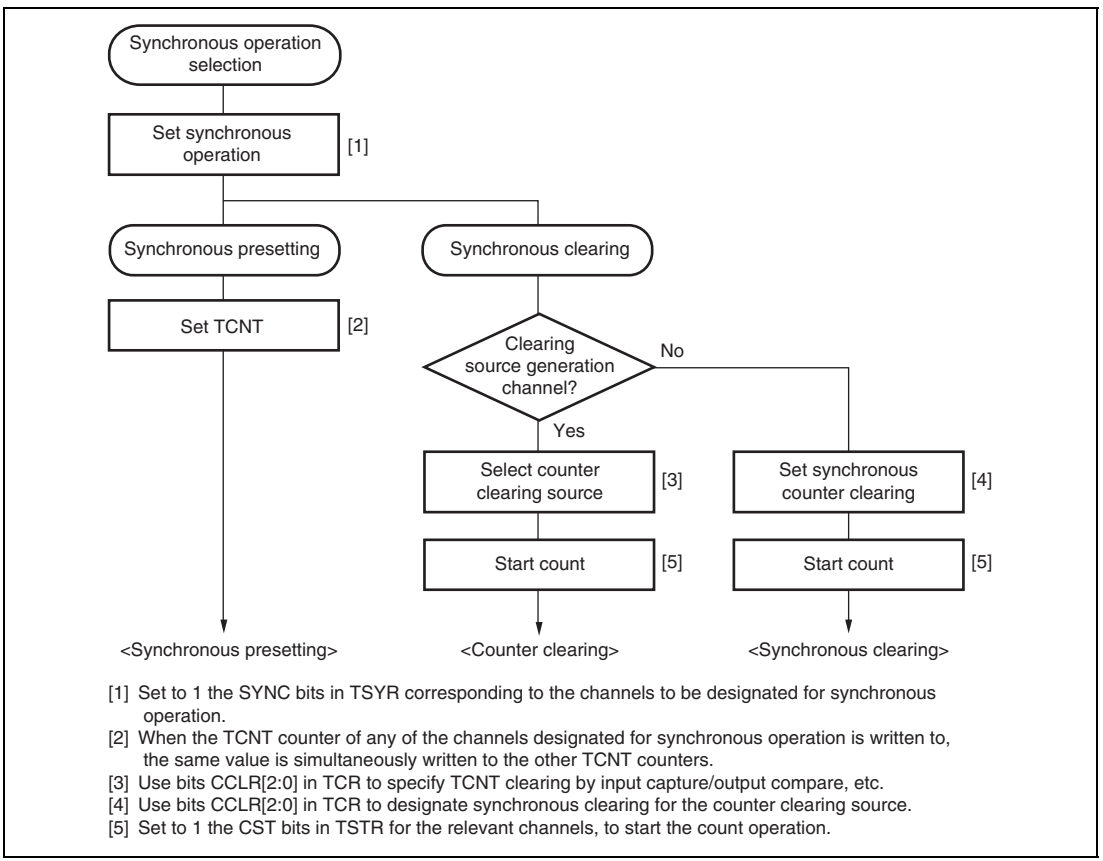


Figure 11.12 Example of Synchronous Operation Setting Procedure

11.4.3 Buffer Operation

Buffer operation, provided for channels 0, 3, and 4, enables TGRC and TGRD to be used as buffer registers. In channel 0, TGRF can also be used as a buffer register.

Buffer operation differs depending on whether TGR has been designated as an input capture register or as a compare match register.

Note: TGRE_0 cannot be designated as an input capture register and can only operate as a compare match register.

Table 11.43 shows the register combinations used in buffer operation.

Table 11.43 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
0	TGRA_0	TGRC_0
	TGRB_0	TGRD_0
	TGRE_0	TGRF_0
3	TGRA_3	TGRC_3
	TGRB_3	TGRD_3
4	TGRA_4	TGRC_4
	TGRB_4	TGRD_4

- When TGR is an output compare register

  When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register.

  This operation is illustrated in figure 11.14.

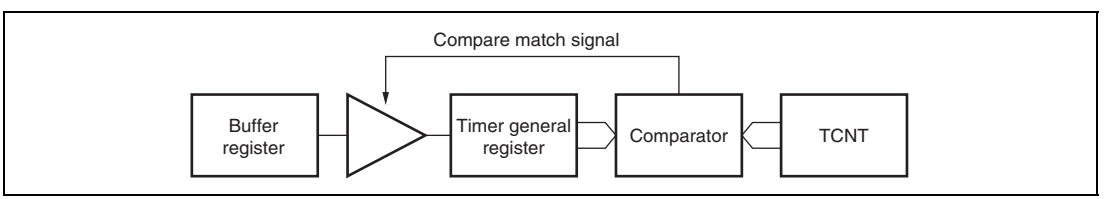


Figure 11.14 Compare Match Buffer Operation

Table 15.8 Maximum Bit Rates with External Clock Input (Asynchronous Mode)

Pϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
10	2.5	156250
12	3.0	187500
14	3.5	218750
16	4.0	250000
18	4.5	281250
20	5.0	312500
22	5.5	343750
24	6.0	375000
26	6.5	406250
28	7.0	437500
30	7.5	468750
32	8.0	500000
34	8.5	531250
36	9.0	562500
38	9.5	593750
40	10.0	625000

17.4.7 Clock Synchronous Communication Mode

In clock synchronous communication mode, data communications are performed via three lines: clock line (SSCK), data input line (SSI), and data output line (SSO).

(1) Initial Settings in Clock Synchronous Communication Mode

Figure 17.12 shows an example of the initial settings in clock synchronous communication mode. Before data transfer, clear both the TE and RE bits in SSER to 0 to set the initial values.

Note: Before changing operating modes and communications formats, clear both the TE and RE bits to 0. Although clearing the TE bit to 0 sets the TDRE bit to 1, clearing the RE bit to 0 does not change the values of the RDRF and ORER bits and SSRDR. Those bits retain the previous values.

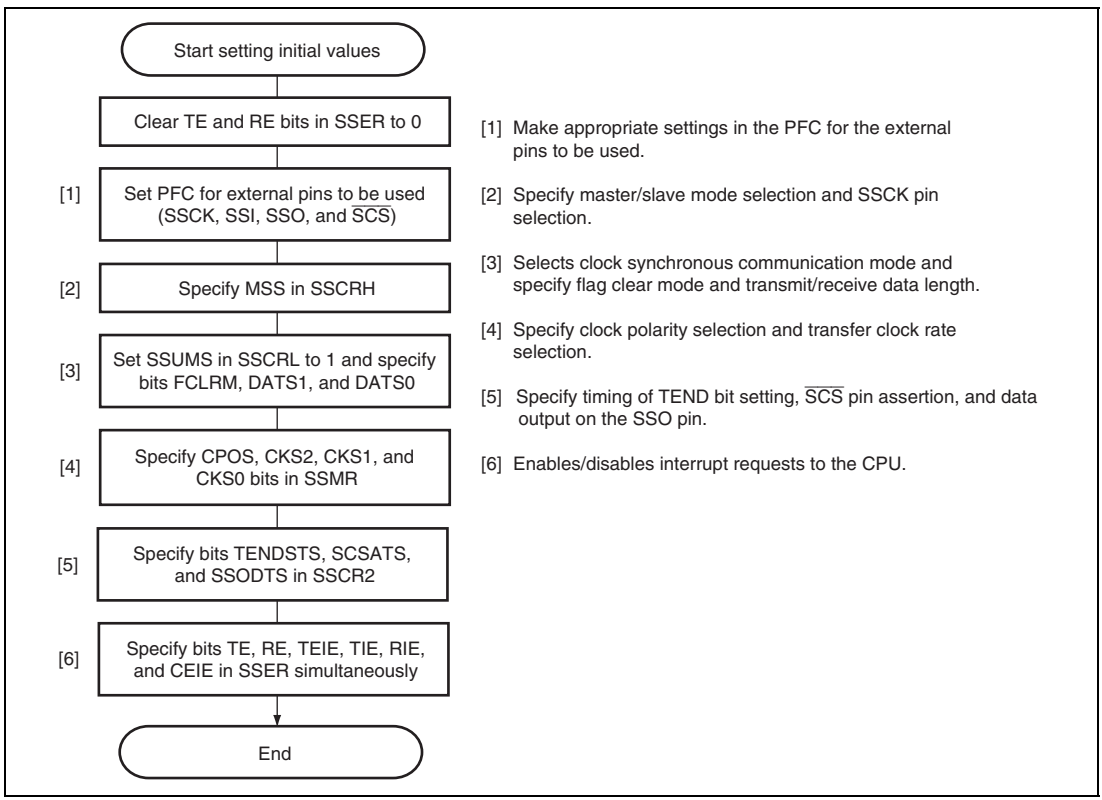


Figure 17.12 Example of Initial Settings in Clock Synchronous Communication Mode

Bit	Bit Name	Initial Value	R/W	Description
14	PE7MD2	0	R/W	PE7 Mode
13	PE7MD1	0	R/W	Select the function of the PE7/$\overline{BS}$/TIOC2B/$\overline{UBCTRG}$/RXD2/SSI pin.
12	PE7MD0	0	R/W	000: PE7 I/O (port) 001: TIOC2B I/O (MTU2) 010: RXD2 input (SCI) 011: $\overline{BS}$ output (BSC)* 101: SSI I/O (SSU) 111: $\overline{UBCTRG}$ output (UBC) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PE6MD2	0	R/W	PE6 Mode
9	PE6MD1	0	R/W	Select the function of the PE6/$\overline{CS7}$/TIOC2A/SCK3/AUDATA0 pin. Fixed to AUDATA0 output when using the AUD function of the E10A.
8	PE6MD0	0	R/W	000: PE6 I/O (port) 001: TIOC2A I/O (MTU2) 010: SCK3 I/O (SCIF) 101: $\overline{CS7}$ output (BSC)* Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

21.1.12 IRQOUT Function Control Register (IFCR)

IFCR is a 16-bit readable/writable register that is used to control the IRQOUT pin output when it is selected as the multiplexed pin function by port D control register H4 (PDCRH4) and port E control register L4 (PECRL4). When PDCRH4 or PECRL4 selects another function, the IFCR setting does not affect the pin function.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	IRQ MD3	IRQ MD2	IRQ MD1	IRQ MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	IRQMD3	0	R/W	Port D $\overline{\text{IRQOUT}}$ Pin Function Select
2	IRQMD2	0	R/W	Select the $\overline{\text{IRQOUT}}$ pin function when bits 9 and 8 (PD30MD1 and PD30MD0) in PDCRH4 are set to B'10. 00: Interrupt request accept signal output 01: Refresh signal output 10: Interrupt request accept signal output or refresh signal output (depends on the operating state) 11: Always high-level output
1	IRQMD1	0	R/W	Port E $\overline{\text{IRQOUT}}$ Pin Function Select
0	IRQMD0	0	R/W	Select the $\overline{\text{IRQOUT}}$ pin function when bits 14 to 12 (PE15MD2 to PE15MD0) in PECRL4 are set to B'011. 00: Interrupt request accept signal output 01: Refresh signal output 10: Interrupt request accept signal output or refresh signal output (depends on the operating state) 11: Always high-level output

22.6.1 Register Descriptions

Port F is an 8-bit input-only port in the SH7083, SH7084, and SH7085; a 16-bit input-only port in the SH7086. Port F has the following register. For details on register addresses and register states during each processing, refer to section 27, List of Registers.

Table 22.11 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port F data register L	PFDRL	R	H'xxxx	H'FFFFD382	8, 16

22.6.2 Port F Data Register L (PFDRL)

The port F data register L (PFDRL) is a 16-bit read-only register that stores port F data. Bits PF7DR to PF0DR correspond to pins PF7 to PF0 (multiplexed functions omitted here) in the SH7083, SH7084, and SH7085. Bits PF15DR to PF0DR correspond to pins PF15 to PF0 (multiplexed functions omitted here) in the SH7086.

Any value written into these bits is ignored, and there is no effect on the state of the pins. When any of the bits are read, the pin state rather than the bit value is read directly. However, when an A/D converter analog input is being sampled, values of 1 are read out. Table 22.12 summarizes port F data register L read/write operations.

23.7 Flash Memory Emulation in RAM

To provide real-time emulation in RAM of data that is to be written to the flash memory, a part of the RAM can be overlaid on an area of flash memory (user MAT) that has been specified by the RAM emulation register (RAMER). After the RAMER setting is made, the RAM is accessible in both the user MAT area and as the RAM area that has been overlaid on the user MAT area. Such emulation is possible in user mode and user program mode.

Figure 23.17 shows an example of the emulation of realtime programming of the user MAT area.

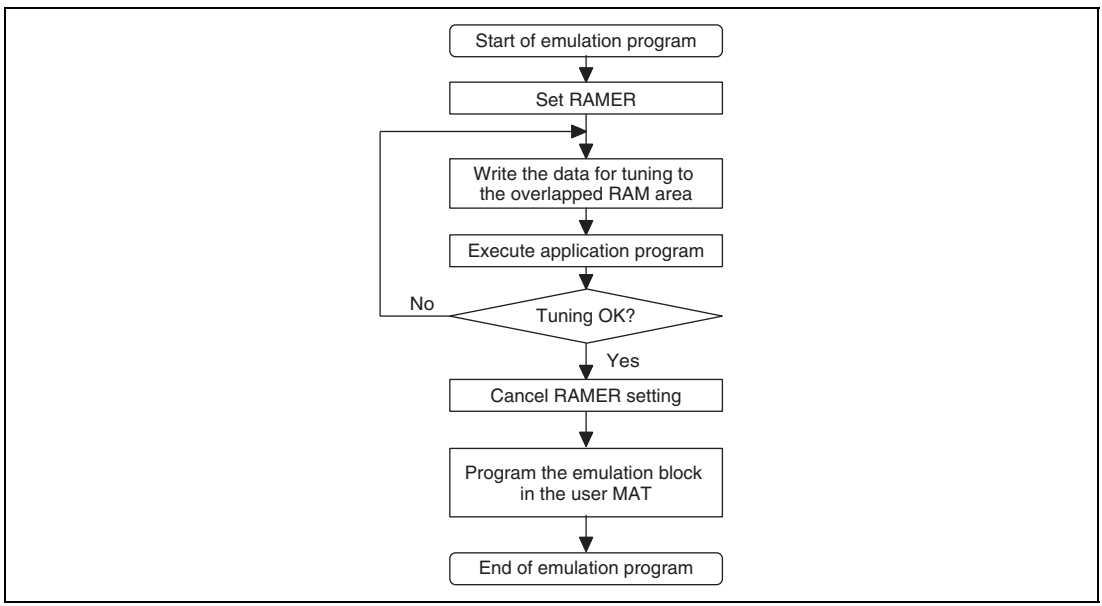


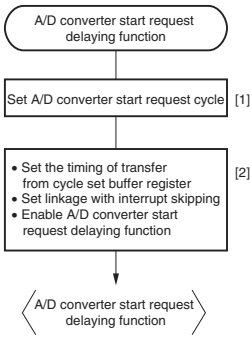
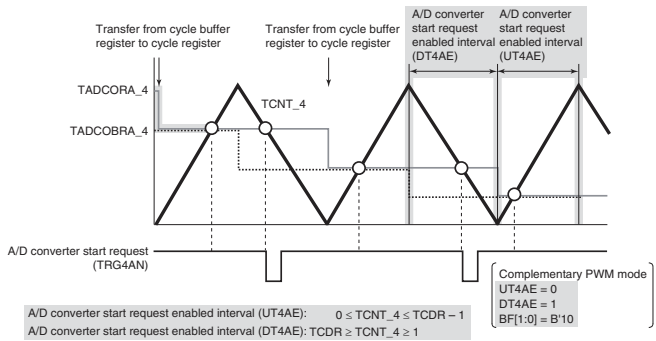
Figure 23.17 Emulation of Flash Memory in RAM

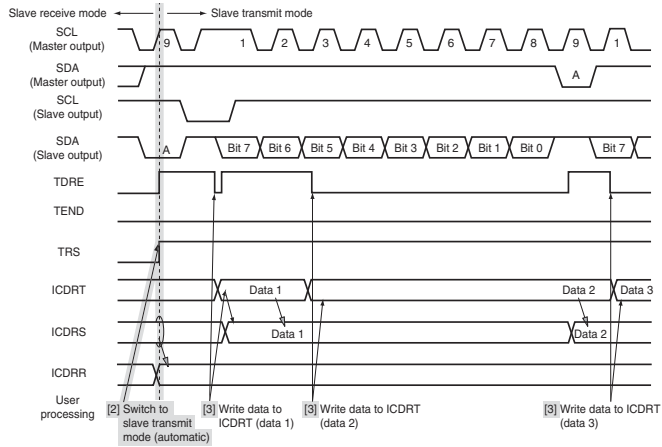
Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
CS2WCR*2	—	—	—	—	—	—	—	—	BSC
	—	—	—	BAS	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		
CS2WCR*5	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	A2CL[1]	
	A2CL[0]	—	—	—	—	—	—	—	
CS3WCR*2	—	—	—	—	—	—	—	—	
	—	—	—	BAS	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		
CS3WCR*5	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	WTRP[1:0]		—	WTRCD[1:0]		—	A3CL[1]	
	A3CL[0]	—	—	TRWL[1:0]		—	WTRC[1:0]		
CS4WCR*2	—	—	—	—	—	—	—	—	
	—	—	—	BAS	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		
CS4WCR*3	—	—	—	—	—	—	—	—	
	—	—	—	BEN	—	—	BW[1:0]		
	—	—	—	SW[1:0]		W[3:1]			
	W[0]	WM	—	—	—	—	HW[1:0]		
CS5WCR*2	—	—	—	—	—	—	—	—	
	—	—	—	BAS	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{CAS}$ delay time	t_{CASD}	1	18	ns	Figures 28.24 to 28.40
DQM delay time	t_{DQMD}	1	18	ns	Figures 28.24 to 28.37
CKE delay time	t_{CKED}	1	18	ns	Figure 28.39
$\overline{AH}$ delay time	t_{AHD}	$1/2t_{Bcyc} + 1$	$1/2t_{Bcyc} + 18$	ns	Figure 28.18
Multiplexed address delay time	t_{MAD}	—	18	ns	Figure 28.18
Multiplexed address hold time	t_{MAH}	1	—	ns	Figure 28.18
DACK, TEND delay time	t_{DACD}	1	18	ns	Figures 28.11 to 28.35
$\overline{FRAME}$ delay time	t_{FMD}	1	18	ns	Figure 28.19 to 28.22
$\overline{ICIORD}$ delay time	t_{ICRSD}	$1/2t_{Bcyc} + 1$	$1/2t_{Bcyc} + 18$	ns	Figures 28.43, 28.44
$\overline{ICIOWR}$ delay time	t_{ICWSD}	$1/2t_{Bcyc} + 1$	$1/2t_{Bcyc} + 18$	ns	Figures 28.43, 28.44
$\overline{IOIS16}$ setup time	t_{IO16S}	$1/2t_{Bcyc} + 13$	—	ns	Figure 28.44
$\overline{IOIS16}$ hold time	t_{IO16H}	$1/2t_{Bcyc} + 10$	—	ns	Figure 28.44

Notes: t_{Bcyc} indicates external bus clock period (Bϕ = CK).

1. n denotes the number of wait cycles.
2. If the access time conditions are satisfied, the t_{RDS1} condition does not need to be satisfied.

Item	Page	Revision (See Manual for Details)
11.4.9 A/D Converter Start Request Delaying Function (a) Example of Procedure for Specifying A/D Converter Start Request Delaying Function Figure 11.79 Example of Procedure for Specifying A/D Converter Start Request Delaying Function	602	Figure amended  [1] Set the cycle in the timer A/D converter start request cycle buffer register (TADCOBRA_4 or TADCOBRB_4) and timer A/D converter start request cycle register (TADCORA_4 or TADCORB_4). (The same initial value must be specified in the cycle buffer register and cycle register.) [2] Use bits BF[1:0] in the timer A/D converter start request control register (TADCR) to specify the timing of transfer from the timer A/D converter start request cycle buffer register to A/D converter start request cycle register. • Specify whether to link with interrupt skipping through bits ITA3AE, ITA4VE, ITB3AE, and ITB4VE. • Use bits TU4AE, DT4AE, UT4BE, and DT4BE to enable A/D conversion start requests (TRG4AN or TRG4BN). Notes: 1. Perform TADCR setting while TCNT_4 is stopped. 2. Set BF1 bit to 0 when complementary PWM mode is not selected. 3. Set ITA3AE, ITA4VE, ITB3AE, ITB4VE, DT4AE, or DT4BE bits to 0 when complementary PWM mode is not selected. 4. Clear the ITA3AE, ITA4VE, ITB3AE, or ITB4VE bit to 0 to disable interrupt skipping.
(b) Basic Operation Example of A/D Converter Start Request Delaying Function Figure 11.80 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation	603	Figure amended 
(c) A/D Converter Start Request Enabled Interval		Section added
(d) Buffer Transfer	604	Description added When using buffer transfer in complementary PWM mode, exercise care regarding the buffer transfer timing. For details, see 11.7.24, Notes on Using the A/D Converter Start Request Delaying Function in Complementary PWM Mode. Also, clear the BF1 bit to 0 when not in complementary PWM mode.

Item	Page	Revision (See Manual for Details)
18.4.4 Slave Transmit Operation Figure 18.10 Slave Transmit Mode Operation Timing (1)	948	Figure amended 
Figure 18.11 Slave Transmit Mode Operation Timing (2)	949	Figure amended