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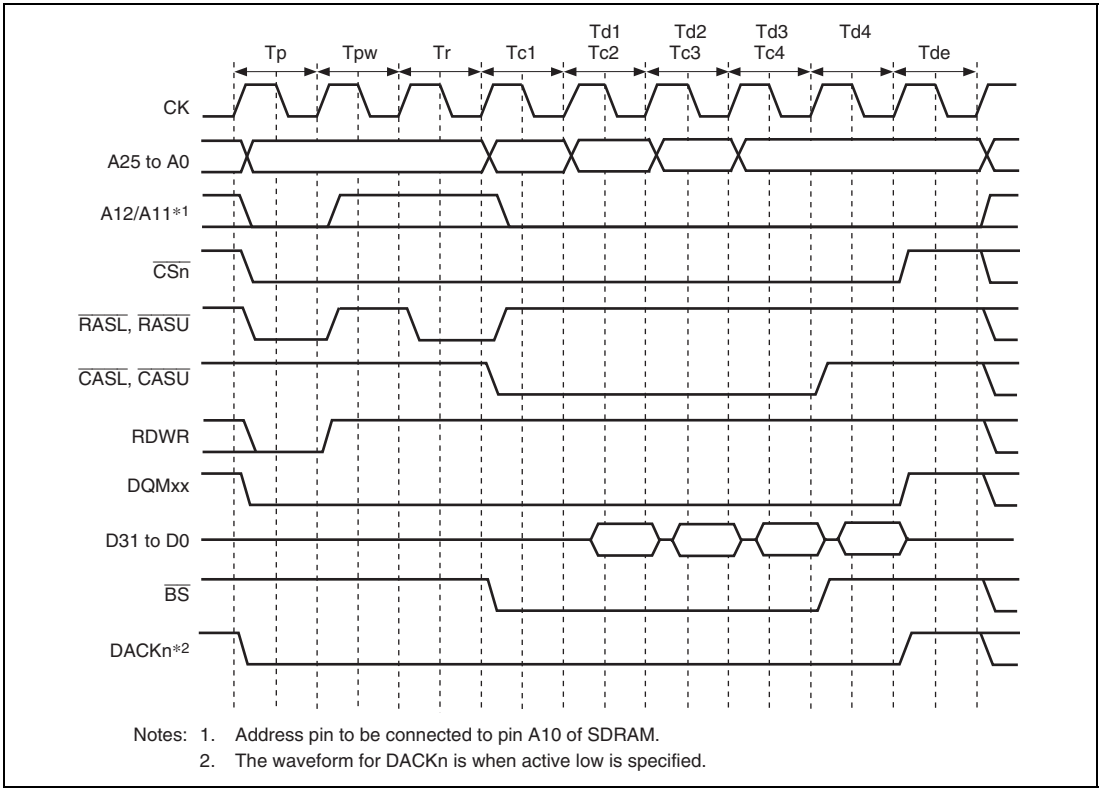
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, FIFO, I²C, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	100
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds70850ad80fpv

Table 6.3 Interrupt Exception Handling Vectors and Priorities

Interrupt Source	Name	Vector No.	Vector Table Starting Address	IPR	Default Priority
User break		12	H'00000030	—	High
External pin	NMI	11	H'0000002C	—	
	IRQ0	64	H'00000100	IPRA15 to IPRA12	
	IRQ1	65	H'00000104	IPRA11 to IPRA8	
	IRQ2	66	H'00000108	IPRA7 to IPRA4	
	IRQ3	67	H'0000010C	IPRA3 to IPRA0	
	IRQ4	68	H'00000110	IPRB15 to IPRB12	
	IRQ5	69	H'00000114	IPRB11 to IPRB8	
	IRQ6	70	H'00000118	IPRB7 to IPRB4	
	IRQ7	71	H'0000011C	IPRB3 to IPRB0	
DMAC_0	DEI0	72	H'00000120	IPRC15 to IPRC12	
DMAC_1	DEI1	76	H'00000130	IPRC11 to IPRC8	
DMAC_2	DEI2	80	H'00000140	IPRC7 to IPRC4	
DMAC_3	DEI3	84	H'00000150	IPRC3 to IPRC0	
MTU2_0	TGIA_0	88	H'00000160	IPRD15 to IPRD12	
	TGIB_0	89	H'00000164		
	TGIC_0	90	H'00000168		
	TGID_0	91	H'0000016C		
	TCIV_0	92	H'00000170	IPRD11 to IPRD8	
	TGIE_0	93	H'00000174		
	TGIF_0	94	H'00000178		
MTU2_1	TGIA_1	96	H'00000180	IPRD7 to IPRD4	
	TGIB_1	97	H'00000184		
	TCIV_1	100	H'00000190	IPRD3 to IPRD0	
	TCIU_1	101	H'00000194		
MTU2_2	TGIA_2	104	H'000001A0	IPRE15 to IPRE12	
	TGIB_2	105	H'000001A4		
	TCIV_2	108	H'000001B0	IPRE11 to IPRE8	
	TCIU_2	109	H'000001B4		Low



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.25 Burst Read Timing (Bank Active, Different Row Addresses)

(2) Transfer from the normal space interface to the external device with DACK

BSC Register Setting*4		Minimum Number of Idle Cycles	
CSnWCR.WM Setting	CSnBCR Idle Setting	When Access Size is Greater than Bus Width*1	When Access Size is Less than or Equal to Bus Width*2
1	0	0	2
0	0	1	3
1	1	1	2
0	1	1	3
1	2	2	2
0	2	2	3
1	4	4	4
0	4	4	4

Notes: DMAC is driven by Bϕ. The minimum number of idle cycles is not affected by changing a clock ratio.

1. Minimum number of idle cycles between the word access to address 0 and the word access to address 2 in the 32-bit access with a 16-bit bus width,
minimum number of idle cycles between the byte access to address 0 and the byte access to address 1 in the 16-bit access with an 8-bit bus width,
minimum number of idle cycles between the byte accesses to address 0, to address 1, to address 2, and to address 3 in the 32-bit access with an 8-bit bus width, and
minimum number of idle cycles between consecutive accesses in 16-byte transfer.
2. Other than the above cases.
3. For single address mode transfer from the external device with DACK to the normal space interface, the minimum number of idle cycles is not affected by the IWW, IWRWD, IWRWS, IWRRD, and IWRRS bits in CSnBCR.
4. For single address mode transfer from the normal space interface to the external device with DACK, the minimum number of idle cycles is not affected by the DMAIWA and DMAIW bits in CMNCR.
5. When the HW[1:0] in the CSnWCR is set to specify 2.5 cycles or more, the number of idle cycles will be 0.

10.5.11 Number of Cycles per Access to On-Chip RAM by DMAC

The number of cycles required for read/write access to on-chip RAM from the DMAC is as shown in table 10.9, which differs depending on the frequency ratio of Iϕ (internal clock) to Bϕ (external bus clock).

Table 10.9 Number of Cycles per Access to On-Chip RAM by DMAC

Setting of Iϕ:Bϕ	Read	Write
1:1	3 × Bcyc	3 × Bcyc
1:1/2	2 × Bcyc	1 × Bcyc
1:1/3	2 × Bcyc	1 × Bcyc
1:1/4 or less	1 × Bcyc	1 × Bcyc

Notes: 1. Bcyc is the external bus clock cycle.
2. The number of cycles for access to the on-chip peripheral I/O or an external device are indicated in section 9.5.16, Access to On-Chip Peripheral I/O Registers by CPU, and section 9.5.17, Access to External Memory by CPU. The access cycles are obtained by subtracting the cycles of Iϕ required for L-bus access from the cycles required for access by the CPU.

10.5.12 Note on DMAC Transfer in Burst Mode when Activation Source Is MTU2

The corresponding bit among DMMTU4 to DMMTU0 in the bus function extending register (BSCEHR) must be set when performing DMA transfer in burst mode with the MTU2 specified as the activation source. For details, see section 9.4.8, Bus Function Extending Register (BSCEHR).

10.5.13 Bus Function Extending Register (BSCEHR)

With the bus function extending register (BSCEHR), it is possible to set the function to perform transfer by the DMAC preferentially. For details, see section 9.4.8, Bus Function Extending Register (BSCEHR).

- TSR2_0

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	TGFF	TGFE
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/(W)*	R/(W)*

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TGFF	0	R/(W)*[1]	Compare Match Flag F Status flag that indicates the occurrence of compare match between TCNT_0 and TGRF_0. [Setting condition] • When TCNT_0 = TGRF_0 and TGRF_0 is functioning as a compare register [Clearing condition] • When 0 is written to TGFF after reading TGFF = 1*[2]
0	TGFE	0	R/(W)*[1]	Compare Match Flag E Status flag that indicates the occurrence of compare match between TCNT_0 and TGRE_0. [Setting condition] • When TCNT_0 = TGRE_0 and TGRE_0 is functioning as compare register [Clearing condition] • When 0 is written to TGFE after reading TGFE = 1*[2]

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.
2. If another flag setting condition occurs before writing 0 to the bit after reading it as 1, the flag will not be cleared by writing 0 to it once. In this case, read the bit as 1 again and write 0 to it.

Bit	Bit Name	Initial Value	R/W	Description
0	OE3B	0	R/W	Master Enable TIOC3B This bit enables/disables the TIOC3B pin MTU2 output. 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled

Note: * The inactive level is determined by the settings in timer output control registers 1 and 2 (TOCR1 and TOCR2). For details, refer to section 11.3.20, Timer Output Control Register 1 (TOCR1), and section 11.3.21, Timer Output Control Register 2 (TOCR2). Set these bits to 1 to enable MTU2 output in other than complementary PWM or reset-synchronized PWM mode. When these bits are set to 0, low level is output.

11.3.20 Timer Output Control Register 1 (TOCR1)

TOCR1 is an 8-bit readable/writable register that enables/disables PWM synchronized toggle output in complementary PWM mode/reset synchronized PWM mode, and controls output level inversion of PWM output.

Bit:	7	6	5	4	3	2	1	0
	-	PSYE	-	-	TOCL	TOCS	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R/(W)*	R/W	R/W	R/W

Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.

Bit	Bit Name	Initial value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PSYE	0	R/W	PWM Synchronous Output Enable This bit selects the enable/disable of toggle output synchronized with the PWM period. 0: Toggle output is disabled 1: Toggle output is enabled
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.4.5 PWM Modes

In PWM mode, PWM waveforms are output from the output pins. The output level can be selected as 0, 1, or toggle output in response to a compare match of each TGR.

TGR registers settings can be used to output a PWM waveform in the range of 0% to 100% duty.

Designating TGR compare match as the counter clearing source enables the period to be set in that register. All channels can be designated for PWM mode independently. Synchronous operation is also possible.

There are two PWM modes, as described below.

1. PWM mode 1

   PWM output is generated from the TIOCA and TIOCC pins by pairing TGRA with TGRB and TGRC with TGRD. The output specified by bits IOA[3:0] and IOC[3:0] in TIOR is output from the TIOCA and TIOCC pins at compare matches A and C, and the output specified by bits IOB[3:0] and IOD[3:0] in TIOR is output at compare matches B and D. The initial output value is the value set in IOA[3:0] or IOC[3:0]. If the set values of paired TGRs are identical, the output value does not change when a compare match occurs.

   In PWM mode 1, a maximum 8-phase PWM output is possible.

2. PWM mode 2

   PWM output is generated using one TGR as the cycle register and the others as duty registers. The output specified in TIOR is performed by means of compare matches. Upon counter clearing by a cycle register compare match, the output value of each pin is the initial value set in TIOR. If the set values of the cycle and duty registers are identical, the output value does not change when a compare match occurs.

   In PWM mode 2, a maximum 8-phase PWM output is possible in combination use with synchronous operation.

The correspondence between PWM output pins and registers is shown in table 11.46.

11.7.16 Overflow Flags in Reset Synchronous PWM Mode

When set to reset synchronous PWM mode, TCNT_3 and TCNT_4 start counting when the CST3 bit of TSTR is set to 1. At this point, TCNT_4's count clock source and count edge obey the TCR_3 setting.

In reset synchronous PWM mode, with cycle register TGRA_3's set value at H'FFFF, when specifying TGR3A compare-match for the counter clear source, TCNT_3 and TCNT_4 count up to H'FFFF, then a compare-match occurs with TGRA_3, and TCNT_3 and TCNT_4 are both cleared. At this point, TSR's overflow flag TCFV bit is not set.

Figure 11.134 shows a TCFV bit operation example in reset synchronous PWM mode with a set value for cycle register TGRA_3 of H'FFFF, when a TGRA_3 compare-match has been specified without synchronous setting for the counter clear source.

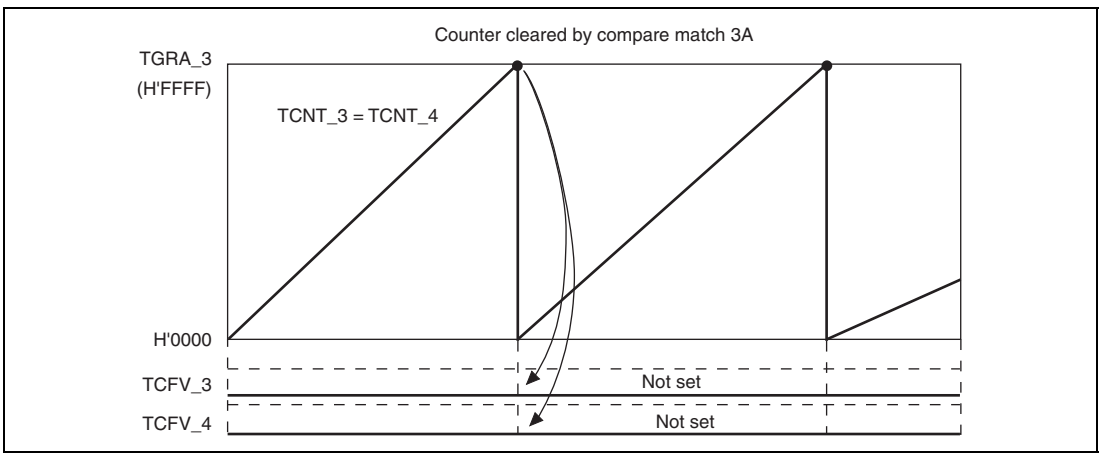


Figure 11.134 Reset Synchronous PWM Mode Overflow Flag

Bit	Bit Name	Initial value	R/W	Description
1	MTU2SP8CZE	0	R/W*	MTU2S Port 8 Output Comparison/High-Impedance Enable This bit specifies whether to compare output levels for the MTU2S high-current PD27/TIOC4AS and PD25/TIOC4CS pins and to place them in high-impedance state when the OSF2 bit is set to 1 while the OCE2 bit is 1 or when any one of the POE4F, POE5F, POE6F, POE7F, and MTU2SHIZ bits is set to 1. 0: Does not compare output levels or place the pins in high-impedance state 1: Compares output levels and places the pins in high-impedance state
0	MTU2SP9CZE	0	R/W*	MTU2S Port 9 Output Comparison/High-Impedance Enable This bit specifies whether to compare output levels for the MTU2S high-current PD26/TIOC4BS and PD24/TIOC4DS pins and to place them in high-impedance state when the OSF2 bit is set to 1 while the OCE2 bit is 1 or when any one of the POE4F, POE5F, POE6F, POE7F, and MTU2SHIZ bits is set to 1. 0: Does not compare output levels or place the pins in high-impedance state 1: Compares output levels and places the pins in high-impedance state

Note: * Can be modified only once after a power-on reset.

Table 16.9 Bit Rates and SCBRR Settings in Clock Synchronous Mode

Bit Rate (bits/s)	Pϕ (MHz)							
	34		36		38		40	
	n	N	n	N	n	N	n	N
250								
500								
1000	3	132	3	140	3	147	3	155
2500	2	212	2	224	2	237	2	249
5000	2	105	2	112	2	118	2	124
10000	1	212	1	224	1	237	1	249
25000	1	84	1	89	1	94	1	99
50000	0	169	0	179	0	189	0	199
100000	0	84	0	89	0	94	0	99
250000	0	33	0	35	0	37	0	39
500000	0	16	0	17	0	18	0	19
1000000	—	—	0	8	—	—	0	9
2500000	—	—	—	—	—	—	0	3
5000000	—	—	—	—	—	—	0	1

[Legend]
Blank: No setting possible
—: Setting possible, but error occurs
*: Continuous transmission/reception is disabled.
Note: Settings with an error of 1% or less are recommended.

Table 16.10 indicates the maximum bit rates in asynchronous mode when the baud rate generator is used. Tables 16.11 and 16.12 list the maximum rates for external clock input.

16.5 SCIF Interrupt Sources and DTC

The SCIF has four interrupt sources: transmit-FIFO-data-empty (TXIF), receive-error (ERIF), receive-data-full (RXIF), and break (BRIF).

Table 16.16 shows the interrupt sources and their order of priority. The interrupt sources are enabled or disabled by means of the TIE, RIE, and REIE bits in SCSCR. A separate interrupt request is sent to the interrupt controller for each of these interrupt sources.

When TXIF request is enabled by TIE bit and the TDFE flag in the serial status register (SCFSR) is set to 1, a TXIF interrupt request is generated.

When RXIF request is enabled by RIE bit and the RDF or DR flag in SCFSR is set to 1, an RXIF interrupt request is generated. The RXIF interrupt request caused by DR flag is generated only in asynchronous mode.

When BRIF request is enabled by RIE bit or REIE bit and the BRK flag in SCFSR or ORER flag in SCLSR is set to 1, a BRIF interrupt request is generated.

When ERIF request is enabled by RIE bit or REIE bit and the ER flag in SCFCR is set to 1, an ERIF interrupt request is generated.

When the RIE bit is set to 0 and the REIE bit is set to 1, SCIF request ERIF interrupt and BRIF interrupt without requesting RXIF interrupt.

The TXIF interrupt indicates that transmit data can be written, and the RXIF interrupt indicates that there is receive data in SCFRDR.

Table 16.16 SCIF Interrupt Sources

Interrupt Source	Description	Interrupt Enable Bit	DTC Activation
ERIF	Interrupt initiated by receive error (ER)	RIE or REIE	—
RXIF	Interrupt initiated by receive data FIFO full (RDF) or data ready (DR)	RIE	√
BRIF	Interrupt initiated by break (BRK) or overrun error (ORER)	RIE or REIE	—
TXIF	Interrupt initiated by transmit FIFO data empty (TDFE)	TIE	√

16.7.3 Break Detection and Processing

When data containing a framing error is received and then space 0 (low level) is input for more than one frame length, a break (BRK) is detected. When a break is detected, not only the transfer of receive data (H'00) to SCFRDR but also the setting in SCRSR of serial data input on the RXD pin is stopped. If the RIE or REIE bit in SCSCR is set to 1, a break interrupt request (BRI) is issued. Reception resumes when the break ends and the receive signal is mark 1 (high level).

It is also possible to perform break detection by reading the value of the RXD pin directly when a framing error (FER) is detected. Use the port register to read the value of the RXD pin. In the break state the input from the RXD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set.

16.7.4 Sending a Break Signal

The I/O condition and level of the TXD pin are determined by the SPBIO and SPBDT bits in the serial port register (SCSPTR). This feature can be used to send a break signal.

Until TE bit is set to 1 (enabling transmission) after initializing, TXD pin does not work. During the period, mark status is performed by SPBDT bit. Therefore, the SPBIO and SPBDT bits should be set to 1 (high level output).

To send a break signal during serial transmission, clear the SPBDT bit to 0 (designating low level), then clear the TE bit to 0 (halting transmission). When the TE bit is cleared to 0, the transmitter is initialized regardless of the current transmission state, and 0 is output from the TXD pin.

16.7.5 Receive Data Sampling Timing and Receive Margin (Asynchronous Mode)

The SCIF operates on a base clock with a frequency of 16 times the transfer rate. In reception, the SCIF synchronizes internally with the fall of the start bit, which it samples on the base clock. Receive data is latched at the rising edge of the eighth base clock pulse. The timing is shown in figure 16.23.

(3) Receive Operation

In receive mode, data is latched at the rise of the transfer clock. The transfer clock is output when MST in ICCR1 is 1, and is input when MST is 0. For receive mode operation timing, refer to figure 18.16. The reception procedure and operations in receive mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MST and CKS[3:0] bits in ICCR1. (Initial setting)
2. When the transfer clock is output, set MST to 1 to start outputting the receive clock.
3. When the receive operation is completed, data is transferred from ICDRS to ICDRR and RDRF in ICSR is set. When MST = 1, the next byte can be received, so the clock is continually output. The continuous reception is performed by reading ICDRR every time RDRF is set. When the 8th clock is risen while RDRF is 1, the overrun is detected and AL/OVE in ICSR is set. At this time, the previous reception data is retained in ICDRR.
4. To stop receiving when MST = 1, set RCVD in ICCR1 to 1, then read ICDRR. Then, SCL is fixed high after receiving the next byte data.

Notes: Follow the steps below to receive only one byte with MST=1 specified. See figure 18.17 for the operation timing.

1. Set the ICE bit in ICCR1 to 1. Set bits CKS[3:0] in ICCR1. (Initial setting)
2. Set MST=1 while the RCVD bit in ICCR1 is 0. This causes the receive clock to be output.
3. Check if the BC[2] bit in ICMR is set to 1 and then set the RCVD bit in ICCR1 to 1. This causes the SCL to be fixed to the high level after outputting one byte of the receive clock.

19.4.3 Single-Cycle Scan Mode

In single-cycle scan mode, A/D conversion is to be performed once on the specified channels (up to four channels in SH7083/SH7084/SH7085 and up to eight channels in SH7086).

1. When the ADST bit in ADCR is set to 1 by a software, MTU2, MTU2S, or external trigger input, A/D conversion starts on the channel with the lowest number in the group (AN0, AN1, ..., AN7).
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends.
4. After A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the idle state. When the ADST bit is cleared to 0 during A/D conversion, A/D conversion stops and the A/D converter enters the idle state.

19.4.4 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit for each module. The A/D converter samples the analog input when the A/D conversion start delay time (t_D) has passed after the ADST bit in ADCR is set to 1, then starts conversion. Figure 19.2 shows the A/D conversion timing. Table 19.4 shows the A/D conversion time.

As indicated in figure 19.2, the A/D conversion time (t_{CONV}) includes t_D and the input sampling time (t_{SPL}). The length of t_D varies depending on the timing of the write access to ADCR. The total conversion time therefore varies within the ranges indicated in table 19.4.

In scan mode, the values given in table 19.4 apply to the first conversion time. The values given in table 19.5 apply to the second and subsequent conversions.

Bit	Bit Name	Initial Value	R/W	Description
14	PE15MD2	0	R/W	PE15 Mode
13	PE15MD1	0	R/W	Select the function of the PE15/CKE/DACK1/TIOC4D/$\overline{\text{IRQOUT}}$ pin.
12	PE15MD0	0	R/W	000: PE15 I/O (port)
				001: TIOC4D I/O (MTU2)
				010: DACK1 output (DMAC)*
				011: $\overline{\text{IRQOUT}}$ output (INTC)
				101: CKE output (BSC)*
				Other than above: Setting prohibited
11	—	0	R	Reserved
				This bit is always read as 0. The write value should always be 0.
10	PE14MD2	0	R/W	PE14 Mode
9	PE14MD1	0	R/W	Select the function of the PE14/$\overline{\text{AH}}$/DACK0/TIOC4C pin.
8	PE14MD0	0	R/W	000: PE14 I/O (port)
				001: TIOC4C I/O (MTU2)
				010: DACK0 output (DMAC)*
				101: $\overline{\text{AH}}$ output (BSC)*
				Other than above: Setting prohibited
7, 6	—	All 0	R	Reserved
				These bits are always read as 0. The write value should always be 0.
5	PE13MD1	0	R/W	PE13 Mode
4	PE13MD0	0	R/W	Select the function of the PE13/TIOC4B/$\overline{\text{MRES}}$ pin.
				00: PE13 I/O (port)
				01: TIOC4B I/O (MTU2)
				10: $\overline{\text{MRES}}$ input (INTC)
				Other than above: Setting prohibited
3	—	0	R	Reserved
				This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	PE10MD2	0	R/W	PE10 Mode
9	PE10MD1	0	R/W	Select the function of the PE10/TIOC3C/TXD2/SSO
8	PE10MD0	0	R/W	pin. 000: PE10 I/O (port) 001: TIOC3C I/O (MTU2) 010: TXD2 output (SCI) 101: SSO I/O (SSU) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PE9MD2	0	R/W	PE9 Mode
5	PE9MD1	0	R/W	Select the function of the PE9/TIOC3B/SCK3/$\overline{\text{RTS3}}$
4	PE9MD0	0	R/W	pin. 000: PE9 I/O (port) 001: TIOC3B I/O (MTU2) 011: SCK3 I/O (SCIF) 100: $\overline{\text{RTS3}}$ output (SCIF) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PE8MD2	0	R/W	PE8 Mode
1	PE8MD1	0	R/W	Select the function of the PE8/TIOC3A/SCK2/SSCK
0	PE8MD0	0	R/W	pin. 000: PE8 I/O (port) 001: TIOC3A I/O (MTU2) 010: SCK2 I/O (SCI) 101: SSCK I/O (SSU) Other than above: Setting prohibited

- PCDRH (SH7083, SH7084, SH7085)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- PCDRH (SH7086)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PC25 DR	PC24 DR	PC23 DR	PC22 DR	PC21 DR	PC20 DR	PC19 DR	PC18 DR	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PC25DR	0	R/W	See table 22.6.
8	PC24DR	0	R/W	
7	PC23DR	0	R/W	
6	PC22DR	0	R/W	
5	PC21DR	0	R/W	
4	PC20DR	0	R/W	
3	PC19DR	0	R/W	
2	PC18DR	0	R/W	
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

26.7 Module Standby Mode

26.7.1 Transition to Module Standby Mode

Setting the MSTP bits in the standby control registers (STBCR2 to STBCR5) to 1 halts the supply of clocks to the corresponding on-chip peripheral modules. This function can be used to reduce the power consumption in normal mode.

Do not access registers of an on-chip peripheral module which has been set to enter module standby mode. For details on the states of on-chip peripheral module registers in module standby mode, refer to section 27.3, Register States in Each Operating Mode.

26.7.2 Canceling Module Standby Function

The module standby function can be canceled by clearing the MSTP bits in STBCR2 to STBCR5 to 0. The module standby function can be canceled by a power-on reset for modules whose MSTP bit has an initial value of 0.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
CS5WCR*6	—	—	—	—	—	—	—	—	BSC
	—	—	SZSEL	MPXW	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		
CS5WCR*7	—	—	—	—	—	—	—	—	
	—	—	SA[1:0]		—	—	—	—	
	—	TED[3:0]				PCW[3:1]			
	PCW[0]	WM	—	—	TEH[3:0]				
CS6WCR*2	—	—	—	—	—	—	—	—	
	—	—	—	BAS		WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		
CS6WCR*7	—	—	—	—	—	—	—	—	
	—	—	SA[1:0]		—	—	—	—	
	—	TED[3:0]				PCW[3:1]			
	PCW[0]	WM	—	—	TEH[3:0]				
CS6WCR*8	—	—	—	—	—	—	—	—	
	—	—	MPXAW[1:0]		MPXMD	—	BW[1:0]		
	—	—	—	—	—	W[3:1]			
	W[0]	WM	—	—	—	—	—	—	
CS7WCR*2	—	—	—	—	—	—	—	—	
	—	—	—	BAS	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		
CS8WCR*2	—	—	—	—	—	—	—	—	
	—	—	—	BAS	—	WW[2:0]			
	—	—	—	SW[1:0]		WR[3:1]			
	WR[0]	WM	—	—	—	—	HW[1:0]		

Item	Page	Revision (See Manual for Details)
15.3.10 Bit Rate Register (SCBRR) Table 15.7 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (Clock Synchronous Mode)	769	Table replaced
15.3.10 Bit Rate Register (SCBRR) Table 15.8 Maximum Bit Rates with External Clock Input (Asynchronous Mode)	770	Table amended

Pφ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
10	2.5	156250
12	3.0	187500
14	3.5	218750
16	4.0	250000
18	4.5	281250
20	5.0	312500
22	5.5	343750
24	6.0	375000
26	6.5	406250
28	7.0	437500
30	7.5	468750
32	8.0	500000
34	8.5	531250
36	9.0	562500
38	9.5	593750
40	10.0	625000

Table 15.9 Maximum Bit Rates with External Clock Input (Clock Synchronous Mode)	771	Table amended

Pφ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
10	1.6667	1666666
12	2.0000	2000000
14	2.3333	2333333
16	2.6667	2666666
18	3.0000	3000000
20	3.3333	3333333
22	3.6667	3666666
24	4.0000	4000000
26	4.3333	4333333
28	4.6667	4666666
30	5.0000	5000000
32	5.3333	5333333
34	5.6667	5666666
36	6.0000	6000000
38	6.3333	6333333
40	6.6667	6666666