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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | EBI/EMI |
| Peripherals | POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | ROM |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.600", 15.24mm) |
| Supplier Device Package | 28-DIP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86c3312pecr2035 |

## PIN DESCRIPTION

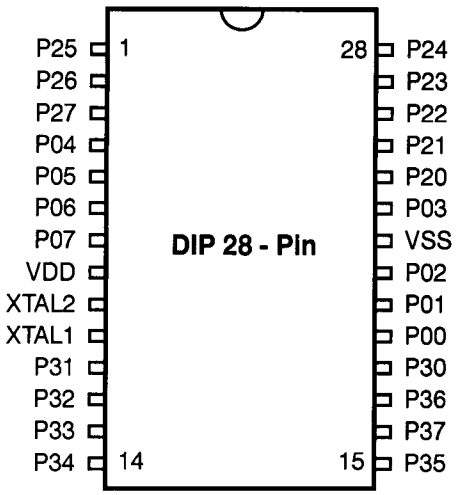



Figure 2. 28-Pin DIP/SOIC Pin Configuration

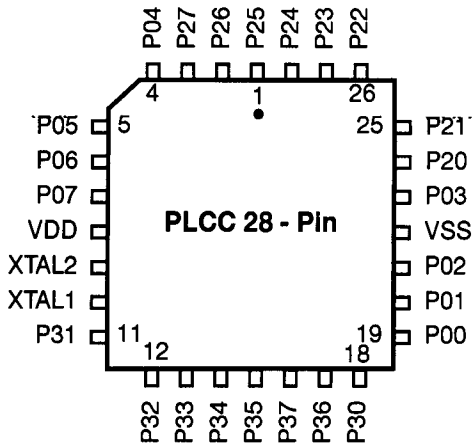



Figure 3. 28-Pin PLCC Pin Configuration

Table 1. 28-Pin DIP/SOIC/PLCC Pin Identification

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1-3 | P25-27 | Port 2, Pins 5,6,7 | In/Output |
| 4-7 | P04-07 | Port 0, Pins 4,5,6,7 | In/Output |
| 8 | $V_{DD}$ | Power Supply | |
| 9 | XTAL2 | Crystal Oscillator | Output |
| 10 | XTAL1 | Crystal Oscillator | Input |
| 11-13 | P31-33 | Port 3, Pins 1,2,3 | Fixed Input |
| 14-15 | P34-35 | Port 3, Pins 4,5 | Fixed Output |
| 16 | P37 | Port 3, Pin 7 | Fixed Output |
| 17 | P36 | Port 3, Pin 6 | Fixed Output |
| 18 | P30 | Port 3, Pin 0 | Fixed Input |
| 19-21 | P00-02 | Port 0, Pins 0,1,2 | In/Output |
| 22 | $V_{SS}$ | Ground | |
| 23 | P03 | Port 0, Pin 3 | In/Output |
| 24-28 | P20-24 | Port 2, Pins 0,1,2,3,4 | In/Output |

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7.)

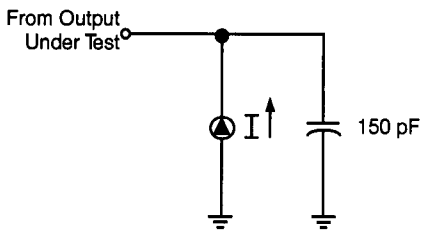



**Figure 7. Test Load Diagram**

## CAPACITANCE

$T_A$ = 25°C, $V_{CC}$ = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND

| Parameter | Min | Max |
|---|---|---|
| Input capacitance | 0 | 12 pF |
| Output capacitance | 0 | 12 pF |
| I/O capacitance | 0 | 12 pF |

## DC ELECTRICAL CHARACTERISTICS

| Sym | Parameter | $V_{CC}$ Note [3] | $T_A$ = 0° C to +70°C Min | Max | $T_A$ = –40°C to +105°C Min | Max | Typical [1] @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CH}$ | Clock Input High Voltage | 3.0V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 1.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.6 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 3.0V | GND-0.3 | 0.2 $V_{CC}$ | GND-0.3 | 0.2 $V_{CC}$ | 1.2 | V | Driven by External Clock Generator | |
| | | 5.5V | GND-0.3 | 0.2 $V_{CC}$ | GND-0.3 | 0.2 $V_{CC}$ | 2.1 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 3.0V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 1.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.6 | V | | |
| $V_{IL}$ | Input Low Voltage | 3.0V | GND-0.3 | 0.2 $V_{CC}$ | GND-0.3 | 0.2 $V_{CC}$ | 1.1 | V | | |
| | | 5.5V | GND-0.3 | 0.2 $V_{CC}$ | GND-0.3 | 0.2 $V_{CC}$ | 1.6 | V | | |
| $V_{OH1}$ | Output High Voltage | 3.0V | $V_{CC}$-0.4 | | $V_{CC}$-0.4 | | 3.1 | V | $I_{OH}$ = -2.0 mA | 8 |
| | | 5.5V | $V_{CC}$-0.4 | | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$ = -2.0 mA | 8 |
| $V_{OL1}$ | Output Low Voltage | 3.0V | | 0.6 | | 0.6 | 0.2 | V | $I_{OL}$ = +4.0 mA | 8 |
| | | 5.5V | | 0.4 | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 8 |
| $V_{OL2}$ | Output Low Voltage | 3.0V | | 1.2 | | 1.2 | 0.3 | V | $I_{OL}$ = +6 mA | 8 |
| | | 5.5V | | 1.2 | | 1.2 | 0.4 | V | $I_{OL}$ = +12 mA | 8 |
| $V_{RH}$ | Reset Input High Voltage | 3.0V | .8 $V_{CC}$ | $V_{CC}$ | .8 $V_{CC}$ | $V_{CC}$ | 1.8 | V | | 13 |
| | | 5.5V | .8 $V_{CC}$ | $V_{CC}$ | .8 $V_{CC}$ | $V_{CC}$ | 2.6 | V | | 13 |
| $V_{RI}$ | Reset Input Low Voltage | 3.0V | GND-0.3 | 0.2 $V_{CC}$ | GND-0.3 | 0.2 $V_{CC}$ | 1.1 | V | | 13 |
| | | 5.5V | GND-0.3 | 0.2 $V_{CC}$ | GND-0.3 | 0.2 $V_{CC}$ | 1.6 | V | | 13 |
| $V_{OLR}$ | Reset Output Low Voltage | 3.0V | | 0.6 | | 0.6 | 0.3 | V | $I_{OL}$ = +1.0 mA | 13 |
| | | 5.5V | | 0.6 | | 0.6 | 0.3 | V | $I_{OL}$ = +1.0 mA | 13 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 3.0V | | 25 | | 25 | 10 | mV | | 10 |
| | | 5.5V | | 25 | | 25 | 10 | mV | | 10 |
| $I_{IL}$ | Input Leakage | 3.0V | -1 | 2 | -1 | 2 | 0.004 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | -1 | 2 | -1 | 2 | 0.004 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 3.0V | -1 | 1 | -1 | 2 | 0.004 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | -1 | 1 | -1 | 2 | 0.004 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| IIR | Reset Input Current | 3.0V | -20 | -130 | -18 | -130 | -60 | µA | | |
| | | 5.5V | -20 | -180 | -18 | -180 | -85 | µA | | |
| $I_{CC}$ | Supply Current | 3.0V | | 20 | | 20 | 7 | mA | @ 16 MHz | 4 |
| | | 5.5V | | 25 | | 25 | 20 | mA | @ 16 MHz | 4 |
| | | 3.0V | | 15 | | 15 | 5 | mA | @ 12 MHz | 4 |
| | | 5.5V | | 20 | | 20 | 15 | mA | @ 12 MHz | 4 |

## AC CHARACTERISTICS (Continued)

| No | Symbol | Parameter | Note [3] $V_{CC}$ | $T_A$=–0°C to 70°C 12 MHz Min | Max | 16 MHz Min | Max | $T_A$ = –40°C to +105°C 12 MHz Min | Max | 16 MHz Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | TdDs(DM) | /DS Rise to DM | 3.0 | 45 | | 35 | | 45 | | 35 | | ns | 2 |
| | | Valid Delay | 5.5 | 45 | | 35 | | 45 | | 35 | | ns | 2 |
| 20 | ThDS(AS) | /DS Valid to Address | 3.0 | 45 | | 35 | | 45 | | 35 | | ns | 2 |
| | | Valid Home Time | 5.5 | 45 | | 35 | | 45 | | 35 | | ns | |

**Notes:**

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The $V_{CC}$ voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the $V_{DD}$ voltage specification of 5.5V guarantees 5.0V ± 0.5V.

**Standard Test Load**

All timing references use 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.

## Additional Timing Diagram

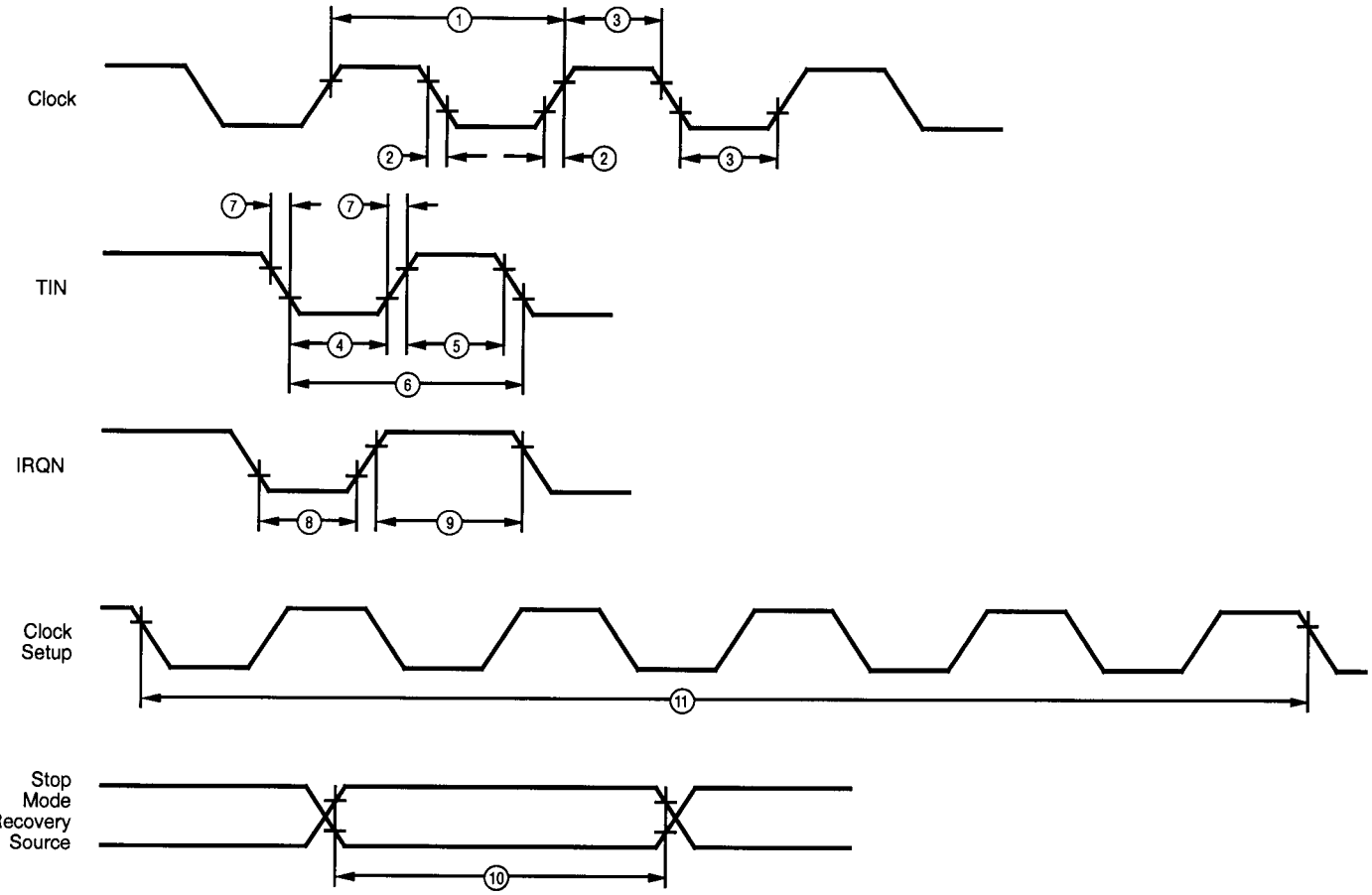



**Figure 9. Additional Timing**

| No | Symbol | Parameter | Note [3] $V_{CC}$ | $T_A$ = 0°C to +70°C 12 MHz Min | 12 MHz Max | 16 MHz Min | 16 MHz Max | $T_A$ =–4 0°C to +105°C 12 MHz Min | 12 MHz Max | 16 MHz Min | 16 MHz Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 13 | TPOR | Power-On Reset Delay | 3.0V | 3 | 24 | 3 | 24 | 3 | 25 | 3 | 25 | ms | |
| | | | 5.5V | 1.5 | 13 | 1.5 | 13 | 1 | 14 | 1 | 14 | ms | |

**Notes: :**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The $V_{CC}$ voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the $V_{DD}$ voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. Standard Oscillator mode, Pcon RegD7=1.
8. Maximum frequency for external XTAL Clock is 4MHz when using low EMI oscillator mode, Pcon Reg D7=0.

## AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

| No | Symbol | Parameter | $V_{CC}$ Note [6] | $T_A$ = 0°C to +70°C 8 MHz Min | Max | $T_A$ = 40°C to +105°C 8 MHz Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| 1 | TpC | Input Clock Period | 3.0V | 250 | DC | 250 | DC | ns | 1,7,8 |
| | | | 5.5V | 250 | DC | 250 | DC | ns | 1,7,8 |
| | | | 3.0V | 125 | DC | 125 | DC | ns | 1,7 |
| | | | 5.5V | 125 | DC | 125 | DC | ns | 1,7 |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.0V | | 25 | | 25 | ns | 1,7 |
| | | | 5.5V | | 25 | | 25 | ns | 1,7 |
| 3 | TwC | Input Clock Width | 3.0V | 125 | | 125 | | ns | 1,7,8 |
| | | | 5.5V | 125 | | 125 | | ns | 1,7,8 |
| | | | 3.0V | 62 | | 62 | | ns | 1,7 |
| | | | 5.5V | 62 | | 62 | | ns | 1,7 |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | ns | 1,7 |
| | | | 5.5V | 70 | | 70 | | ns | 1,7 |
| 5 | TwTinH | Timer Input High Width | 3.0V | 3TpC | | 3TpC | | | 1,7 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1,7 |
| 6 | TpTin | Timer Input Period | 3.0V | 4TpC | | 4TpC | | | 1,7 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1,7 |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Timer | 3.0V | | 100 | | 100 | ns | 1,7 |
| | | | 5.5V | | 100 | | 100 | ns | 1,7 |
| 8A | TwIL | Int. Request Low Time | 3.0V | 100 | | 100 | | ns | 1,2,7 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2,7 |
| 8B | TwIL | Int. Request Low Time | 3.0V | 3TpC | | 3TpC | | | 1,3,7 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1,3,7 |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 3TpC | | 3TpC | | | 1,2,7 |
| | | | 5.5V | 3TpC | | 2TpC | | | 1,2,7 |
| 10 | Twsm | Stop-Mode Recovery Width Spec | 3.0V | 12 | | 12 | | ns | 4 |
| | | | 5.5V | 12 | | 12 | | ns | 4 |
| 11 | Tost | Oscillator Startup Time | 3.0V | | 5TpC | | 5TpC | | 4,9 |
| | | | 5.5V | | 5TpC | | 5TpC | | 4,9 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The $V_{CC}$ voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the $V_{DD}$ voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0.
8. Maximum frequency for external XTAL clock is 4 MHz when using low EMI Oscillator mode Pcon Reg.D7=0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

## AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

| | | | | $T_A$= 0°C to +70°C | | | | $T_A$ = –40°C to +105°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ | 12 MHz | | 16 MHz | | 12 MHz | | 16 MHz | | Direction |
| No | Symbol | Parameter | Note [1] | Min | Max | Min | Max | Min | Max | Min | Max | Data |
| 1 | TsDI(DAV) | Data In Setup Time | 3.0V | 0 | | 0 | | 0 | | 0 | | IN |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | IN |
| 2 | ThDI(RDY) | Data In Hold Time | 3.0V | 0 | | 0 | | 0 | | 0 | | IN |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | IN |
| 3 | TwDAV | Data Available Width | 3.0V | 155 | | 155 | | 155 | | 155 | | IN |
| | | | 5.5V | 110 | | 110 | | 110 | | 110 | | IN |
| 4 | TdDAVI(RDY) | DAV Fall to RDY Fall Delay | 3.0V | | 0 | | 0 | | 0 | | 0 | IN |
| | | | 5.5V | | 0 | | 0 | | 0 | | 0 | IN |
| 5 | TdDAVId(RDY) | DAV Out to DAV Fall Delay | 3.0V | | 120 | | 120 | | 120 | | 120 | IN |
| | | | 5.5V | | 80 | | 80 | | 80 | | 80 | IN |
| 6 | RDY0d(DAV) | RDY Rise to DAV Fall Delay | 3.0V | 0 | | 0 | | 0 | | 0 | | IN |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | IN |
| 7 | TdD0(DAV) | Data Out to DAV Fall Delay | 3.0V | 42 | | 31 | | 42 | | 31 | | OUT |
| | | | 5.5V | 42 | | 31 | | 42 | | 31 | | OUT |
| 8 | TdDAV0(RDY) | DAV Fall to RDY Fall Delay | 3.0V | 0 | | 0 | | 0 | | 0 | | OUT |
| | | | 5.5V | 0 | | 0 | | 0 | | 0 | | OUT |
| 9 | TdRDY0(DAV) | RDY Fall to DAV Rise Delay | 3.0V | | 160 | | 160 | | 160 | | 160 | OUT |
| | | | 5.5V | | 115 | | 115 | | 115 | | 115 | OUT |
| 10 | TwRDY | RDY Width | 3.0V | 110 | | 110 | | 110 | | 110 | | OUT |
| | | | 5.5V | 80 | | 80 | | 80 | | 80 | | OUT |
| 11 | TdRDY0d(DAV) | RDY Rise to DAV Fall Delay | 3.0V | | 110 | | 110 | | 110 | | 110 | OUT |
| | | | 5.5V | | 80 | | 80 | | 80 | | 80 | OUT |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. The $V_{CC}$ voltage specification of 3.0V guarantees 3.3V ± 0.3V and the $V_{DD}$ voltage specification of 5.5V guarantees 5.0V ± 0.5V.

## ROM Mask options available:

1. Enable ROM Protect
2. Enable RAM Protect
3. RC or Crystal Clock Source
4. WDT automatically enabled after reset.
5. Enable autolatches

## PIN FUNCTIONS

**/ROMless** (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90 ROMless Z8. (Note that, when left unconnected or pulled High to $V_{CC}$, the device functions normally as a Z8 ROM version) Not available on Z86C33.

**Note:** When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to $V_{CC}$.

**/DS** (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid. Not available on Z86C33.

**/AS** (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write. Not available on Z86C33.

**XTAL1** Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

**XTAL2** Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

**R//W** (output, write Low). Read/Write, the R//W signal is Low when the Z86C33/43 is writing to the external program or data memory. Not available on Z86C33.

**Port 0** (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03-P00 input/output and P07-P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W (Figure 12).

## PIN FUNCTIONS (Continued)

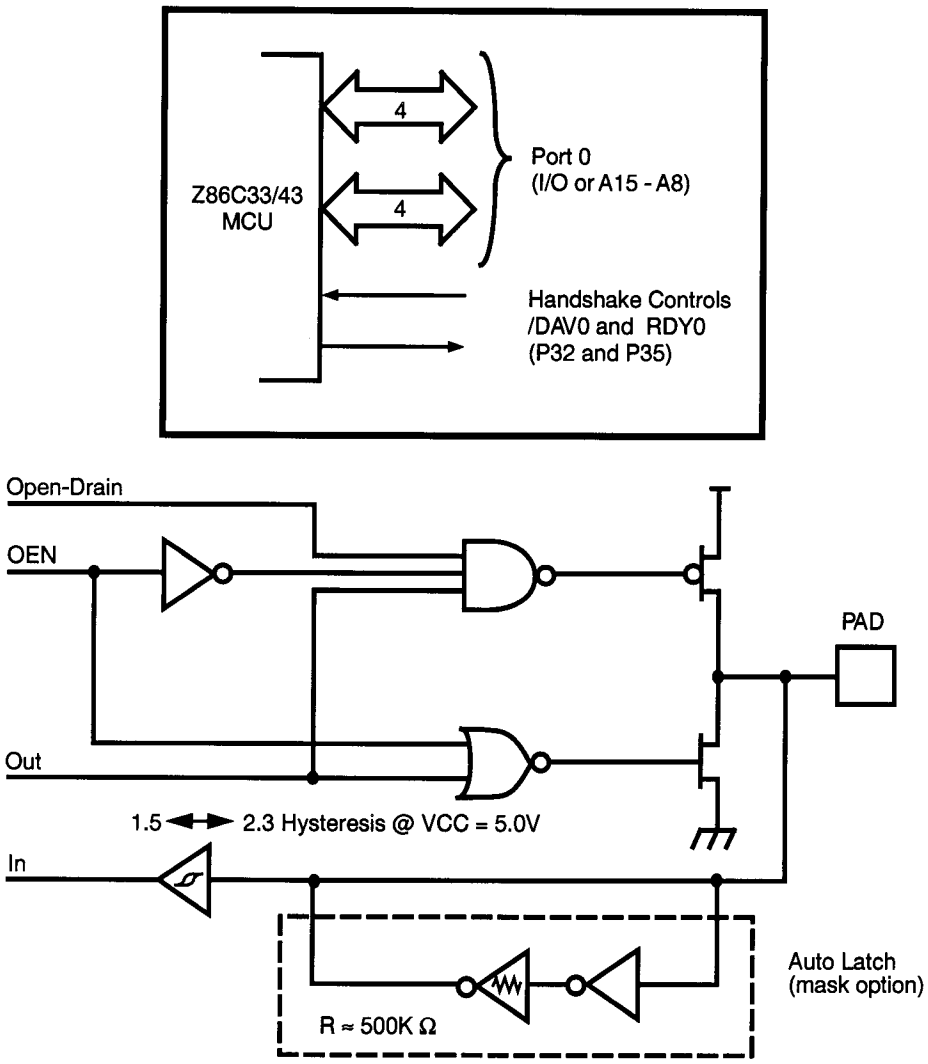



**Figure 12. Port 0 Configuration**

## PIN FUNCTIONS (Continued)

**Port 2** (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 2 may be placed under handshake control. In this Handshake Mode, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 14).

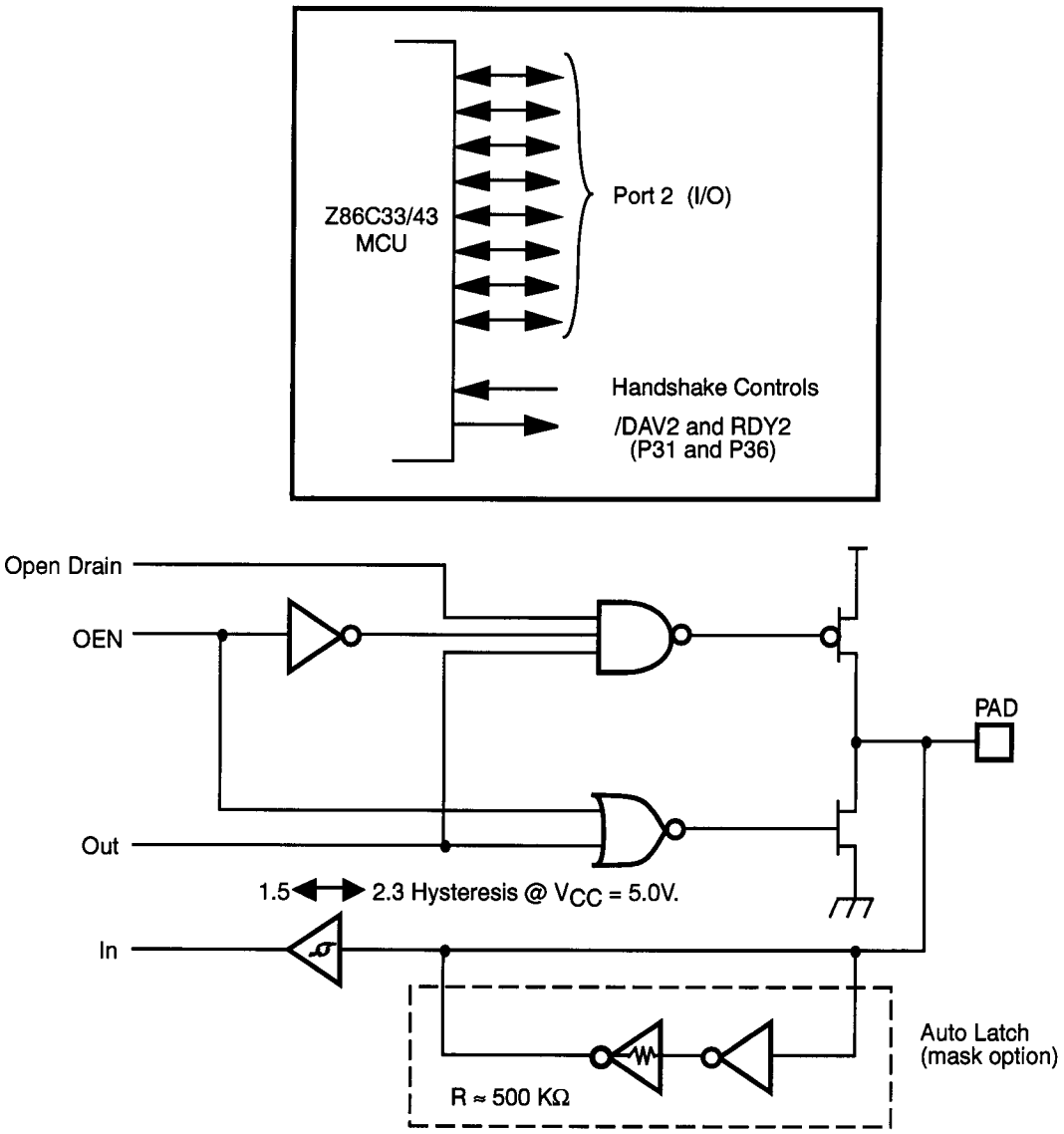



**Figure 14. Port 2 Configuration**

## PIN FUNCTIONS (Continued)

**/RESET** (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. RESET does depend on oscillator operating to achieve full reset conditions except a permanently enabled WDT reset.** Pull-up is provided internally.

**Note:** /RESET pin is not available on Z86C33.

After the POR time, /RESET is a Schmitt-triggered input. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000C (HEX), after the RST is released. For Power-On Reset, the reset output time is TPOR ms.

Once program execution begins, /AS and /DS toggles only for external memory accesses. The Z86C33/43 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a Stop-Mode Recovery operation or from a WDT reset out of STOP Mode.

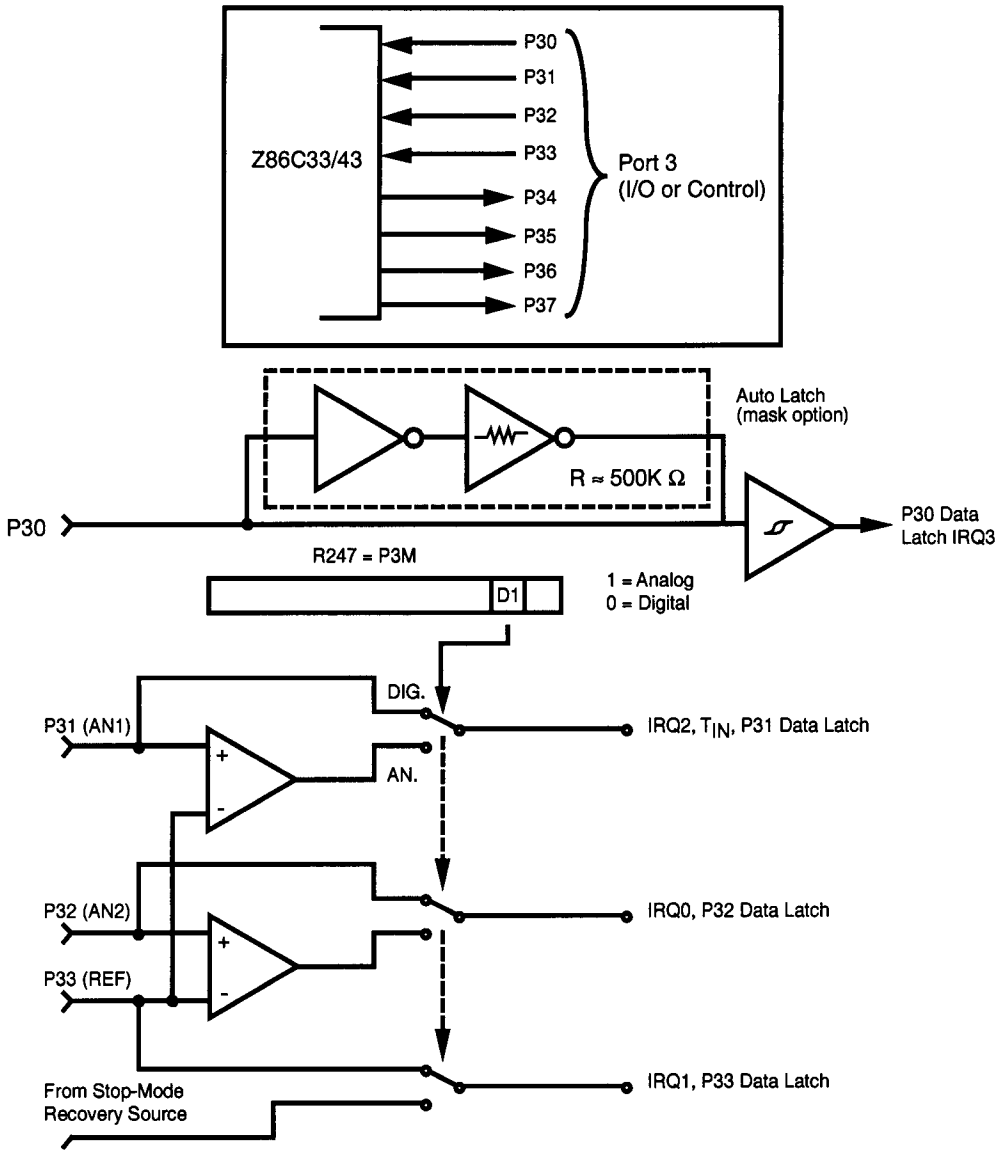



**Figure 15. Port 3 Configuration**

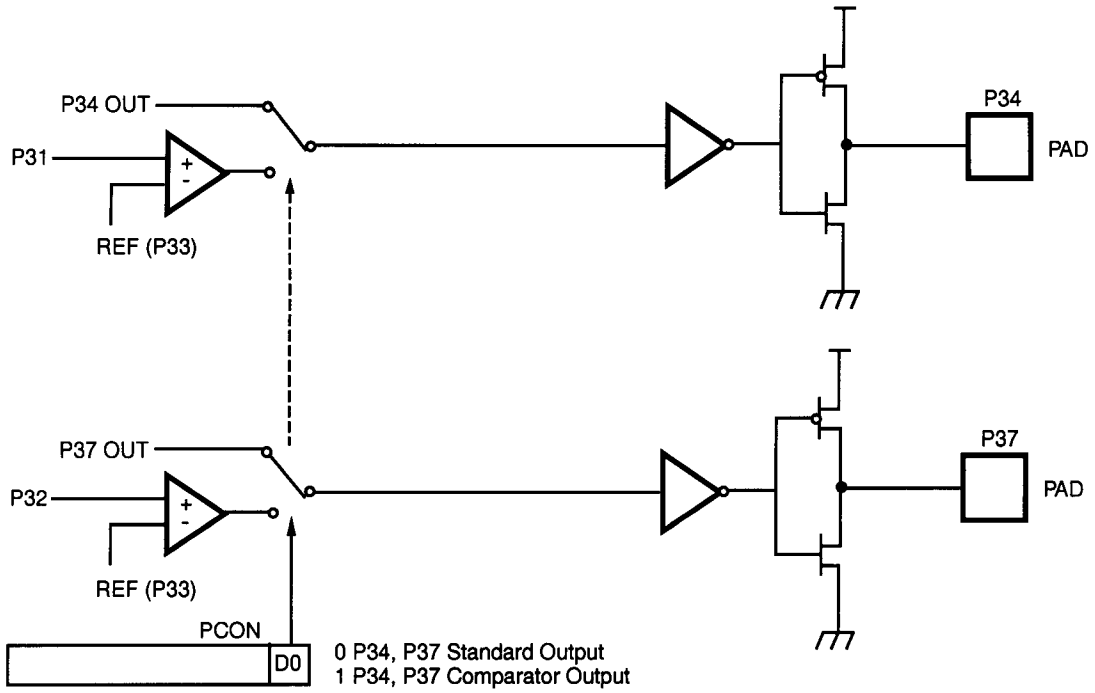



**Figure 16. Port 3 Configuration**

## FUNCTIONAL DESCRIPTION (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z86C33/43 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin. When in analog mode, the IRQ1 is generated by the Stop-Mode Recovery source selected by SMR Reg. bits D4,D3,D2, or SMR2 D1or D0.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 7.

**Table 7. IRQ Register**

| IRQ | | Interrupt Edge | |
|---|---|---|---|
| D7 | D6 | P31 | P32 |
| 0 | 0 | F | F |
| 0 | 1 | F | R |
| 1 | 0 | R | F |
| 1 | 1 | R/F | R/F |

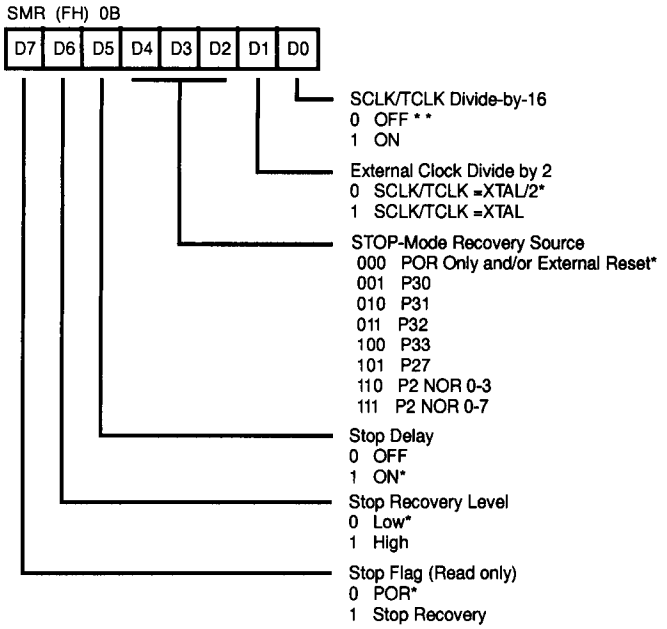
**Notes:**
F = Falling Edge
R = Rising Edge

**Clock.** The Z86C33/43 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when counting from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator. The RC oscillator option is mask-programmable on the Z86C33/43 and is selected by the customer at the time when the ROM code is submitted. (Note that the RC option is available up to 8 MHz.) The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 24).

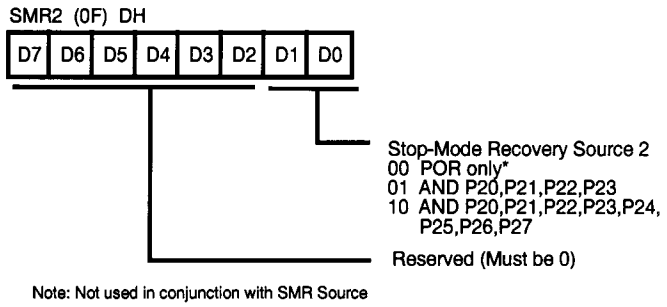
**Note:** For better noise immunity, the capacitors should be tied directly to the device Ground pin ($V_{SS}$).

## FUNCTIONAL DESCRIPTION (Continued)




Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

**Figure 26. Stop-Mode Recovery Register (Write Only Except Bit D&, Which Is Read Only)**




Note: Not used in conjunction with SMR Source

**Figure 27. Stop-Mode Recovery Register 2 (0F) DH: Write Only)**

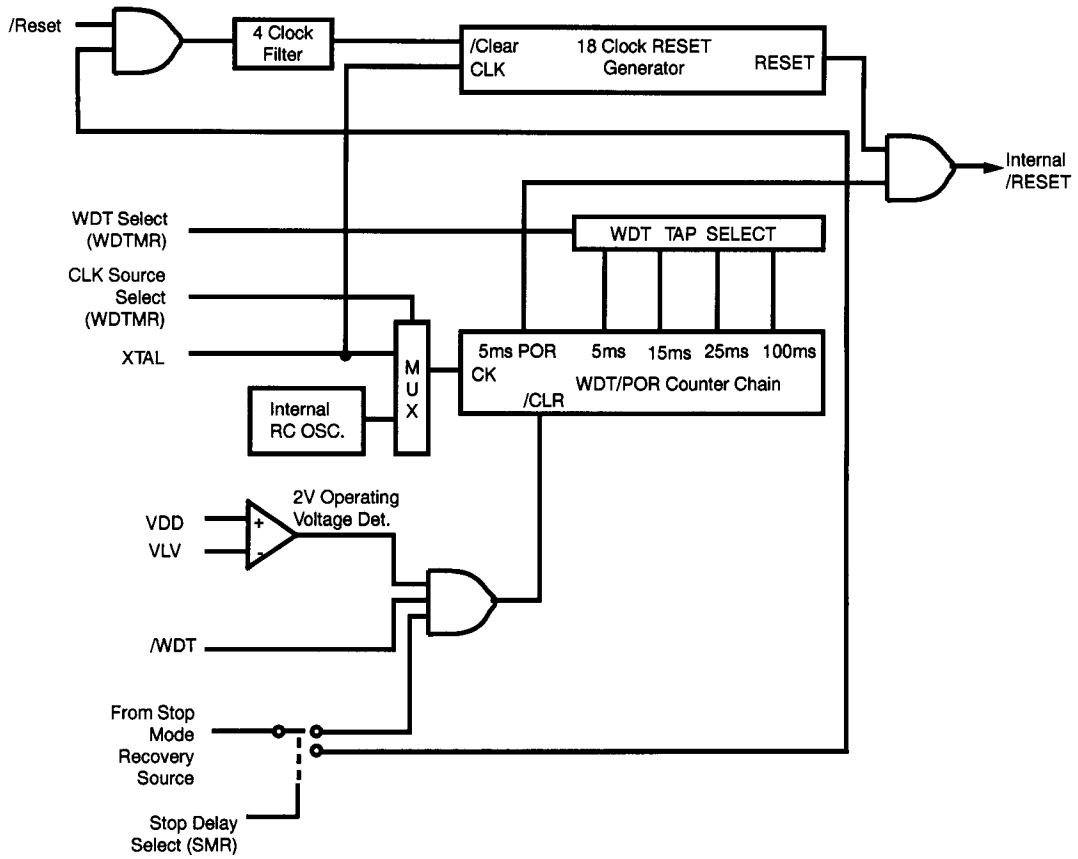



**Figure 30. Resets and WDT**

## FUNCTIONAL DESCRIPTION (Continued)

**WDT Time Select. (D0,D1).** Selects the WDT time period and is configured as shown in Table 10.

**Table 10. WDT Time Select**

| D1 | D0 | Timeout of Internal RC OSC | Timeout of System Clock |
|---|---|---|---|
| 0 | 0 | 3.5 ms min | 128 SCLK |
| 0 | 1 | 7 ms min | 256 SCLK |
| 1 | 0 | 14 ms min | 512 SCLK |
| 1 | 1 | 56 ms min | 2048 SCLK |

**Notes:**
SCLK = system bus clock cycle
The default on reset is 15 ms.
Values given are for $V_{CC}$ = 5.0V.

**WDTMR During HALT (D2).** This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

**WDTMR During STOP (D3).** This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

**Note:** If permanent WDT is selected, the WDT will run in all modes and can not be stopped or disabled if the on board RC oscillator is selected as the clock source for WDT.

**Clock Source for WDT (D4).** This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the Internal RC oscillator.

**WDTMR Register Accessibility.** The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, watch dog reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH (Figure 30).

**Note:** The WDT can be permanently enabled (automatically enabled after reset) through a mask programming option. The option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP Modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

**Low Voltage Protection.** An on-board Voltage Comparator checks that $V_{CC}$ is at the required level to ensure correct operation of the device. Reset is globally driven if $V_{CC}$ is below the specified voltage (Low Voltage Protection ). The minimum operating voltage is varying with the temperature and operating frequency, while the Low Voltage Protection ($V_{LV}$) varies with temperature only.

The Low Voltage Protection trip voltage ($V_{LV}$) is less than 3V and above 1.4V under the following conditions.

Maximum ($V_{LV}$) Conditions:

**Case 1:** TA = –40°C, +105°C, Internal Clock Frequency equal or less than 4 MHz

**Case 2:** TA = –40°C, +85°C, Internal Clock Frequency equal or less than 6 MHz

**Note:** The internal clock frequency relationship to the XTAL clock is dependent on SMR Bit 0 1 setting.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point ($V_{LV}$) is reached, for the temperatures and operating frequencies in Case 1 and Case 2, above. The device is guaranteed to function normally at supply voltages above the Low Voltage Protection trip point. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 32).

## Z8 CONTROL REGISTERS

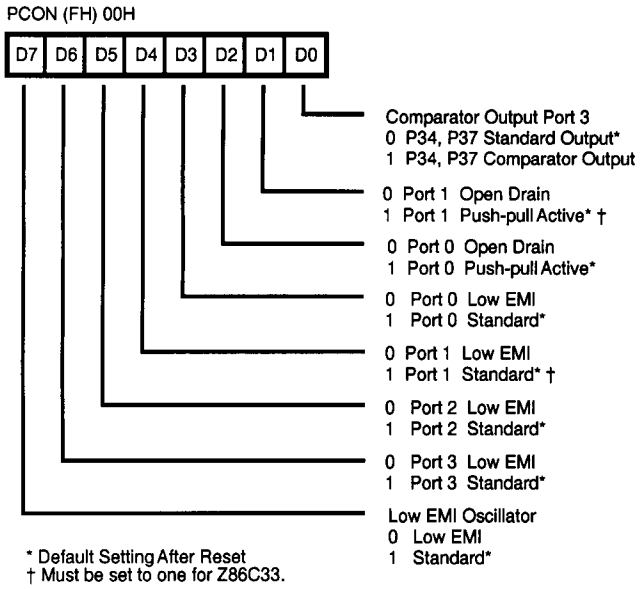



**Figure 35. Port Configuration Register (PCON) (Write Only)**

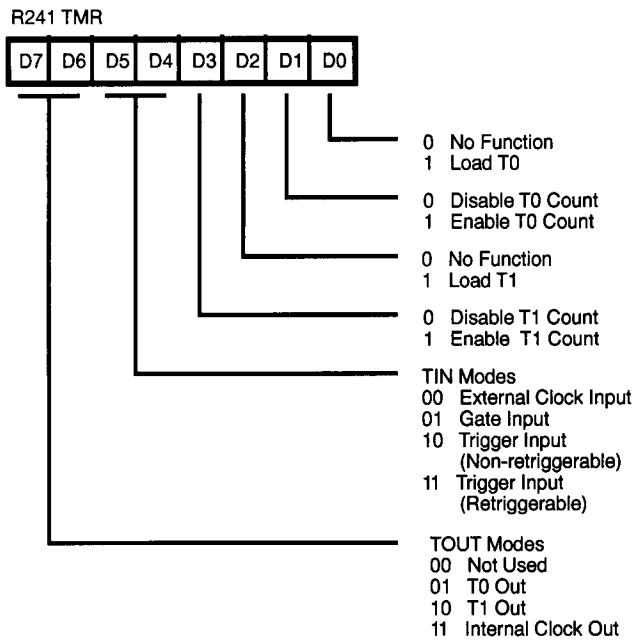



**Figure 36. Timer Mode Register ($F1_H$: Read/Write)**

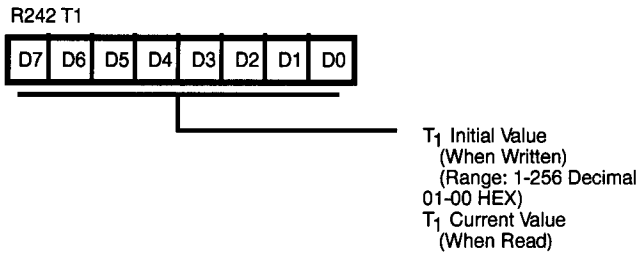



**Figure 37. Counter/Timer 1 Register ($F2_H$: Read/Write)**

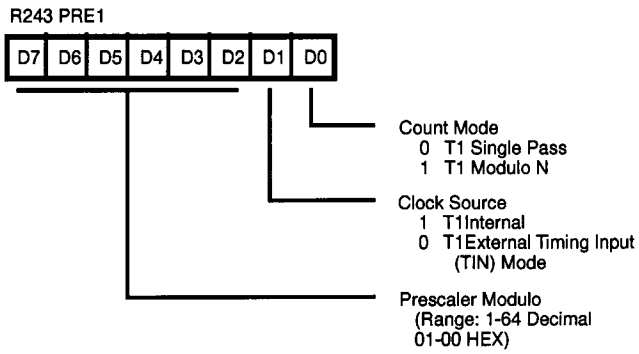



**Figure 38. Prescaler 1 Register ($F3_H$: Write Only)**

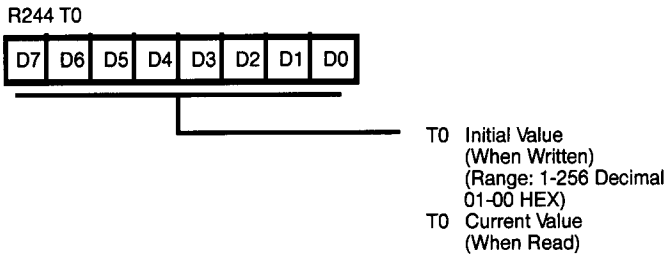



**Figure 39. Counter/Timer 0 Register ($F4_H$: Read/Write)**

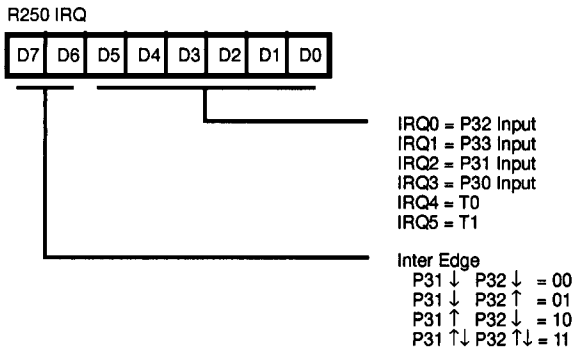



**Figure 45. Interrupt Request Register ($FA_H$: Read/Write)**

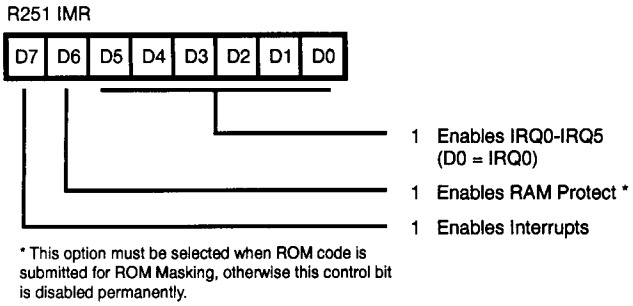



**Figure 46. Interrupt Mask Register ($FB_H$: Read/Write)**

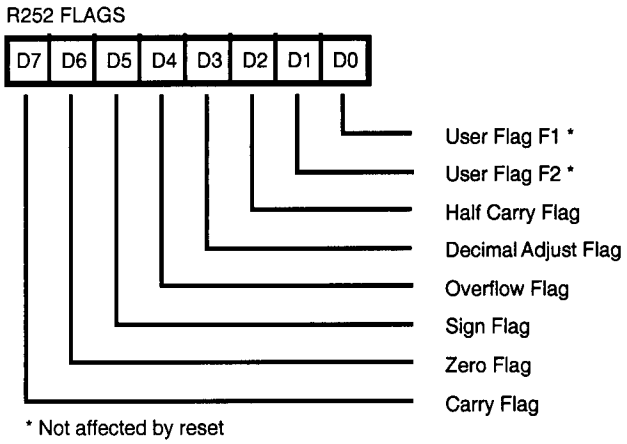



**Figure 47. Flag Register ($FC_H$: Read/Write)**

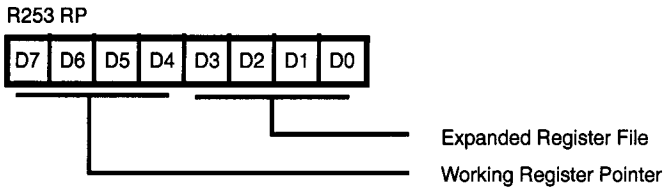



**Figure 48. Register Pointer ($FD_H$: Read/Write)**

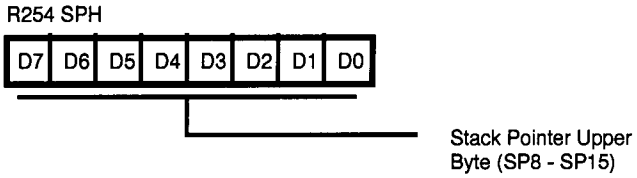



**Figure 49. Stack Pointer High ($FE_H$: Read/Write)**

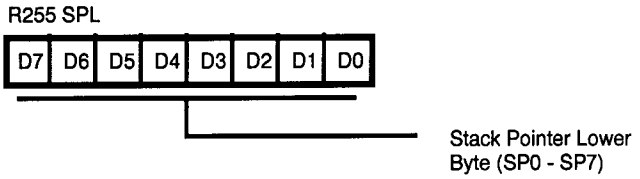



**Figure 50. Stack Pointer Low ($FF_H$: Read/Write)**

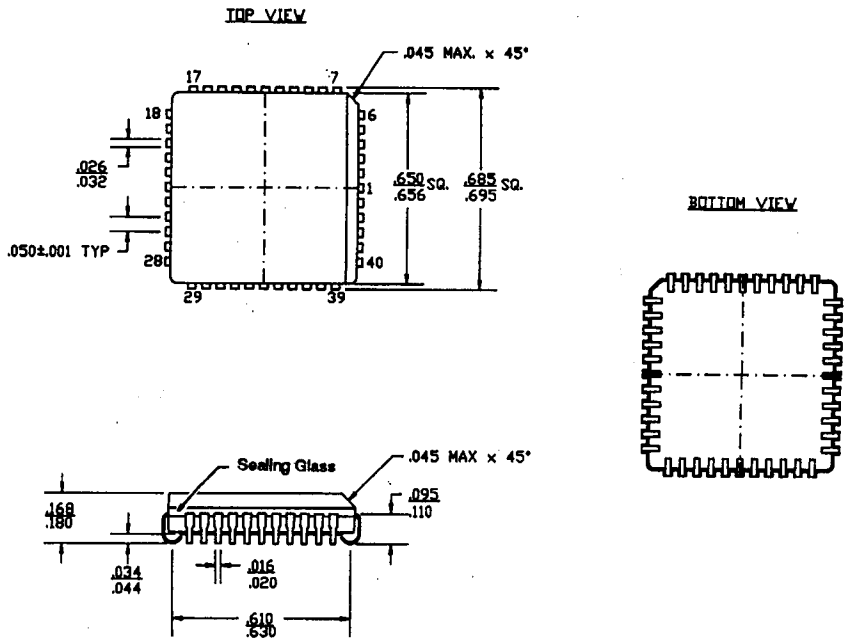



Figure 55. 44-Pin LQFP Package Diagram