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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c3312pscr2130

PIN DESCRIPTION (Continued)

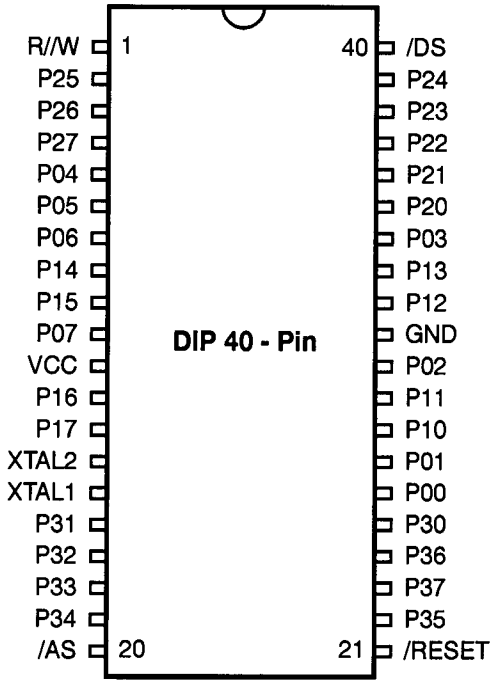


Figure 4. 40-Pin DIP Assignments

Table 2. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output
8-9	P14-15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output
15	XTAL1	Crystal, Oscillator Clock	Input
16-18	P31-33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output

Table 2. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-01	Port 0, Pin 0,1	In/Output
28-29	P10-11	Port 1, Pin 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-13	Port 1, Pin 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

PIN DESCRIPTION (Continued)

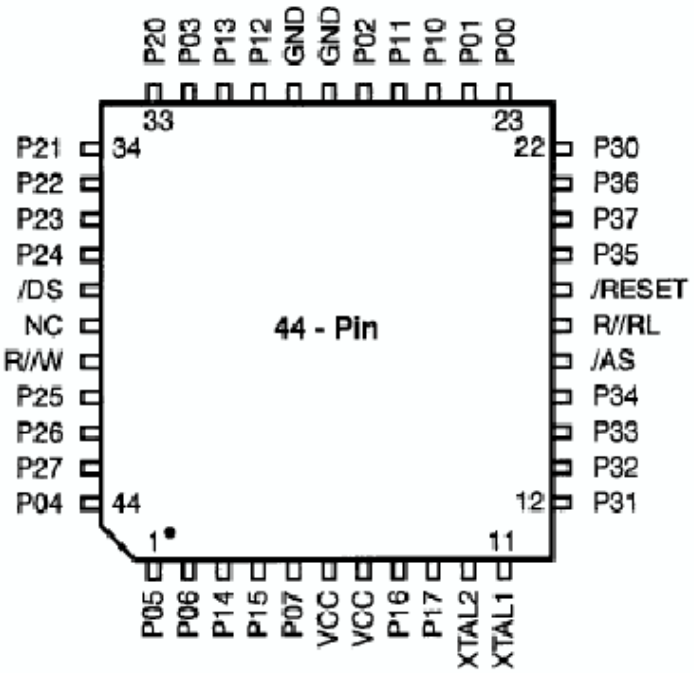


Figure 6. 44-Pin LQFP Pin Assignments

Table 4. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output
3-4	P14-15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	V_{CC}	Power Supply	
8-9	P16-17	Port 1 Pins 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless Control	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output

Table 4. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-01	Port 0, Pins 0,1	In/Output
25-26	P10-11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	N/C	Not Connected	
40	R//W	Read/Write	Output
41-43	P25-27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:

1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA
3. This excludes XTAL pins.
4. Device pin is not atan output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH} \,] + \text{sum of } (V_{0L} \times I_{0L})$$

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	0.7	10	3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	1.4	15	1.4	20	5	µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.0V	-0.6	-5	-0.6	-7	-3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-8	-1.0	-10	-6	µA	$0V < V_{IN} < V_{CC}$	9
V_{LV}	V_{CC} Low Voltage Protection Voltage				2.0	3.3	2.8	V	4 MHz max Int. CLK Freq.	7,15
			2.2	3.1			2.8		6 MHz max Int. CLK Freq.	7,14
V_{OH}	Output High Voltage (Low EMI Mode)	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -0.5 mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.0V		0.6		0.6	0.2	V	I_{OL} = 1.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = 1.0 mA	

Notes:

1. Typicals are at V_{CC} = 5.0V and 3.3V.
2. GND = 0V.
3. The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC}=3.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC}-5.0V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 10 pF.
6. Same as note [4] except inputs at V_{CC}.
7. The V_{LV} voltage increases as the temperature decreases and will overlap lower V_{CC} operating region.
8. Standard Mode (not Low EMI).
9. Auto Latch (Mask Option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Z86C43 only.
14. 0°C to 70°C (standard temperature).
15. –40°C to 150°C (extended temperature).

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	Note [3] V_{CC}	T_A=–0°C to 70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = –40°C to +105°C 12 MHz Min	Max	16 MHz Min	Max	Units	Notes
19	TdDs(DM)	/DS Rise to DM	3.0	45		35		45		35		ns	2
		Valid Delay	5.5	45		35		45		35		ns	2
20	ThDS(AS)	/DS Valid to Address	3.0	45		35		45		35		ns	2
		Valid Home Time	5.5	45		35		45		35		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3]	T_A = 0°C to +70°C				T_A =–4 0°C to +105°C					
				12 MHz		16 MHz		12 MHz		16 MHz			
			V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1,7
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1,7
			3.0V	250	DC	250	DC	250	DC	250	DC	ns	1,8
			5.5V	250	DC	250	DC	250	DC	250	DC	ns	1,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
			3.0V	125		125		125		125		ns	1,8
			5.5V	125		125		125		125		ns	1,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		4
			5.5V		5TpC		5TpC		5TpC		5TpC		4

No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	D1, D0 [Note]
12	Twdt	Watch-Dog Timer Delay Time before time-out	3.0V	7		7		7		7		ms	0, 0 [5]
			5.5V	3.5		3.5		3.5		3.5		ms	0, 0 [5]
			3.0V	14		14		14		14		ms	0, 1 [5]
			5.5V	7		7		7		7		ms	0, 1 [5]
			3.0V	28		28		28		28		ms	1, 0 [5]
			5.5V	14		14		14		14		ms	1, 0 [5]
			3.0V	112		112		112		112		ms	1, 1 [5]
			5.5V	56		56		56		56		ms	1, 1 [5]

PIN FUNCTIONS

/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version) Not available on Z86C33.

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid. Not available on Z86C33.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write. Not available on Z86C33.

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W (output, write Low). Read/Write, the R//W signal is Low when the Z86C33/43 is writing to the external program or data memory. Not available on Z86C33.

Port 0 (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03-P00 input/output and P07-P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W (Figure 12).

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 2 may be placed under handshake control. In this Handshake Mode, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 14).

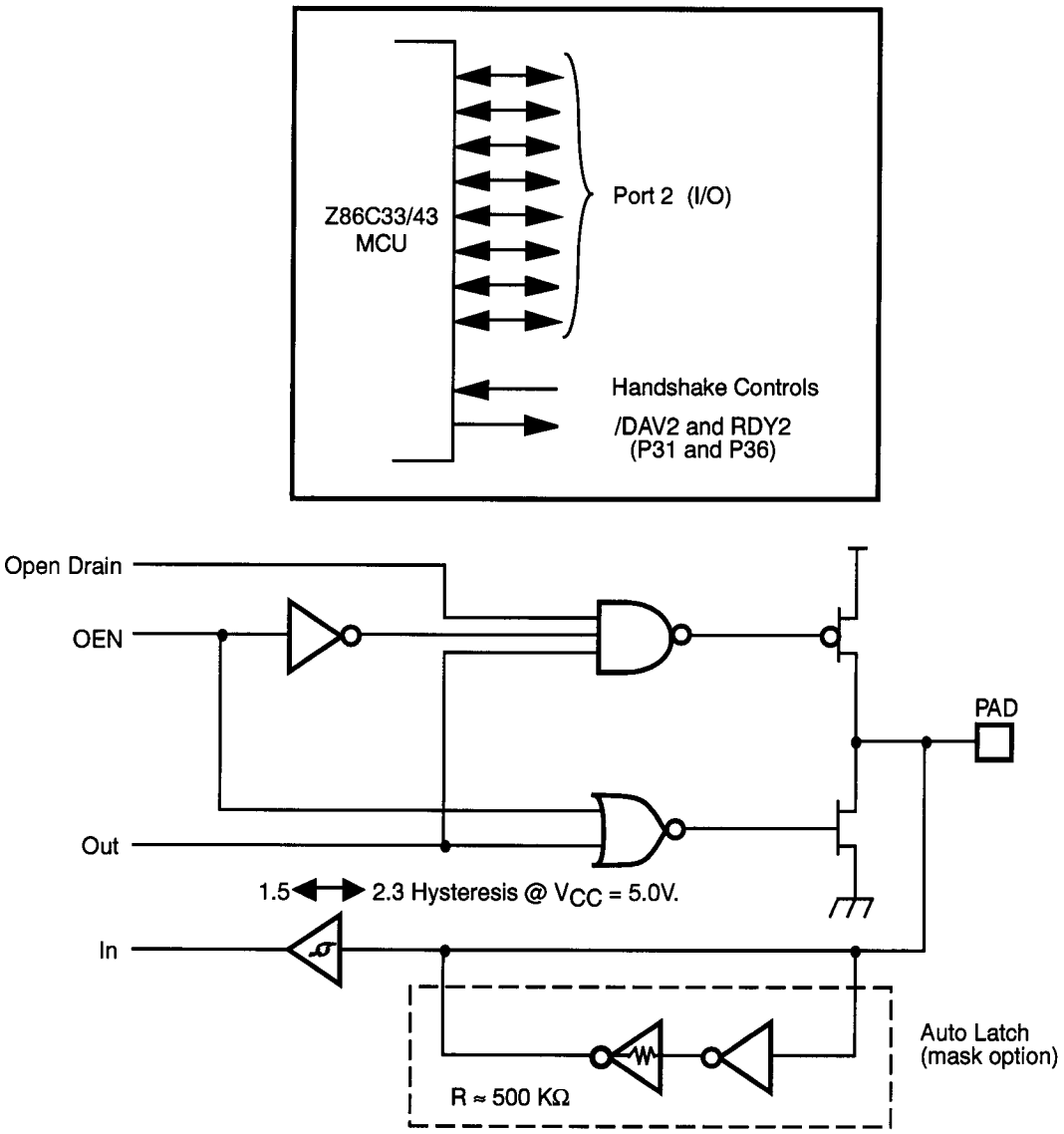


Figure 14. Port 2 Configuration

PIN FUNCTIONS (Continued)

/RESET (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. RESET does depend on oscillator operating to achieve full reset conditions except a permanently enabled WDT reset.** Pull-up is provided internally.

Note: /RESET pin is not available on Z86C33.

After the POR time, /RESET is a Schmitt-triggered input. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000C (HEX), after the RST is released. For Power-On Reset, the reset output time is TPOR ms.

Once program execution begins, /AS and /DS toggles only for external memory accesses. The Z86C33/43 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a Stop-Mode Recovery operation or from a WDT reset out of STOP Mode.

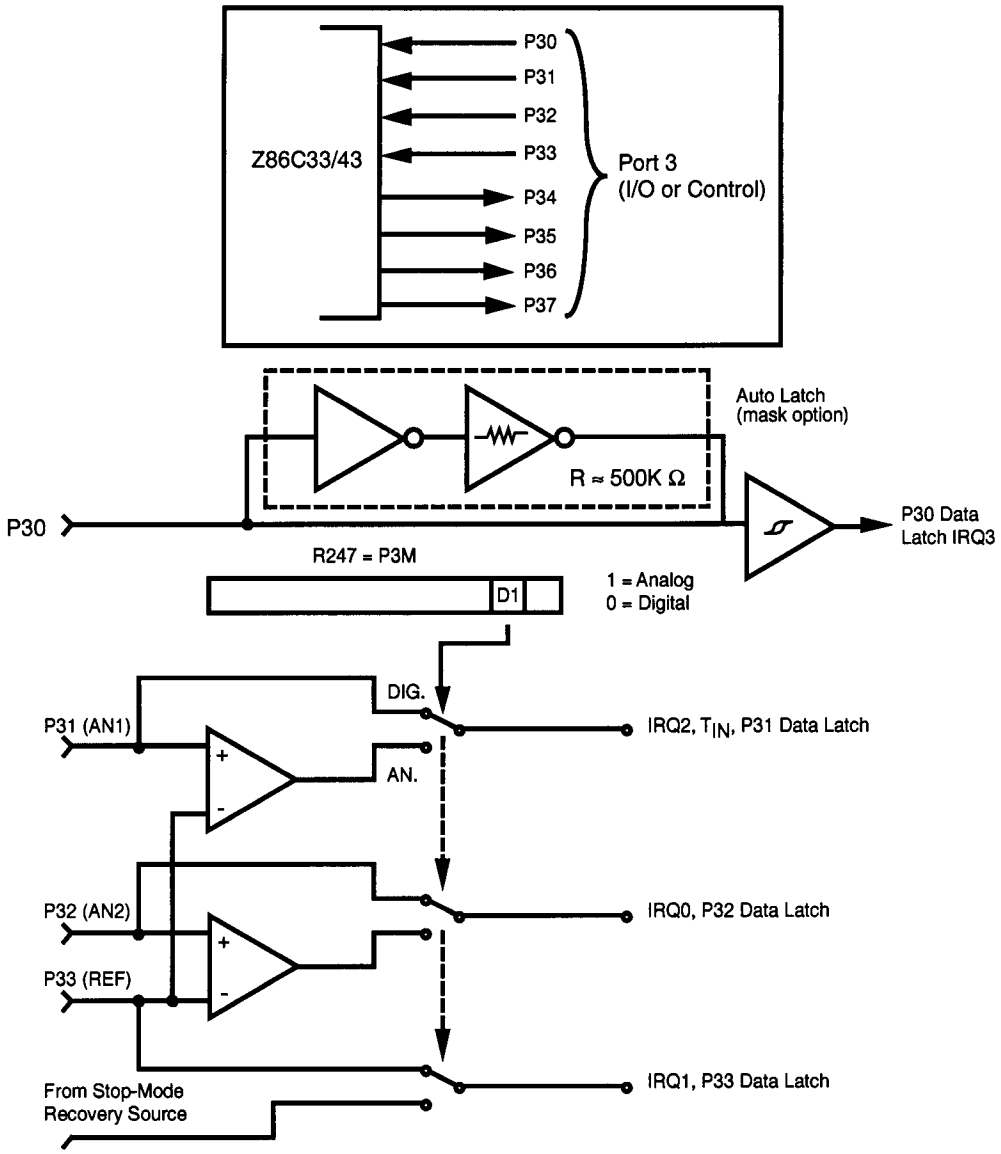


Figure 15. Port 3 Configuration

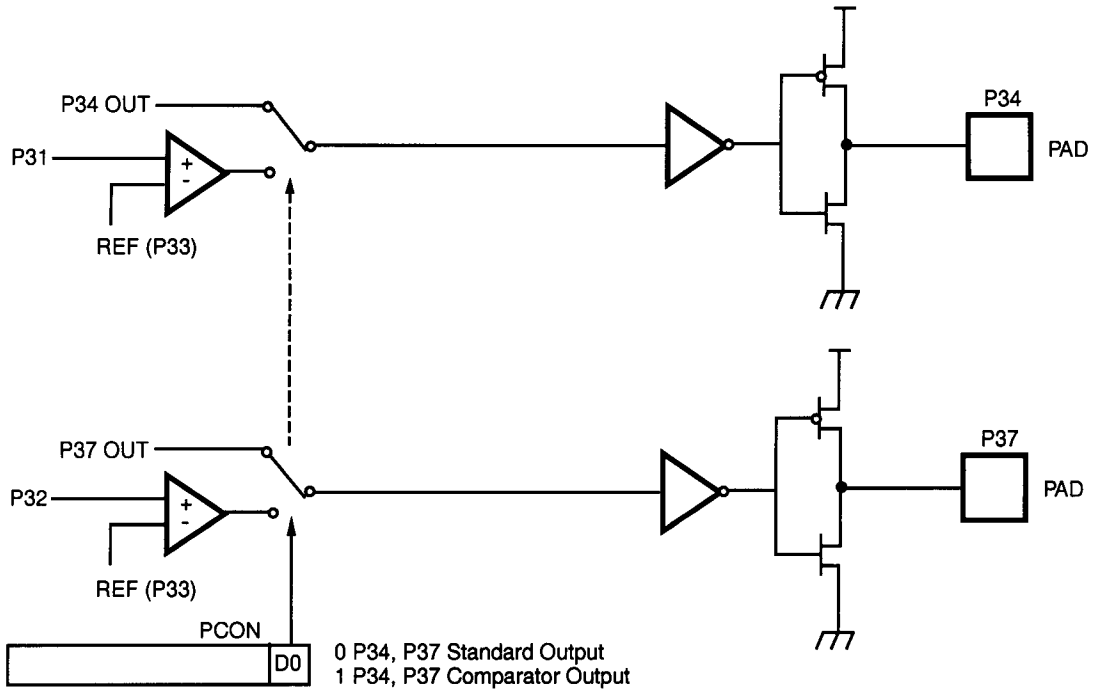


Figure 16. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86C33/43 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset
- Low Voltage Recovery

Auto Power-On Reset circuitry is built into the Z86C33/43, eliminating the need for an external reset circuit to reset upon power-up. The internal pull-up resistor is on the Reset pin, so a pull-up resistor is not required; however, in high EMI (noisy) environment, it is recommended that a small value pull-up resistor be used.

Note: /RESET pin is not available on Z86C33.

Program Memory. The Z86C33/43 addresses up to 4 KB of internal program memory and 60 KB of external memory (Figure 18). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, address 12 to address 4095 consists of on-chip mask-programmed ROM. At addresses 4096 and greater, the Z86C33/43 executes external program memory fetches through Port 0 and Port 1 in Address/Data mode.

The 4 KB program memory is mask programmable. **A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in external program mode. ROM look-up tables can be used with this feature.**

The ROM Protect option is mask-programmable, to be selected by the customer when the ROM code is submitted.

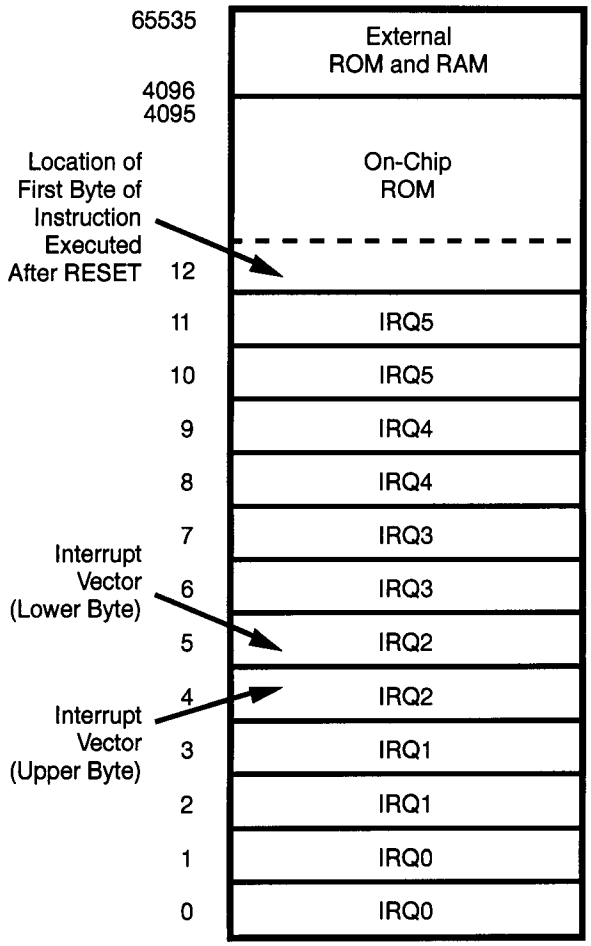


Figure 17. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Data Memory (/DM). The Z86C33/43 ROM version can address up to 60 KB of external data memory beginning at location 4096. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 19). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode. Available only on Z86C43.

Expanded Register File (ERF). The Z86C33/43 register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group (Figure 18). These register groups are known as the Expanded Register File (ERF). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 18). Three system configuration registers reside in the Expanded Register File at Bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented, and is open for future expansion.

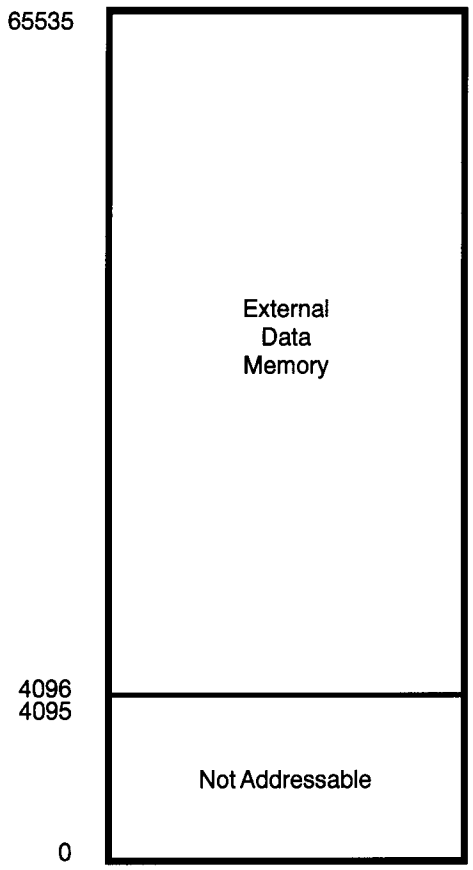
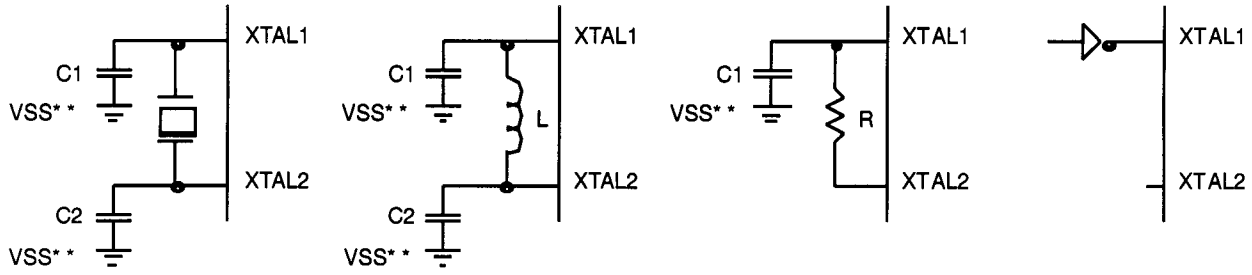


Figure 18. Data Memory Map



Ceramic Resonator or Crystal
C1, C2 = 22 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 uH *
f = 3 MHz *

RC
@ 5V VCC (TYP)

C1 = 44 pF *
R = 1.90K *
f = 6 MHz *

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 24. Oscillator Configuration

Power-On-Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR=1).
3. WDT time-out.

The POR time is a specified as TPOR. Bit 5 of the STOP-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be enabled and executed to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

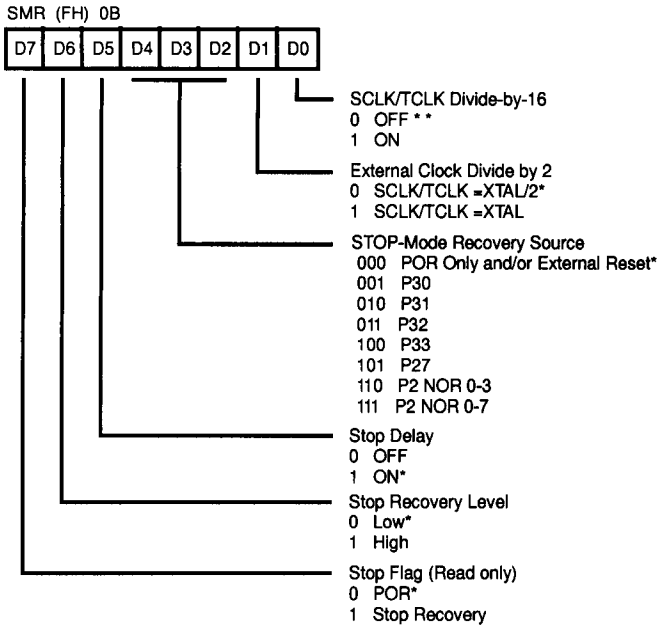
```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP Mode
               or
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT Mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. It also reduces the standby current to 10 µA or less. The STOP Mode is terminated by a reset only, either by WDT time-out, POR, SMR recovery, or external reset. This causes the processor to restart the application program at address 000C (HEX).A WDT time out in STOP Mode will affect all registers the same as if a Stop-Mode Recovery occurred via a selected Stop-Mode Recovery source except that the POR delay is enabled even if the delay is selected for disable.

Note: If permanent WDT is selected, the WDT will run in all modes and can not be stopped or disabled if on board RC oscillator is selected to drive the WDT.

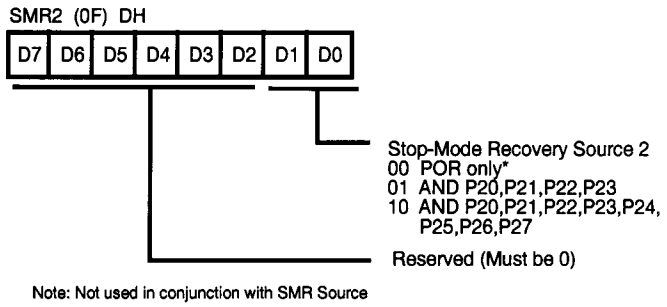
Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 25).

FUNCTIONAL DESCRIPTION (Continued)



Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 26. Stop-Mode Recovery Register (Write Only Except Bit D&, Which Is Read Only)



Note: Not used in conjunction with SMR Source

Figure 27. Stop-Mode Recovery Register 2 (0F) DH: Write Only)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 4 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 28 and Table 8). When the STOP-Mode Recovery Sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.

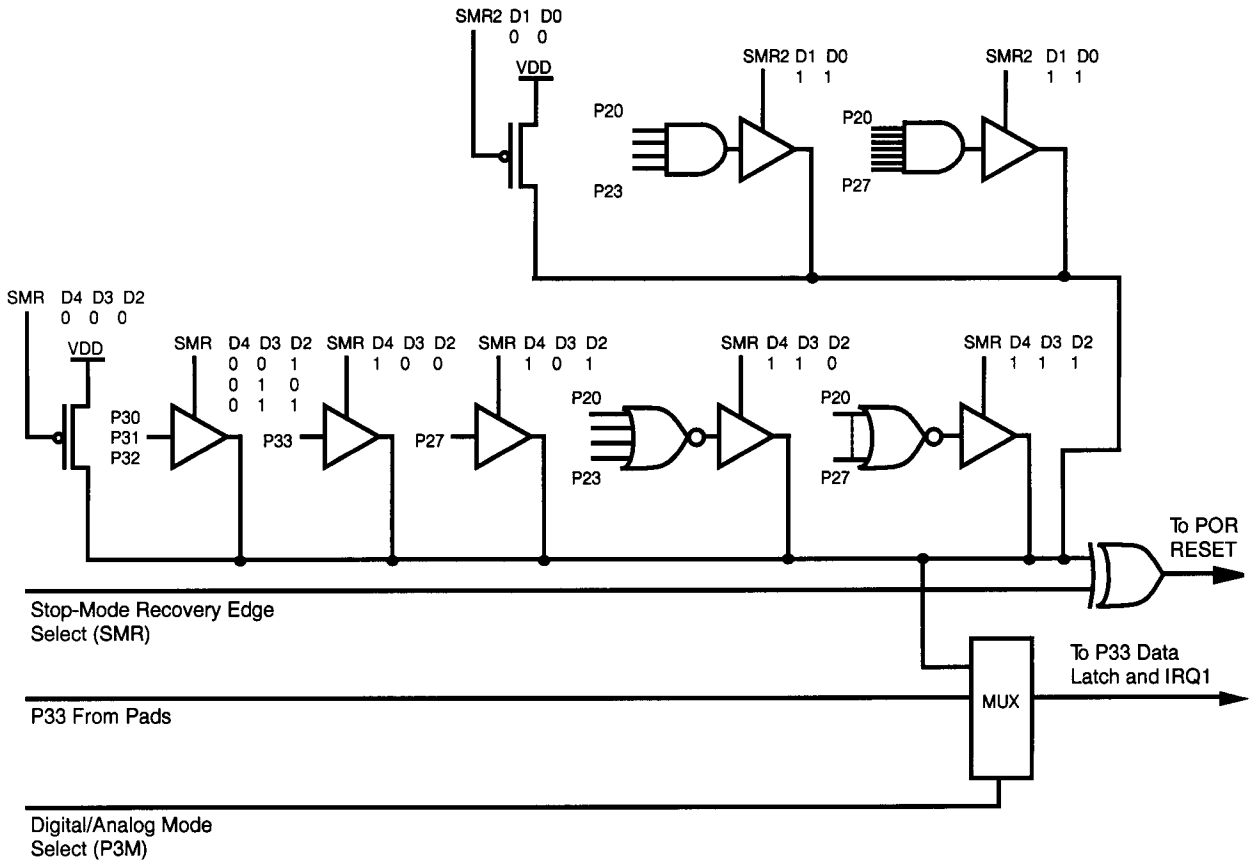


Figure 28. Stop-Mode Recovery Source

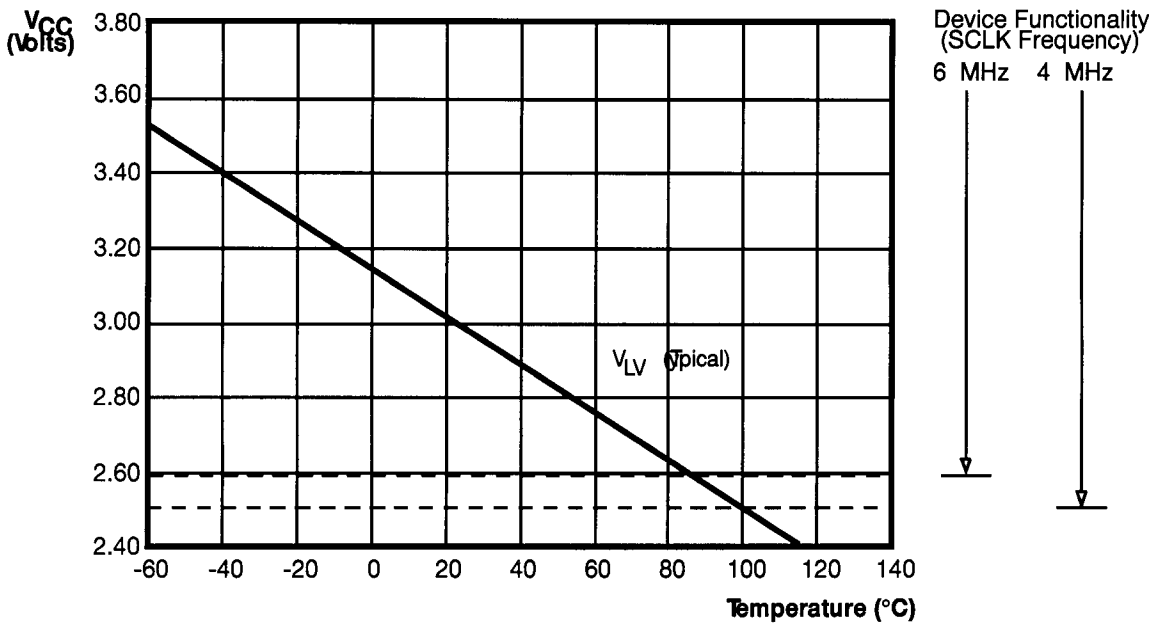
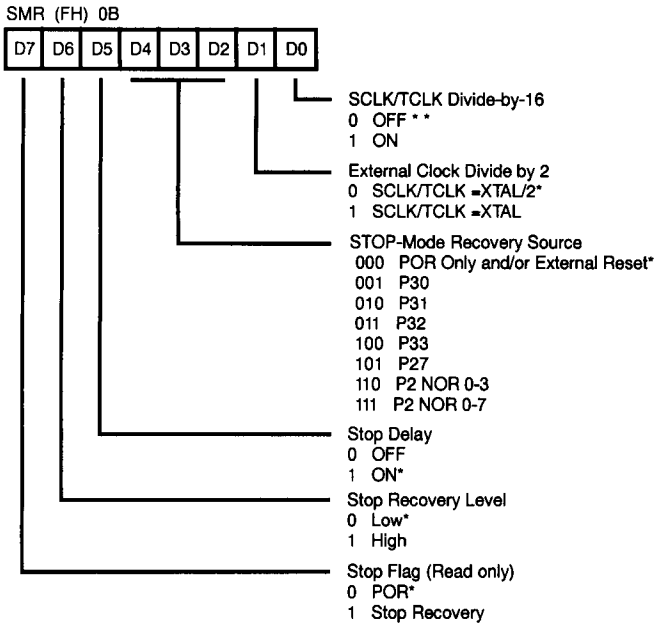


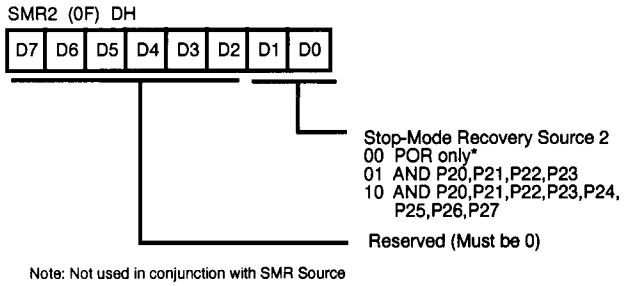
Figure 31. Typical Z86C33/43 Low Voltage Protection vs Temperature

EXPANDED REGISTER FILE CONTROL REGISTERS



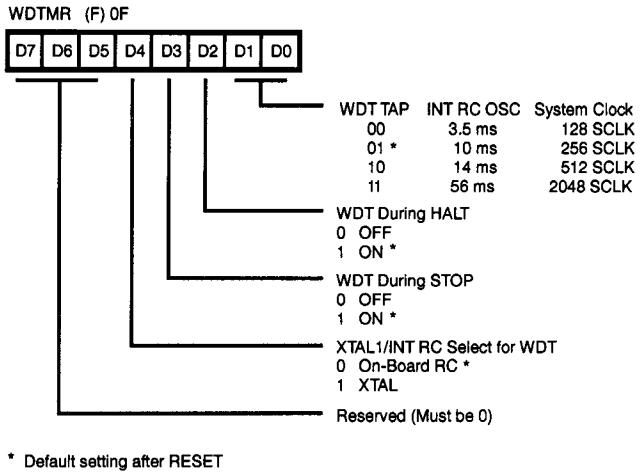
Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 32. Stop-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only)



Note: Not used in conjunction with SMR Source

Figure 33. Stop-Mode Recovery Register2



* Default setting after RESET

Figure 34. Watch-Dog Timer Mode Register (Write Only)

Z8 CONTROL REGISTERS

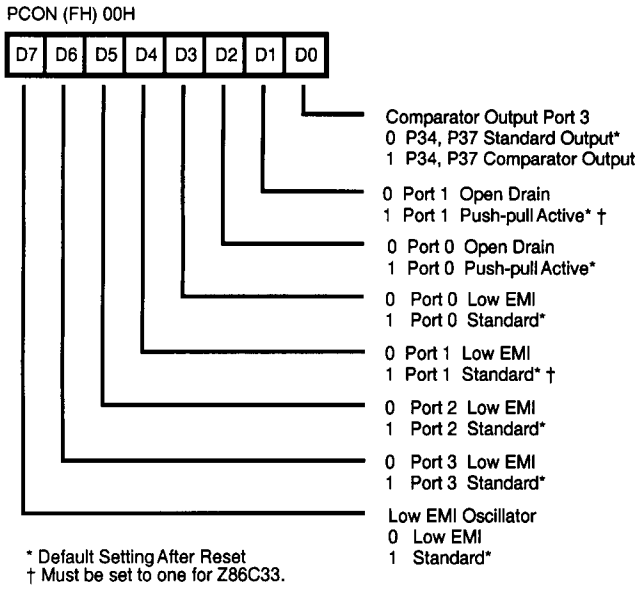


Figure 35. Port Configuration Register (PCON) (Write Only)

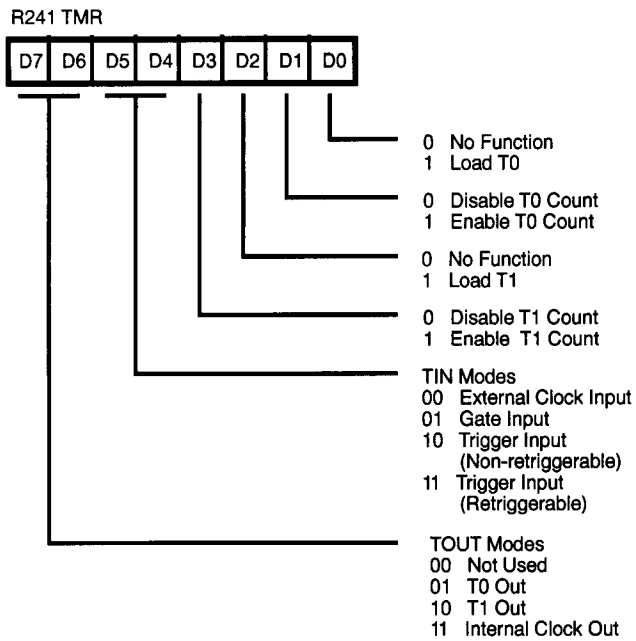


Figure 36. Timer Mode Register ($F1_H$: Read/Write)

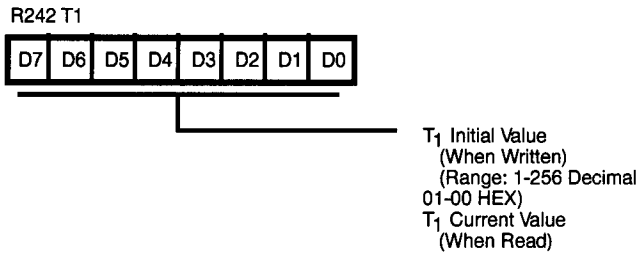


Figure 37. Counter/Timer 1 Register ($F2_H$: Read/Write)

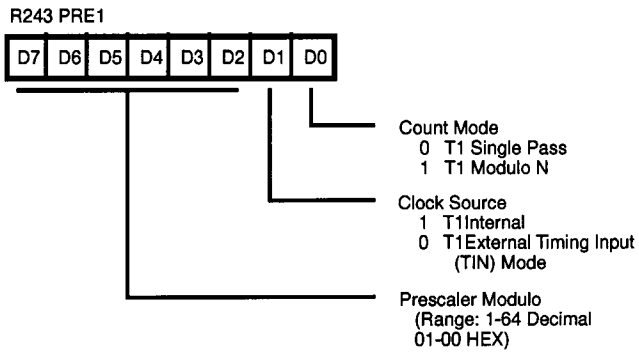


Figure 38. Prescaler 1 Register ($F3_H$: Write Only)

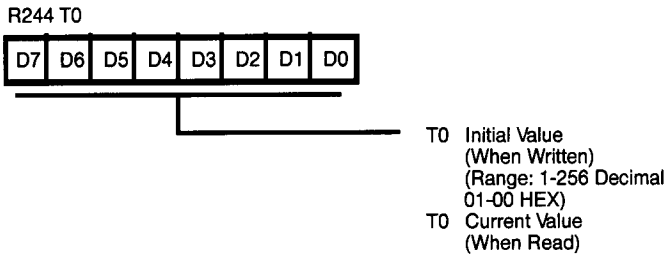


Figure 39. Counter/Timer 0 Register ($F4_H$: Read/Write)

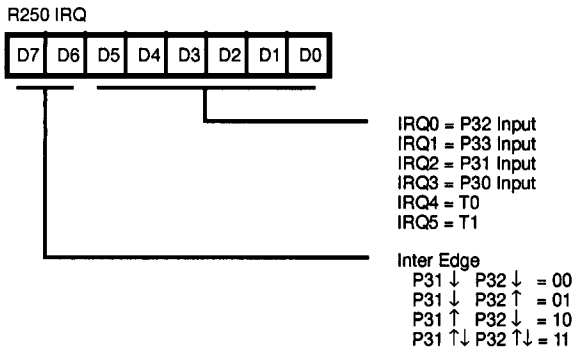


Figure 45. Interrupt Request Register (FA_H: Read/Write)

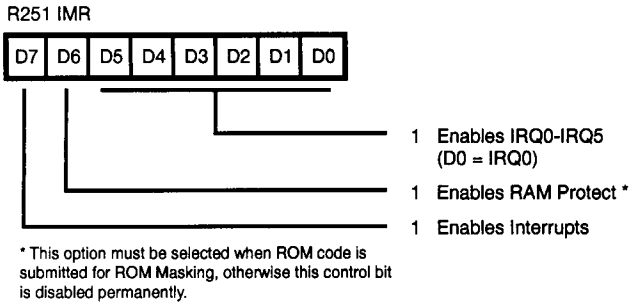


Figure 46. Interrupt Mask Register (FB_H: Read/Write)

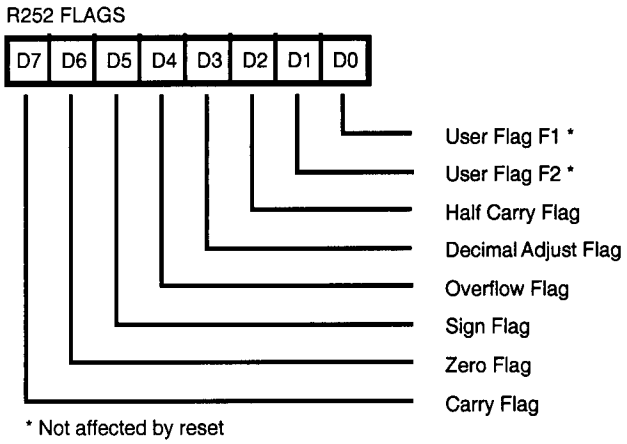


Figure 47. Flag Register (FC_H: Read/Write)

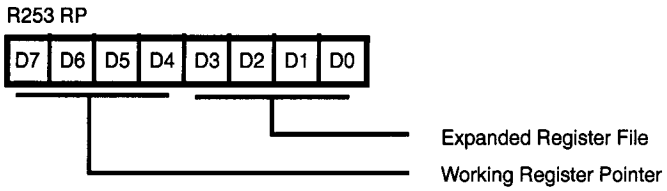


Figure 48. Register Pointer (FD_H: Read/Write)

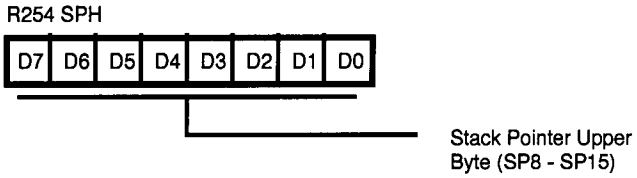


Figure 49. Stack Pointer High (FE_H: Read/Write)

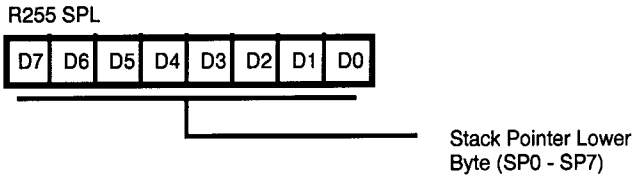
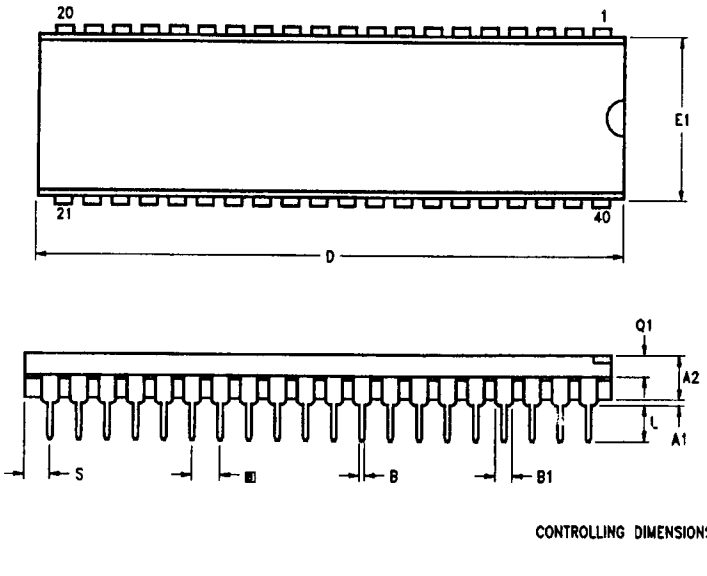
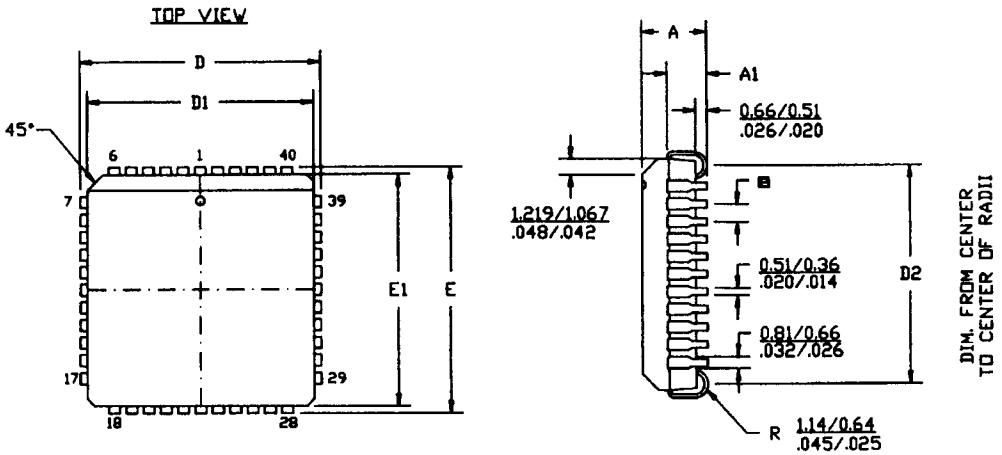


Figure 50. Stack Pointer Low (FF_H: Read/Write)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 53. 40-Pin DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 54. 44-Pin PLCC Package Diagram