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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c3312pscr5104

GENERAL DESCRIPTION (Continued)

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

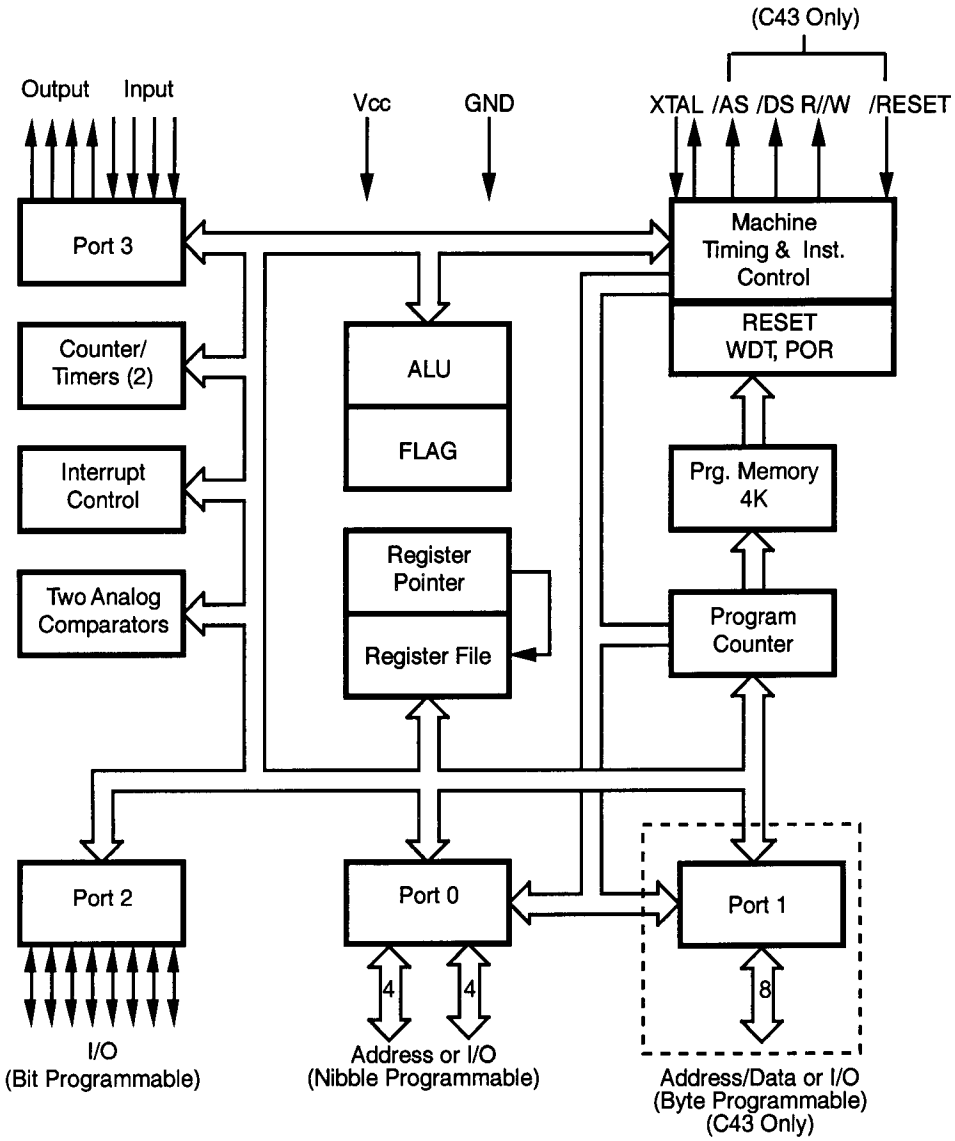

Figure 1. Functional Block Diagram

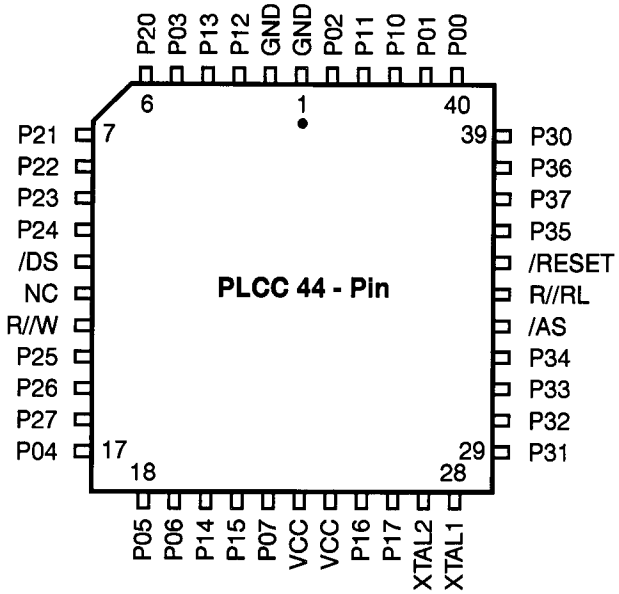

Figure 5. 44-Pin PLCC Pin Assignments

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	N/C	Not Connected	
13	R//W	Read/Write	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output
20-21	P14-15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23,24	V_{CC}	Power Supply	
25-26	P16-17	Port 1, Pins 6,7	In/Output

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
27	XTAL2	Crystal, Oscillator Clock	Output
28	XTAL1	Crystal, Oscillator Clock	Input
29-31	P31-33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless Control	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-01	Port 0, Pins 0,1	In/Output
42-43	P10-11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN DESCRIPTION (Continued)

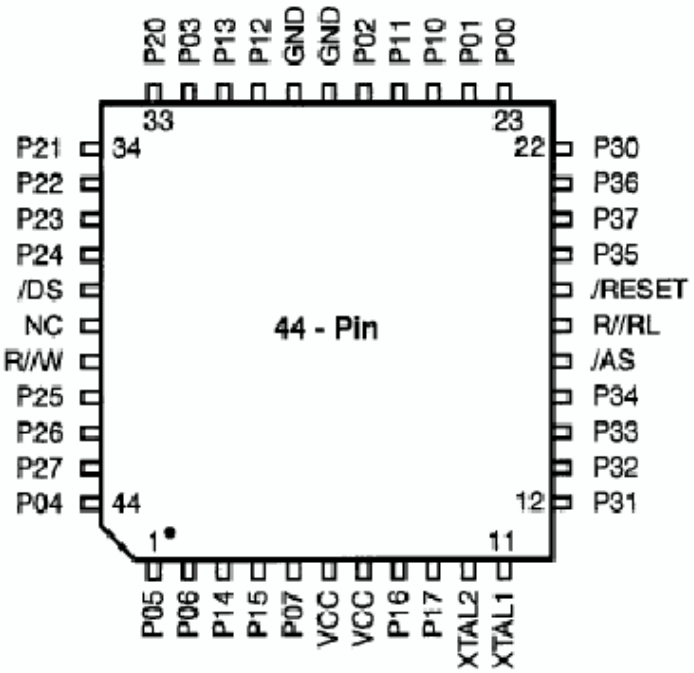

Figure 6. 44-Pin LQFP Pin Assignments

Table 4. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output
3-4	P14-15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	V_{CC}	Power Supply	
8-9	P16-17	Port 1 Pins 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless Control	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output

Table 4. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-01	Port 0, Pins 0,1	In/Output
25-26	P10-11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	N/C	Not Connected	
40	R//W	Read/Write	Output
41-43	P25-27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7.)

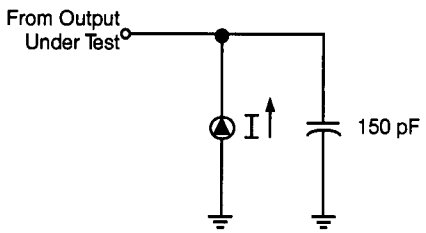

Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.6	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.4	V	I_{OL} = +12 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.8	V		13
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.6	V		13
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		13
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.6	V		13
V_{OLR}	Reset Output Low Voltage	3.0V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	13
		5.5V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	13
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	2	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
IIR	Reset Input Current	3.0V	-20	-130	-18	-130	-60	µA		
		5.5V	-20	-180	-18	-180	-85	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	4
		5.5V		25		25	20	mA	@ 16 MHz	4
		3.0V		15		15	5	mA	@ 12 MHz	4
		5.5V		20		20	15	mA	@ 12 MHz	4

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A = 0° C to +70°C		T_A = –40°C to +105°C					
		V_{CC}					Typical [1]			
Sym	Parameter	Note [3]	Min	Max	Min	Max	@ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		5.5V		10		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,11, 14
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (C43 Only) (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3]	T_A=–0°C to 70°C				T_A = –40°C to +105°C					
				12 MHz		16 MHz		12 MHz		16 MHz			
			V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25		ns	2
			5.5	35		25		35		25			2
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	1,2
			5.5		250		180		250		180	ns	2
4	TwAS	/AS Low Width	3.0	55		40		55		40		ns	2
			5.5	55		40		55		40		ns	2
5	TdAS(DS)	Address Float to /DS Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135		ns	1,2
			5.5	200		135		200		135		ns	1,2
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80		ns	1,2
			5.5	110		80		110		80		ns	1,2
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	1,2
			5.5		150		75		150		75	ns	1,2
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.0	0		0		0		0		ns	2
			5.5	0		0		0		0		ns	2
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50		ns	2
			5.5	55		50		55		50		ns	2
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35		ns	2
			5.5	45		35		45		55		ns	2
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	3.0	45		25		45		25		ns	2
			5.5	45		25		45		25		ns	2
13	TdDS(R/W)	/DS Rise to R//W Not Valid	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25		ns	2
			5.5	55		25		55		25		ns	2
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	1,2
			5.5		310		230		310		230	ns	1,2
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45		ns	2
			5.5	65		45		65		45		ns	2
18	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30		ns	2
			5.5	35		30		35		30		ns	2

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	Note [3] V_{CC}	T_A=–0°C to 70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = –40°C to +105°C 12 MHz Min	Max	16 MHz Min	Max	Units	Notes
19	TdDs(DM)	/DS Rise to DM	3.0	45		35		45		35		ns	2
		Valid Delay	5.5	45		35		45		35		ns	2
20	ThDS(AS)	/DS Valid to Address	3.0	45		35		45		35		ns	2
		Valid Home Time	5.5	45		35		45		35		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

No	Symbol	Parameter	Note [3] V_{CC}	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A =–4 0°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
13	TPOR	Power-On Reset Delay	3.0V	3	24	3	24	3	25	3	25	ms	
			5.5V	1.5	13	1.5	13	1	14	1	14	ms	

Notes: :

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. Standard Oscillator mode, Pcon RegD7=1.
8. Maximum frequency for external XTAL Clock is 4MHz when using low EMI oscillator mode, Pcon Reg D7=0.

PIN FUNCTIONS (Continued)

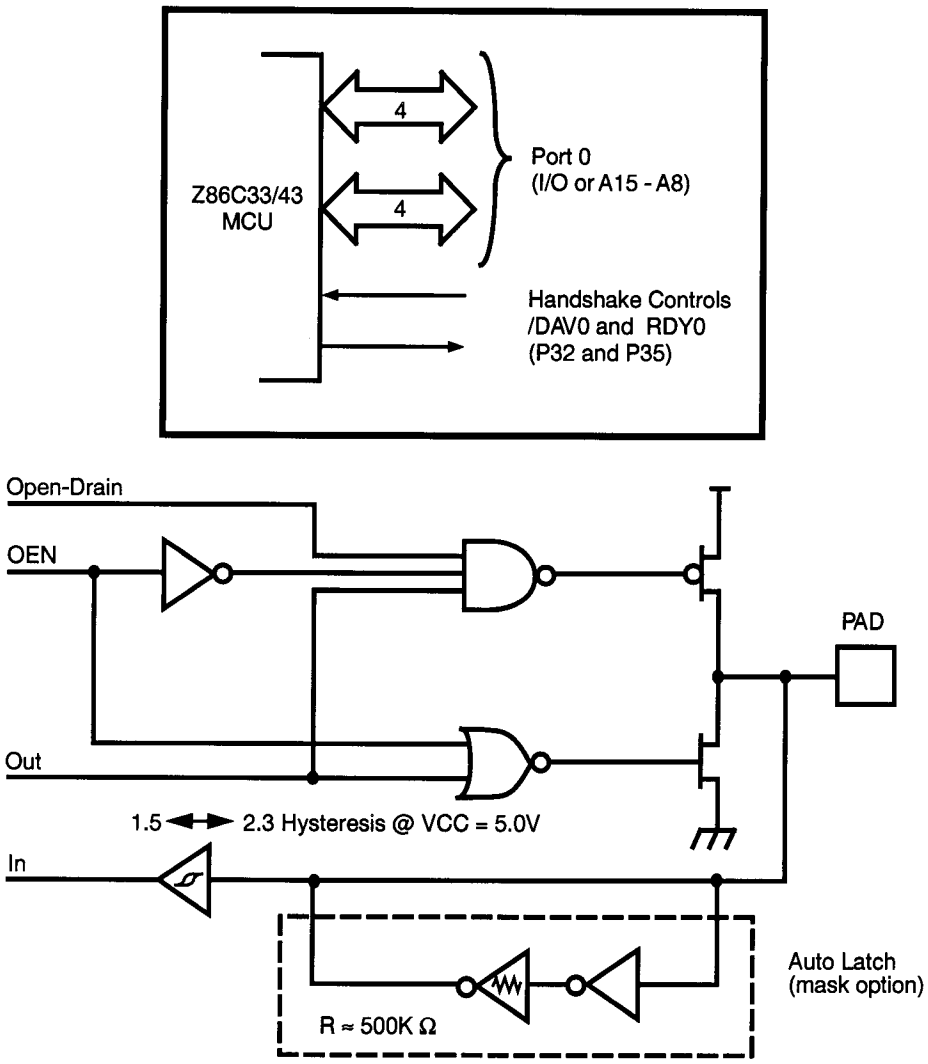

Figure 12. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port (Figure 13), with multiplexed Address (A7-A0) and Data (D7-D0) ports. For the Z86C33/43 ROM device, these eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and byte-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Note: Port 1 is not available on Z86C33 and P01M Register for Z86C33 must have Bit D4,D3 set as 00.

Note: Low EMI mode is not supported on the emulator for Port1. Pcon reg. D4 must be 1.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 4095 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z86C33/43 to share common resources in multiprocessor and DMA applications.

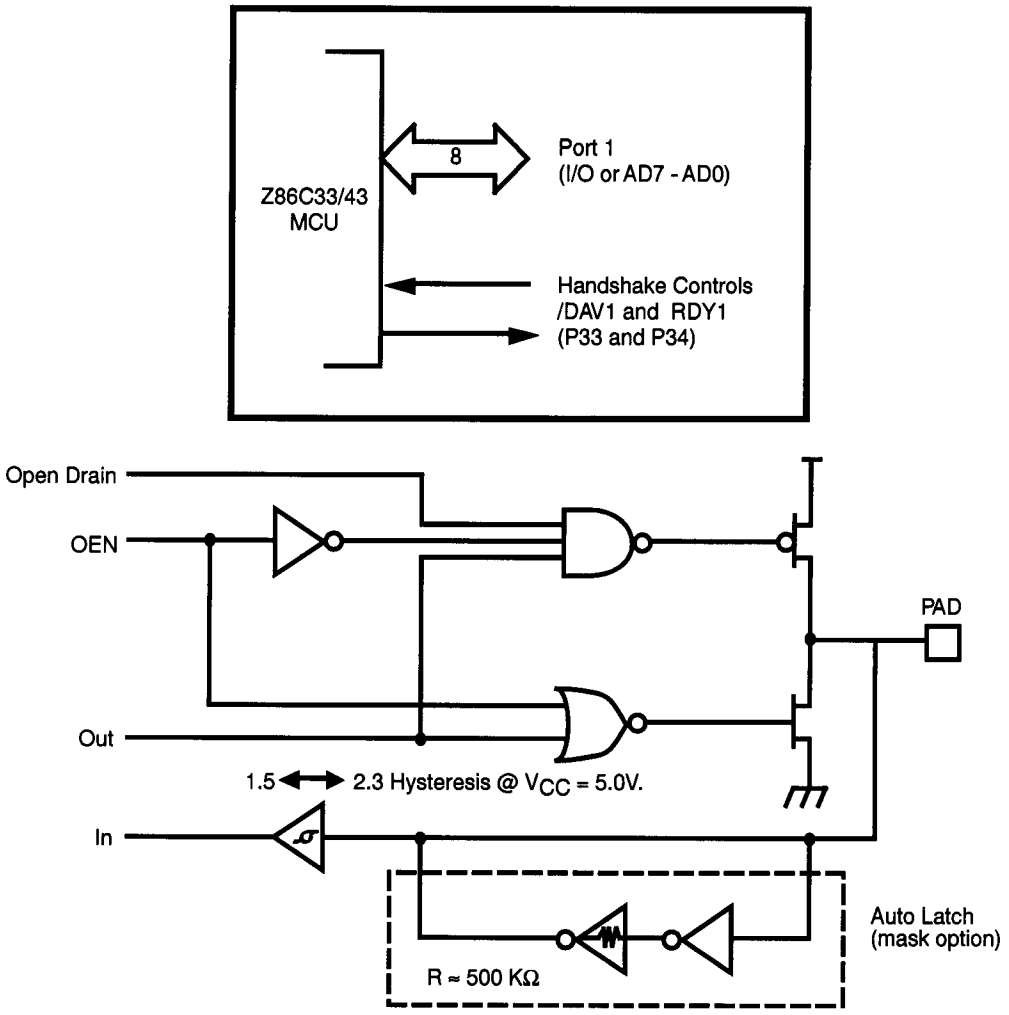

Figure 13. Port 1 Configuration

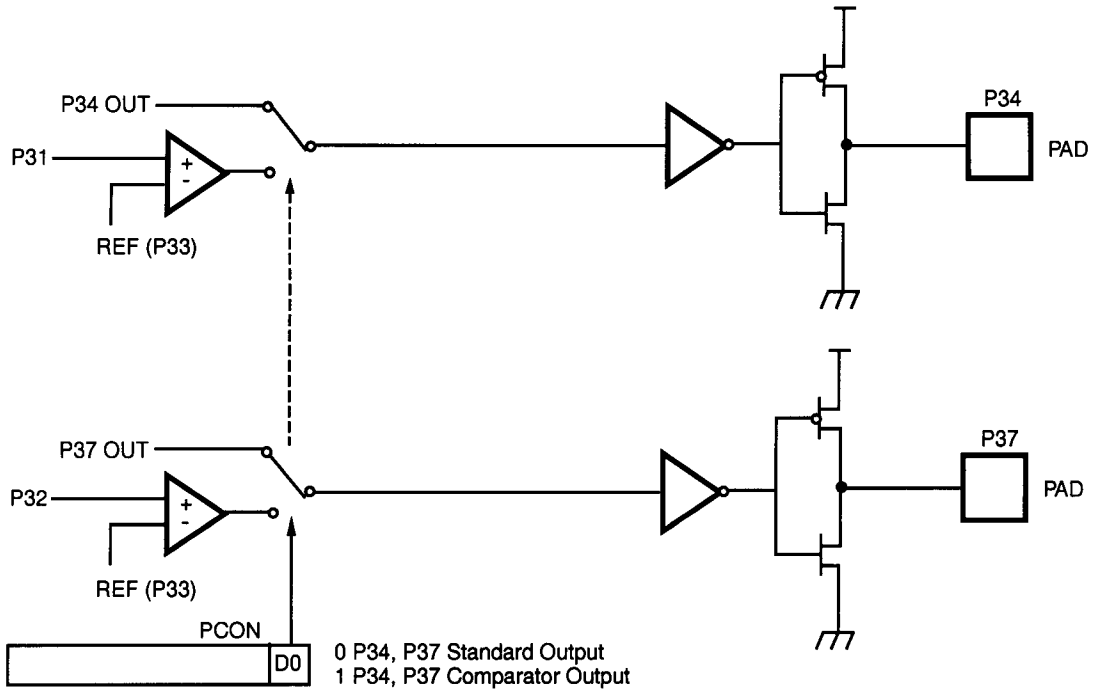

Figure 16. Port 3 Configuration

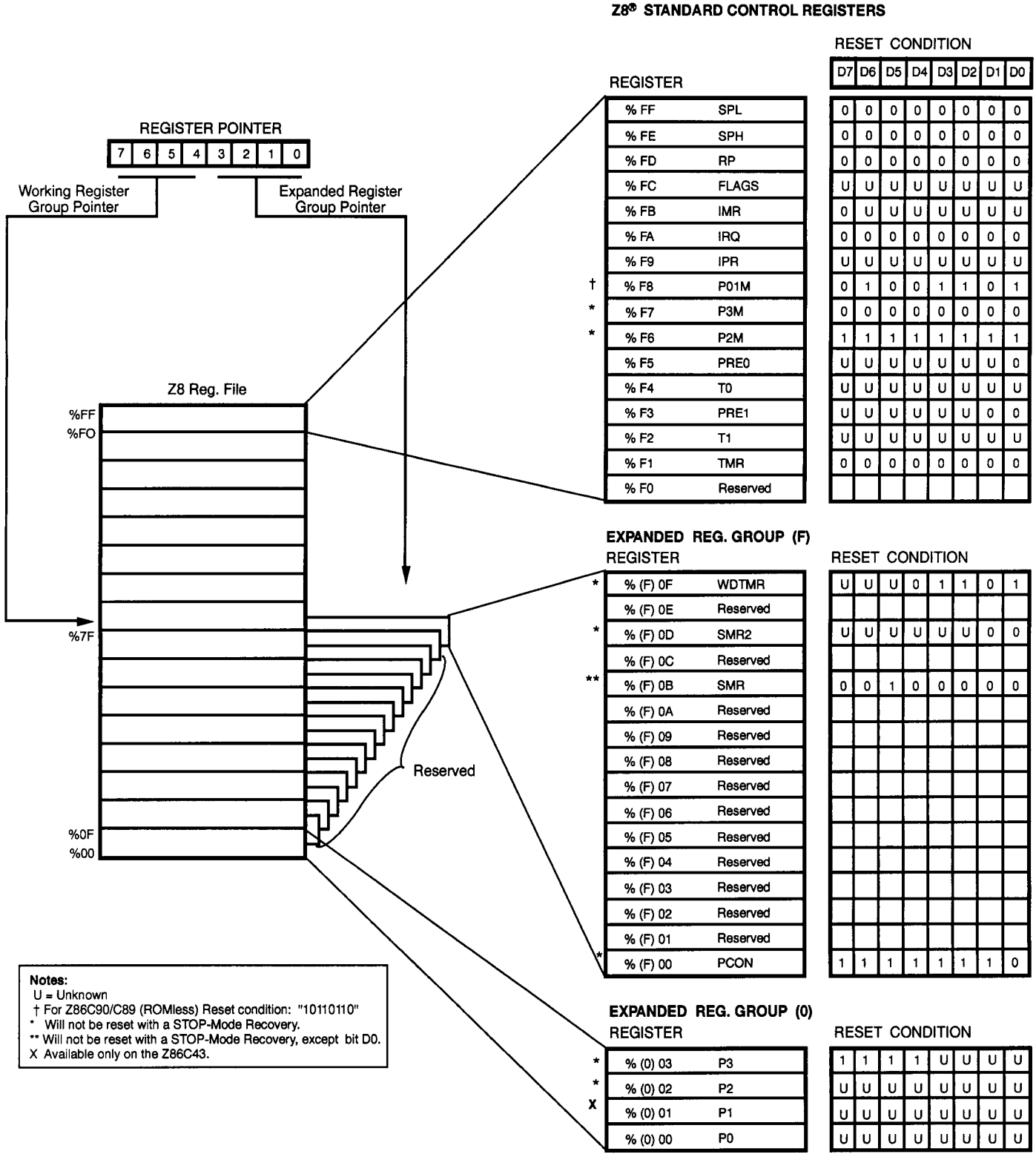

Figure 19. Expanded Register File Architecture

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V.

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the IMR register, bit D6. A 1 in D6 enables RAM Protect.

Stack. The Z86C33/43 external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). SPH is used as a general-purpose register when using internal stack only. The Z86C33 uses the 8-bit stack pointer (R255) for internal stack only.

Note: R254 and R255 are set to 00Hex after any reset or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 23).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. TIN Mode is enabled by setting R243 PRE1 Bit D1 to 0.

Interrupts. The Z86C33/43 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 23) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 6). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

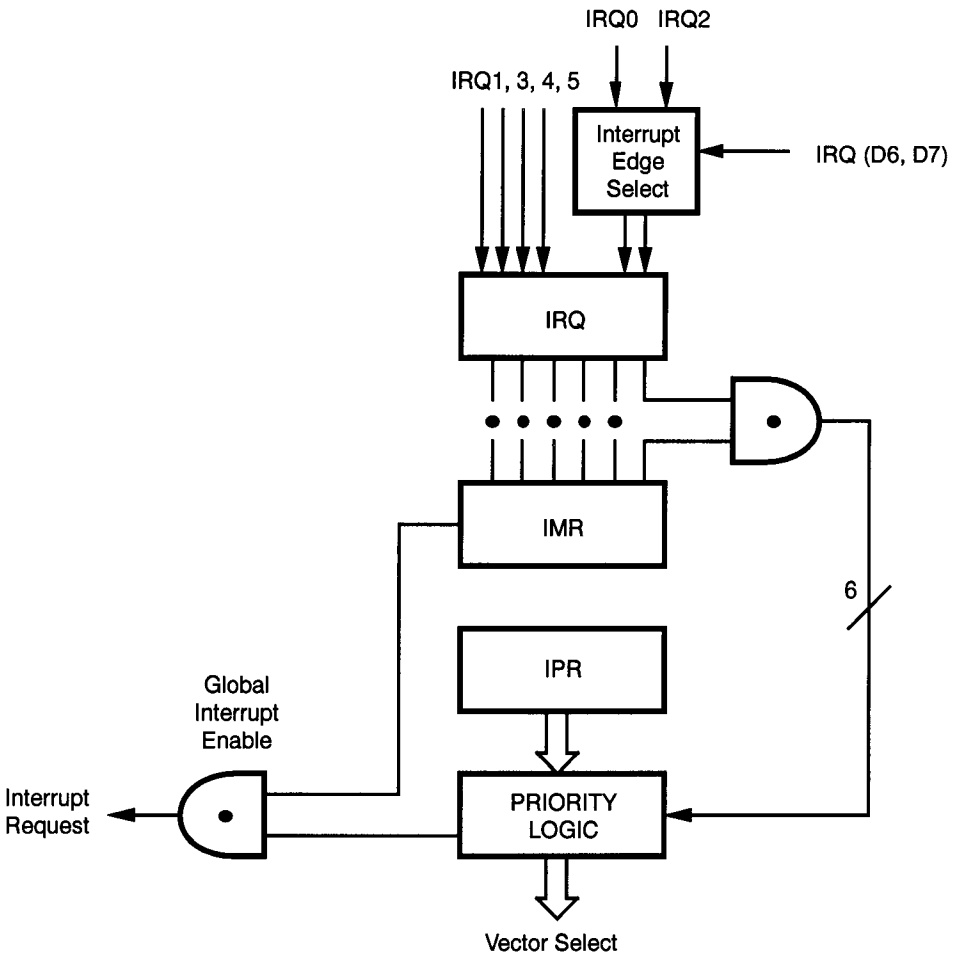

Figure 23. Interrupt Block Diagram

Table 6. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, TIN	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

Table 8. Stop-Mode Recovery Source

SMR:432 D4	D3	D2	Operation Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the TPOR /RESET delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C33/43 from STOP Mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 27). This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source. Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR2 circuitry.

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

Table 9. Stop-Mode Recovery Source

SMR:10 D1	D0	Operation Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 29).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in STOP-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but the POR delay counter will still be enabled even though the SMR stop delay is disabled.

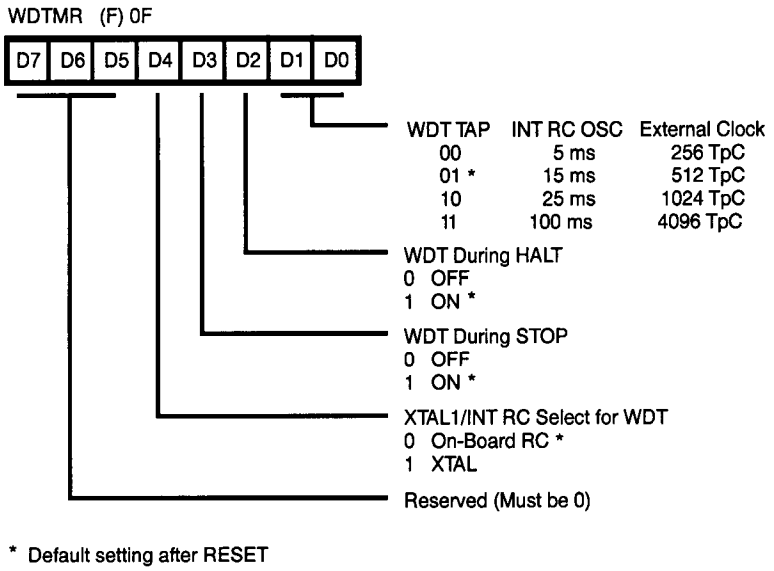

Figure 29. Watch-Dog Timer Mode Register (Write Only)

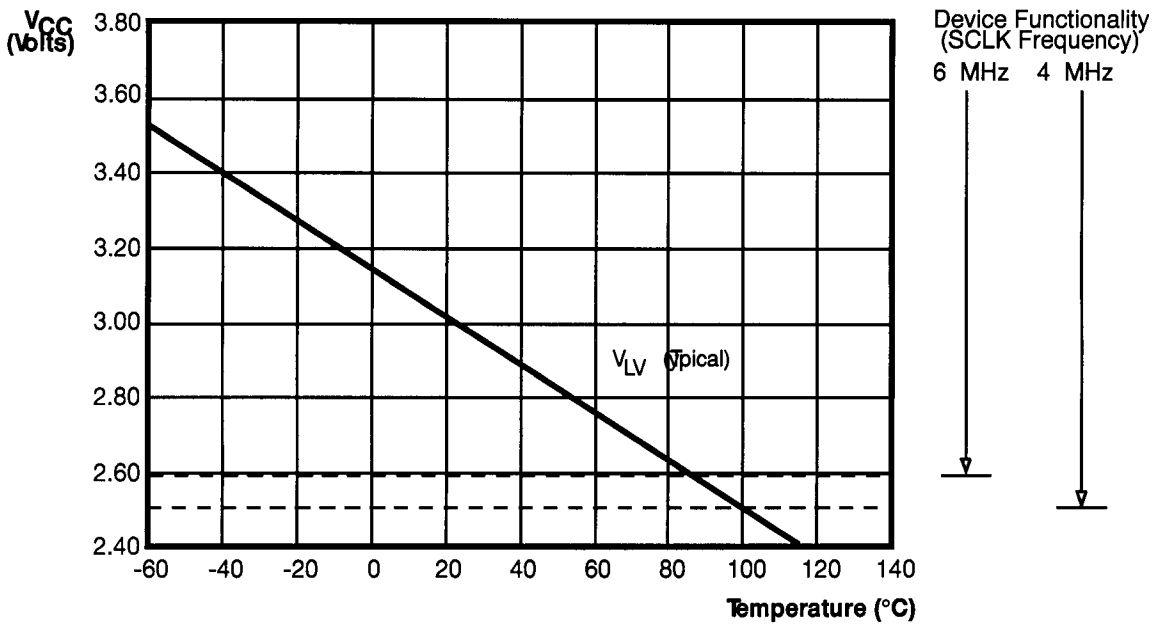

Figure 31. Typical Z86C33/43 Low Voltage Protection vs Temperature

Z8 CONTROL REGISTERS (Continued)

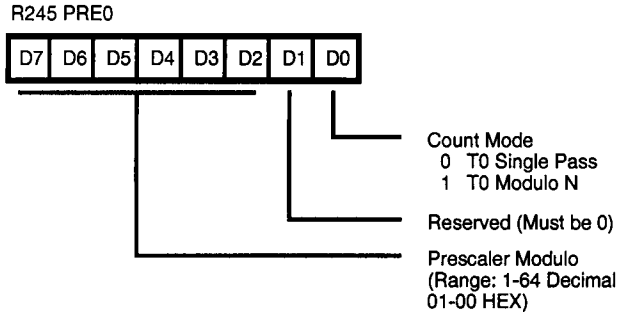

Figure 40. Prescaler 0 Register ($F5_H$: Write Only)

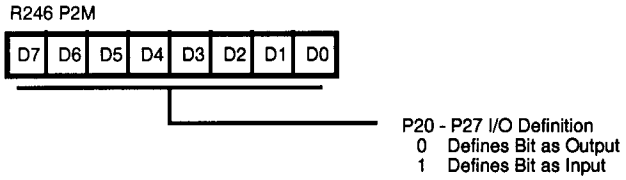

Figure 41. Port 2 Mode Register ($F6_H$: Write Only)

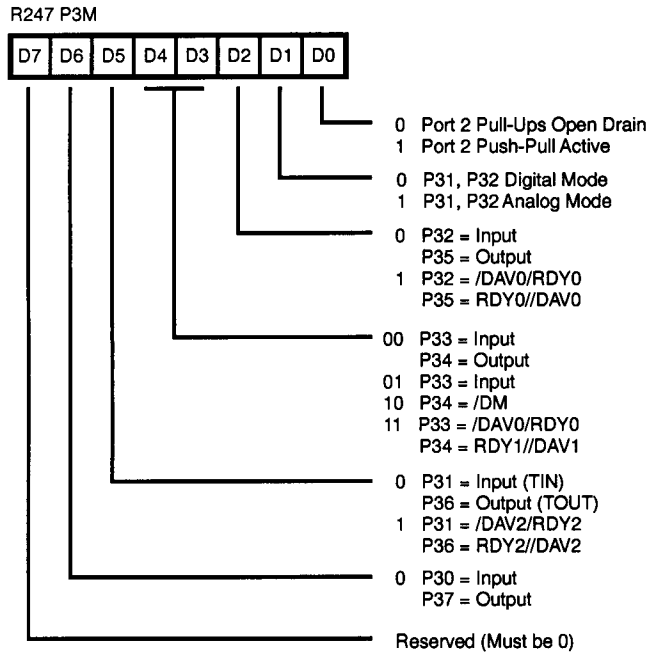

Figure 42. Port 3 Mode Register ($F7_H$: Write Only)

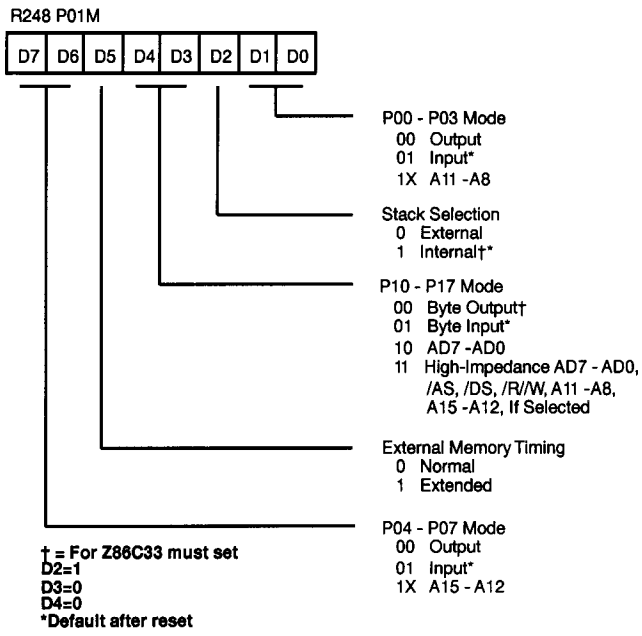

Figure 43. Port 0 and 1 Mode Register ($F8_H$: Write Only)

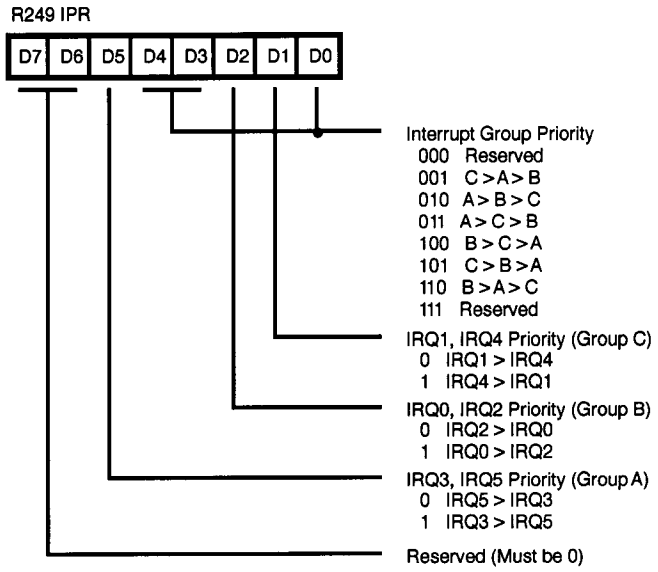

Figure 44. Interrupt Priority Register ($F9_H$: Write Only)

Precautions

1. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory
2. When in ROM Protect Mode, and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.
3. The device has an oscillator-free WDT reset for the device pins. When the device is reset from a WDT timeout, the reset will force the device pins to their reset default state even if the oscillator is not running.
4. The Port 3 outputs are reset to High State after Reset, except after Stop-Mode Recovery, at which time the outputs remain in the last state.
5. Extended timing is operable.
6. P0/P1/P2/P3 is Low-EMI software programmable.
7. P0/P1/P2 is software programmable for open-drain.
8. Expanded register PCON is Write-Only.
9. WDTMR is writeable only within the first 60 internal system clocks after Reset. Afterward, the WDTMR is write protected.
10. Device functions down to the V_{LV} threshold. At temperatures less than 25°C, the V_{LV} threshold will rise to a maximum V_{DD} of 3.6V.
11. Low-EMI is 25 percent of standard pull-down output driver, and 25 percent of standard pull-up output driver.
12. There is no clock filter on Reset pin.
13. Registers FE Hex (SPH) and FF Hex (SPL) are set to 00 Hex after any reset.
14. When Low EMI OSC is selected (PCON Reg Bit D7=0), the output drive of /DS, /AS, and R//W will also be in Low-EMI Mode.
15. P01M Reg Bit D4, D3 must be set to 00 Hex for Z86C33.
16. Must add a two NOP delay after selecting the P3M bit D1 to 1 before the comparitor output is valid. IRQ0, IRQ1, and IRQ2 should be cleared in IRQ register when the comparitor is enabled or disabled to avoid spurious noise creating a false interrupt.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.