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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8245lvv333d

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, a 16-Kbyte instruction cache, a 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade off performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8245 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8245 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8245 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—Entire cache or on a per-way basis up to three of four ways
  - Dynamic power management: 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing supporting SDRAM
    - One to eight banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System-level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—Marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std 1149.1® (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8245:

Technology	0.25-µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully-static
Packages	Surface-mount 352 tape ball grid array (TBGA)
Core power supply	1.7 V to 2.1 V DC for 266 and 300 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 1.8/1.9/2.0 volts. 1.9 V to 2.2 V DC for 333 and 350 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 2.0/2.1 volts. See Table 2 for details of recommended operating conditions)
I/O power supply	3.0- to 3.6-V DC

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8245.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other DC electrical characteristics.

Table 2. Recommended Operating Conditions[1] (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8/1.9/2.0 V ±	V	4, 7, 12
			2.0/2.1 V ±	V	5, 7, 12
PCI reference		LV_{DD}	5.0 ± 5%	V	2, 10, 11
			3.3 ± 0.3	V	3, 10, 11
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	2, 3
	All other inputs		0 to 3.6	V	6
Die-junction temperature		T_j	0 to 105	°C	

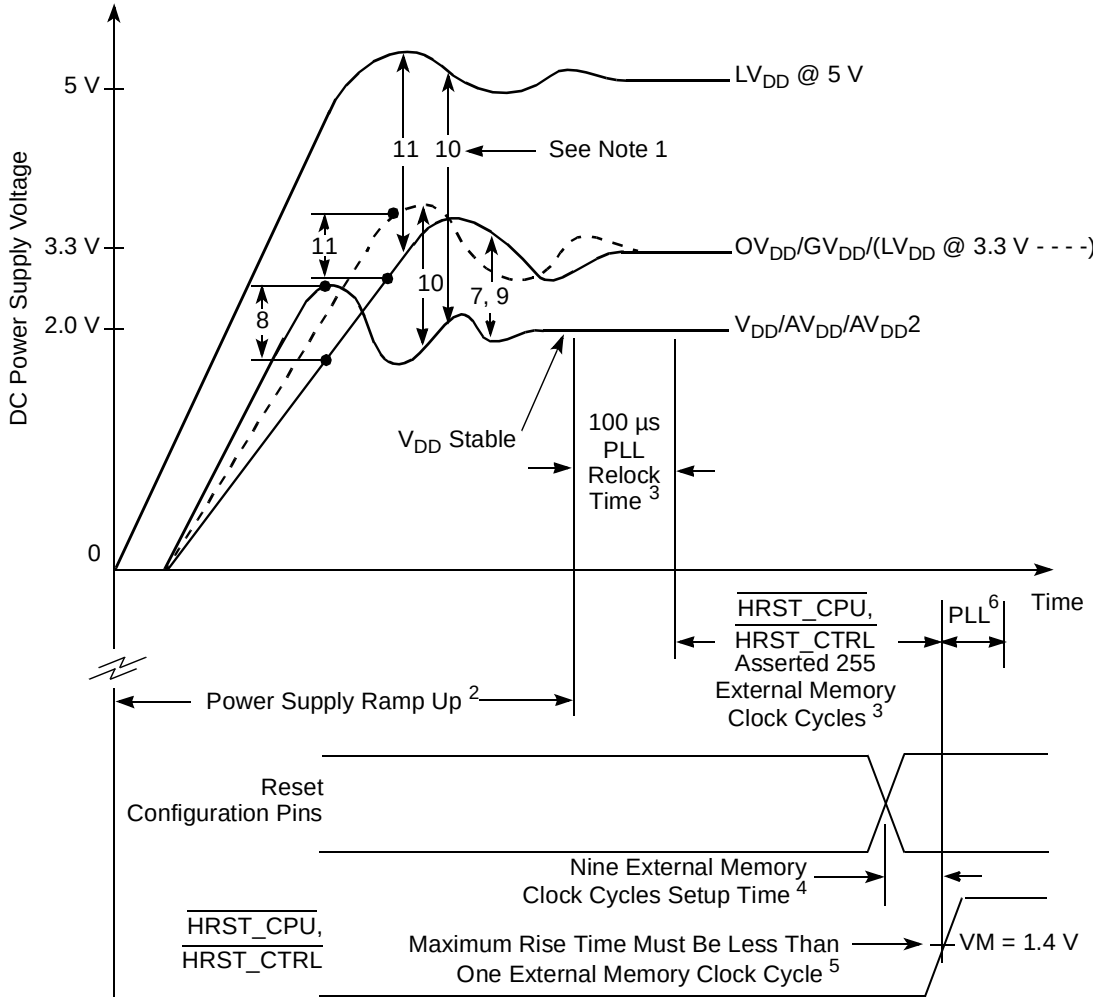
Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PCI pins are designed to withstand LV_{DD} + 5% V DC when LV_{DD} is connected to a 5.0-V DC power supply.
3. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3-V DC power supply.
4. The voltage supply value of 1.8/1.9/2.0 V ± 100 mV applies to parts marked as having a maximum CPU speed of 266 and 300 MHz. See Table 7. For each chosen nominal value (1.8/1.9/2.0 V) the supply voltage should not exceed ± 100 mV of the nominal value.
5. The voltage supply value of 2.0/2.1 V ± 100 m V applies to parts marked as having a maximum CPU speed of 333 and 350 MHz. See Table 7. For each chosen nominal value (2.0/2.1 V) the supply voltage should not exceed ± 100 mV of the nominal value.

Cautions:

6. Input voltage (V_{in}) must not be greater than the supply voltage (V_{DD}/AV_{DD}/$AV_{DD}2$) by more than 2.5 V at all times, including during power-on reset. Input voltage (V_{in}) must not be greater than GV_{DD}/OV_{DD} by more than 0.6 V at all times, including during power-on reset.
7. OV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. V_{DD}/AV_{DD}/$AV_{DD}2$ must not exceed OV_{DD} by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. GV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. LV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
11. LV_{DD} must not exceed OV_{DD} by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
12. This voltage is the input to the filter discussed in Section 7.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. See Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for additional information on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8245. For details, see Section 7.8, "Thermal Management."

Table 6. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection (Single-layer board—1s)	$R_{\theta JA}$	16.1	°C/W	1, 2
Junction-to-ambient natural convection (Four-layer board—2s2p)	$R_{\theta JMA}$	12.0	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Single-layer board—1s)	$R_{\theta JMA}$	11.6	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Four layer board—2s2p)	$R_{\theta JMA}$	9.0	°C/W	1, 3
Junction-to-board	$R_{\theta JB}$	4.8	°C/W	4
Junction-to-case	$R_{\theta JC}$	1.8	°C/W	5
Junction-to-package top (natural convection)	Ψ_{JT}	1.0	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate used for case temperature.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 9, "Ordering Information," for details on ordering parts.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for details on MPC8245 memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

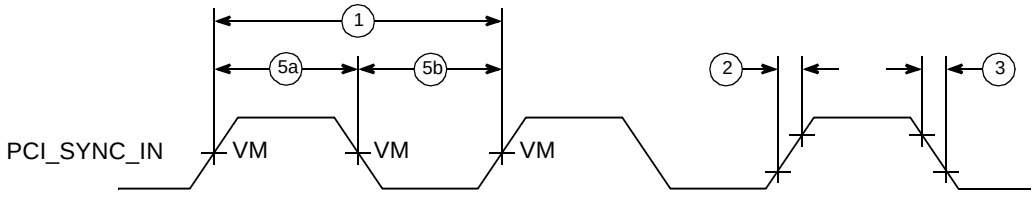


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The gray areas show where the DLL locks.

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL; that is, the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Note that keeping a DLL mode that is locked below tap point decimal 12 is not recommended.

Table 10. Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to *sys_logic_clk* (input setup)				
10b0	Tap 0, register offset <0x77>, bits 5–4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5–4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5–4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5–4 = 0b11	0.5	—		
10c	PIC, misc. debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^2C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5–4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5–4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5–4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5–4 = 0b11	2.1	—		
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to Inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5–4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. To maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*, the feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range. The feedback trace length is relative to the SDRAM clock output trace lengths. We recommend that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the problem of T_{os}, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.

Table 13. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8245 provides a delay time of at least 300 ns for the SDA signal (referred to as the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the MPC8245acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA is balanced, the MPC8245 does not cause the unintended generation of a Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8245 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved. It is assumed that the desired I²C SCL clock frequency is 400 KHz and the digital filter sampling rate register (DFFSR bits in I2CFDR) is programmed with its default setting of 0x10 (decimal 16):

SDRAM Clock Frequency	100 MHz	133 MHz
FDR Bit Setting	0x00	0x2A
Actual FDR Divider Selected	384	896
Actual I²C SCL Frequency Generated	260.4 KHz	148.4 KHz

   For details on I²C frequency calculation, refer to the application note AN2919 “Determining the I²C Frequency Divider Ratio for SCL”.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design.

Figure 16 provides the AC test load for the I²C.

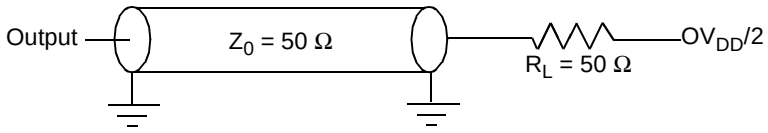


Figure 16. I²C AC Test Load

5.3 Pinout Listings

Table 16 provides the pinout listing for the MPC8245, 352 TBGA package.

Table 16. MPC8245 Pinout Listing

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{\text{C/BE}}$[3:0]	P25 K23 F23 A25	I/O	OV_{DD}	DRV_PCI	6, 15
$\overline{\text{DEVSEL}}$	H26	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{FRAME}}$	J24	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{IRDY}}$	K25	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{LOCK}}$	J26	Input	OV_{DD}	—	8
AD[31:0]	V25 U25 U26 U24 U23 T25 T26 R25 R26 N26 N25 N23 M26 M25 L25 L26 F24 E26 E25 E23 D26 D25 C26 A26 B26 A24 B24 D19 B23 B22 D22 C22	I/O	OV_{DD}	DRV_PCI	6, 15
PAR	G25	I/O	OV_{DD}	DRV_PCI	15
$\overline{\text{GNT}}$[3:0]	W25 W24 W23 V26	Output	OV_{DD}	DRV_PCI	6, 15
$\overline{\text{GNT4}}$/DA5	W26	Output	OV_{DD}	DRV_PCI	7, 15, 14
$\overline{\text{REQ}}$[3:0]	Y25 AA26 AA25 AB26	Input	OV_{DD}	—	6, 12
$\overline{\text{REQ4}}$/DA4	Y26	I/O	OV_{DD}	—	12, 14
$\overline{\text{PERR}}$	G26	I/O	OV_{DD}	DRV_PCI	8, 15, 18
$\overline{\text{SERR}}$	F26	I/O	OV_{DD}	DRV_PCI	8, 15, 16
$\overline{\text{STOP}}$	H25	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{TRDY}}$	K26	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{INTA}}$	AC26	Output	OV_{DD}	DRV_PCI	10, 15, 16
IDSEL	P26	Input	OV_{DD}	—	
Memory Interface Signals					
MDL[0:31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GV_{DD}	DRV_STD_MEM	5, 6
MDH[0:31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GV_{DD}	DRV_STD_MEM	6

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DUART Control Signals					
SOUT1/PCI_CLK0	AC25	Output	GV_{DD}	DRV_MEM_CTRL	13, 14
SIN1/PCI_CLK1	AB25	I/O	GV_{DD}	DRV_MEM_CTRL	13, 14, 26
SOUT2/$\overline{\text{RTS1}}$/ PCI_CLK2	AE26	Output	GV_{DD}	DRV_MEM_CTRL	13, 14
SIN2/$\overline{\text{CTS1}}$/ PCI_CLK3	AF25	I	GV_{DD}	DRV_MEM_CTRL	13, 14, 26
Clock-Out Signals					
PCI_CLK0/SOUT1	AC25	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_CLK1/SIN1	AB25	Output	GV_{DD}	DRV_PCI_CLK	13, 14, 26
PCI_CLK2/$\overline{\text{RTS1}}$/ SOUT2	AE26	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_CLK3/$\overline{\text{CTS1}}$/ SIN2	AF25	Output	GV_{DD}	DRV_PCI_CLK	13, 14, 26
PCI_CLK4/DA3	AF26	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_SYNC_OUT	AD25	Output	GV_{DD}	DRV_PCI_CLK	
PCI_SYNC_IN	AB23	Input	GV_{DD}	—	
SDRAM_CLK [0:3]	D1 G1 G2 E1	Output	GV_{DD}	DRV_MEM_CTRL or DRV_MEM_CLK	6, 21
SDRAM_SYNC_OUT	C1	Output	GV_{DD}	DRV_MEM_CTRL or DRV_MEM_CLK	21
SDRAM_SYNC_IN	H3	Input	GV_{DD}	—	
CKO/DA1	B15	Output	OV_{DD}	DRV_STD_MEM	14
OSC_IN	AD21	Input	OV_{DD}	—	19
Miscellaneous Signals					
$\overline{\text{HRST\_CTRL}}$	A20	Input	OV_{DD}	—	27
$\overline{\text{HRST\_CPU}}$	A19	Input	OV_{DD}	—	27
$\overline{\text{MCP}}$	A17	Output	OV_{DD}	DRV_STD_MEM	3, 4, 17
NMI	D16	Input	OV_{DD}	—	
$\overline{\text{SMI}}$	A18	Input	OV_{DD}	—	10
$\overline{\text{SRESET}}$/SDMA12	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TBEN/SDMA13	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
13	10011[12]	Not available			25[2,7]	100	300	4 (2)	3 (2)
14	10100[12]	26[6]–38[5]	52–76	182–266	26[6]–42[5]	52–84	182–294	2 (4)	3.5 (2)
15	10101[12]	Not available			27[3]–30[5,7]	68–75	272–300	2.5 (2)	4 (2)
16	10110[12]	25–33[5]	50–66	200–264	25–37[5]	50–74	200–296	2 (4)	4 (2)
17	10111[12]	25–33[5]	100–132	200–264	25–33[2]	100–132	200–264	4 (2)	2 (2)
18	11000[12]	27[3]–35[5]	68–88	204–264	27[3]–40[5,7]	68–100	204–300	2.5 (2)	3 (2)
19	11001[12]	36[6]–53[5]	72–106	180–265	36[6]–59[2]	72–118	180–295	2 (2)	2.5 (2)
1A	11010[12]	50[18]–66[1]	50–66	200–264	50[18]–66[1]	50–66	200–264	1 (4)	4 (2)
1B	11011[12]	34[3]–44[5]	68–88	204–264	34[3]–50[5,7]	68–100	204–300	2 (2)	3 (2)
1C	11100[12]	44[3]–59[5]	66–88	198–264	44[3]–66[1]	66–99	198–297	1.5 (2)	3 (2)
1D	11101[12]	48[6]–66[1]	72–99	180–248	48[6]–66[1]	72–99	180–248	1.5 (2)	2.5 (2)
1E Rev B	11110[8]	Not usable			Not usable			Off	Off
1E Rev D	11110	33[3]–38[5]	66–76	231–266	33[3]–42[5]	66–84	231–294	2(2)	3.5(2)

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Not usable			Off	Off

Notes:

1. Limited by the maximum PCI input frequency (66 MHz).
2 Limited by the maximum system memory interface operating frequency (100 MHz @ 300 MHz CPU).
3. Limited by the minimum memory VCO frequency (133 MHz).
4. Limited due to the maximum memory VCO frequency (372 MHz).
5. Limited by the maximum CPU operating frequency.
6. Limited by the minimum CPU VCO frequency (360 MHz).
7. Limited by the maximum CPU VCO frequency (maximum marked CPU speed X 2).
8. In clock-off mode, no clocking occurs inside the MPC8245, regardless of the PCI_SYNC_IN input.
9. Range values are rounded down to the nearest whole number (decimal place accuracy removed).
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting differ from the MPC8240 and are not backward-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting differs from or does not exist on the MPC8240 and may not be fully backward-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
16. Limited by the maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).
17. Limited by the minimum CPU operating frequency (100 MHz).
18. Limited by the minimum memory bus frequency (50 MHz).

Table 18. PLL Configurations (333- and 350-MHz Parts)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–44[16]	75–132	188–330	25–44[16]	75–132	188–330	3 (2)	2.5 (2)
1	00001[12]	25–37[5,7]	75–111	225–333	25–38[5]	75–114	225–342	3 (2)	3 (2)

7 System Design

This section provides electrical and thermal design recommendations for successful application of the MPC8245.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8245 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500-kHz to 10-MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 25 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), using multiple small capacitors of equal value is recommended over using multiple values.

Place the circuits as closely as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing from the capacitors to the input signal pins should be as direct as possible with minimal inductance of vias.

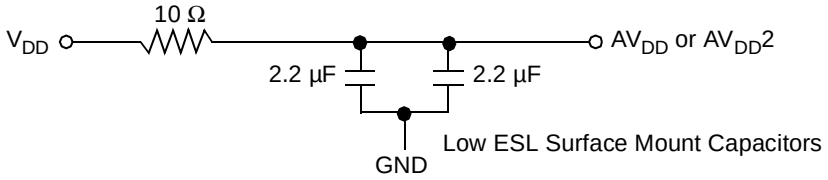


Figure 25. PLL Power Supply Filter Circuit

7.2 Decoupling Recommendations

Due to its dynamic power management feature, large address and data buses, and high operating frequencies, the MPC8245 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8245 system, and the MPC8245 itself requires a clean, tightly regulated source of power. Therefore, place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin. These decoupling capacitors should receive their power from dedicated power planes in the PCB, with short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
2	—	Globally changed EPIC to PIC. Section 1.4.1.4—Note 5: Changed register reference from 0x72 to 0x73. Section 1.4.1.5—Table 5: Updated power dissipation numbers based on latest characterization data. Section 1.4.2—Table 6: Updated table to show more thermal specifications. Section 1.4.3—Table 7: Updated minimum memory bus value to 50 MHz. Section 1.4.3.1—Changed equations for DLL locking range based on characterization data. Added updates and reference to AN2164 for note 6. Added table defining Tdp parameters. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Table 10: Changed bit definitions for tap points. Updated note on Tos and added reference to AN2164 for note 7. Updated Figure 9 to show significance of Tos. Section 1.4.3.4—Added column for SDRAM_CLK @ 133 MHz Sections 1.5.1 and 1.5.2—Corrected packaging information to state TBGA packaging. Section 1.5.3—Corrected some signals in Table 16 which were missing overbars in the Rev 1.0 release of the document. Section 1.6—Updated Note 10 of Tables 18 and 19. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.9—Updated format of tables in Ordering Information section.
1	—	Updated document template. Section 1.4.1.4—Changed the driver type names in Table 6 to match with the names used in the MPC8245 Reference Manual. Section 1.5.3—Updated driver type names for signals in Table 16 to match with names used in the MPC8245 Integrated Processor Reference Manual. Section 1.4.1.2—Updated Table 7 to refer to new PLL Tables for VCO limits. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid timing. Section 1.5.1—Updated solder balls information to 62Sn/36PB/2Ag. Section 1.6—Updated PLL Tables 17 and 18 and appropriate notes to reflect changes of VCO ranges for memory and CPU frequencies. Section 1.7—Updated voltage sequencing requirements in Table 2 and removed Section 1.7.2. Section 1.7.8—Updated TRST information and Figure 26. New Section 1.7.2—Updated the range of I/O power consumption numbers for OV_{DD} and GV_{DD} to correct values as in Table 5. Updated fastest frequency combination to 66:100:350 MHz. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of Ordering Information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.
0.5	—	Corrected labels for Figures 5 through 8.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.4	—	Section 1.2—Changed Features list (format) to match with the features list of the *MPC8245 Integrated Processor Reference Manual*. Section 1.4.1.2—Updated Table 2 to include 1.8 ± 100mV numbers. Section 1.4.3—Changed Table 7 to include new part offerings of 333 and 350 MHz. Added rows to include VCO frequency ranges for all parts for both memory VCO and CPU VCO. Section 1.4.1.5—Updated power consumption table to include 1.8 V (V_{DD}) and higher frequency numbers. Section 1.4.3—Updated Table 7 to include higher frequency offerings and CPU VCO frequency range. Section 1.4.3.1—Changed lettering to caps for DLL_EXTEND and DLL_MAX_DELAY in graph description section. Section 1.4.3.2—Changed name of item 11 from T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* Offset Time. Changed name to T_{os} in Note 7 as well. Section 1.6—Updated notes in Table 17. Included minimum and maximum VCO numbers for memory VCO. Changed Note 13 for location of PLL_CFG[0:4] to correct bits location. Bits 7–4 of register offset <0xE2>. Added Table 18 to cover PLL configuration of higher frequency part offerings. Section: 1.7—Changed frequency ranges for reference numbers 0, 9, 10, and 17, for the 300-MHz part to include the higher memory bus frequencies when operating at lower CPU bus frequencies. Added Table 18 to include PLL configurations for the 333 MHz and the 350 MHz CPU part offerings. Added VCO multipliers in Tables 17 and 18. Section 1.7.8—Changed T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_ SYNC_IN to *sys_logic_clk* Offset Time." Section 1.7.10—Added vendor (Cool Innovations, Inc.) to list of heat sink vendors.
0.3	—	Section 1.4.1.5—Changed Max-FP value for 33/133/266 of Table 5 from 2.3 to 2.1 watts to represent characterization data. Changed Note 4 to say V_{DD} = 2.1 for power measurements (for 2-V part). Changed numbers for maximum I/O power supplies for OV_{DD} and GV_{DD} to represent characterization data. Section 1.4.3.1—Added four graphs (Figures 5–8) and description for DLL Locking Range vs. Frequency of Operation to replace Figure 5 of Rev 0.2 document. Section 1.4.3.2—Added row (item 11: T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN timing) to Table 9 to include offset change requirement. Section 1.5.3—Changed Note 4 of PLL_CFG pins in Table 16 to Note 20. Section 1.7.2—Added diode (MUR420) to Figure 27, Voltage Sequencing Circuit, to compensate for voltage extremes in design. Section 1.7.5—Added sentence with regards to SDRAM_SYNC_IN to PCI_SYNC_IN timing requirement (T_{su}) as a connection recommendation. Section 1.7.8—Mention of T_{su} offset timing and driver capability differences between the MPC8240 and the MPC8245.

9.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications that supplement and supersede this document. Table 21 shows the part numbers addressed by the MPC8245T*XXnnnx* series. The revision level can be determined by reading the Revision ID register at address offset 0x08.

Table 21. Part Numbers Addressed by MPC8245T*XXnnnx* Series
Part Number Specification Markings
(Document Order No. MPC8245ECS01AD)

MPC	*nnnn*	X	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process Descriptor	Package [1]	Processor Frequency [2]	Revision Level	Processor Version Register Value
MPC	8245	T: –40° to 105°C	ZU = TBGA V V= Lead-free TBGA	266 MHz, 300 MHz: 1.7 V to 2.1 V 333 MHz, 350 MHz: 1.9 V to 2.2 V	D:1.4 Rev ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.

Table 22 shows the part numbers addressed by the MPC8245ARZU*nnnx* series.

Table 22. Part Numbers Addressed by MPC8245ARZU*nnnx* Series
Part Number Specification Markings
(Document Order No. MPC8245ECS02AD)

MPC	*nnnn*	*X*	X	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process [3] Identifier	Process Descriptor	Package [1]	Processor Frequency [2]	Revision Level	Processor Version Register Value
MPC	8245	A	R: 0° to 85°C	ZU = TBGA V V= Lead-free TBGA	400 MHz 2.1 V ± 100 mV	D:1.4 Rev ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.
3. Process identifier ‘A’ represents parts that are manufactured under a 29-angstrom process verses the original 35-angstrom process.

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