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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8245lvv350d

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, a 16-Kbyte instruction cache, a 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade off performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8245 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8245 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8245 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—Entire cache or on a per-way basis up to three of four ways
  - Dynamic power management: 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing supporting SDRAM
    - One to eight banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System-level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—Marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std 1149.1® (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8245:

Technology	0.25-µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully-static
Packages	Surface-mount 352 tape ball grid array (TBGA)
Core power supply	1.7 V to 2.1 V DC for 266 and 300 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 1.8/1.9/2.0 volts. 1.9 V to 2.2 V DC for 333 and 350 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 2.0/2.1 volts. See Table 2 for details of recommended operating conditions)
I/O power supply	3.0- to 3.6-V DC

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8245.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other DC electrical characteristics.

4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC8245 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.25	V
Supply voltage—memory bus drivers	GV_{DD}	–0.3 to 3.6	V
Supply voltage—PCI and standard I/O buffers	OV_{DD}	–0.3 to 3.6	V
Supply voltage—PLLs	AV_{DD}/AV_{DD} 2	–0.3 to 2.25	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105[3]	°C
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.
3. Note that this temperature range does not apply to the 400 MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8245. Some voltage values do not apply to the 400-MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

Table 2. Recommended Operating Conditions[1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply voltage	V_{DD}	1.8/1.9/2.0 V ± 100 mV	V	4, 7
		2.0/2.1 V ± 100 mV	V	5, 7
I/O buffer supply for PCI and standard	OV_{DD}	3.3 ± 0.3	V	7
Supply voltages for memory bus drivers	GV_{DD}	3.3 ± 5%	V	9
CPU PLL supply voltage	AV_{DD}	1.8/1.9/2.0 V ±	V	4, 7, 12
		2.0/2.1 V ±	V	5, 7, 12

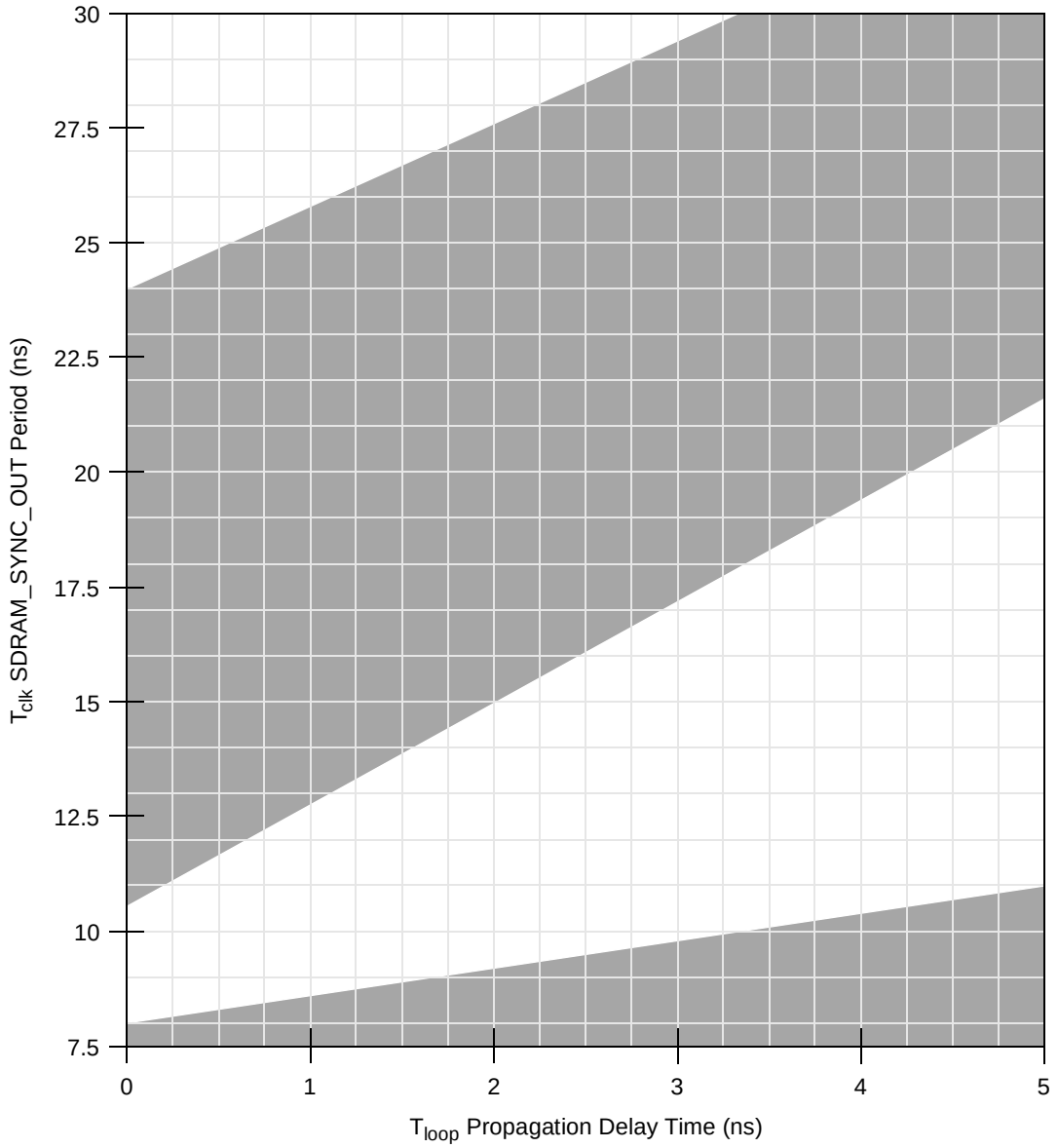
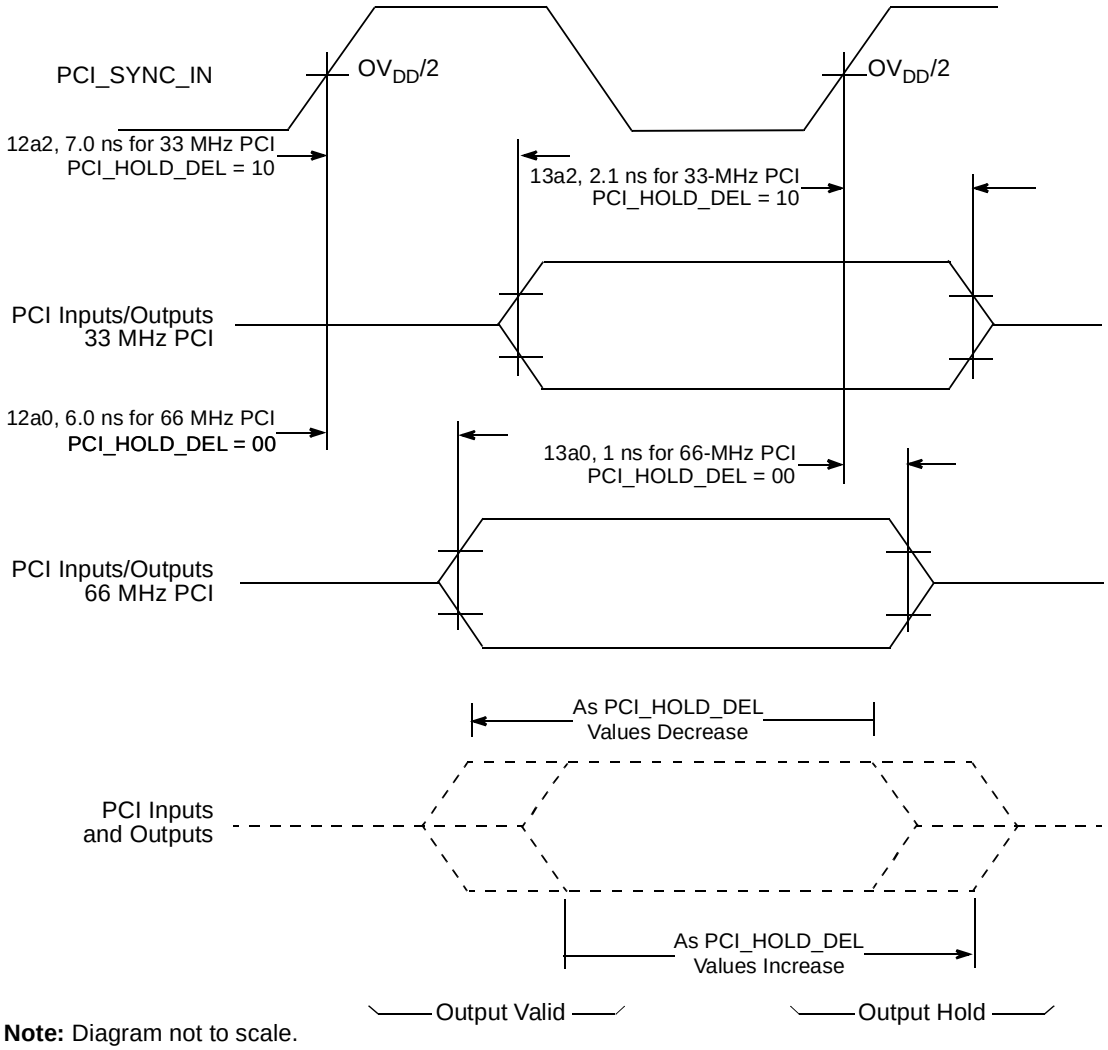


Figure 8. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

Figure 15 provides the PCI_HOLD_DEL effect on output valid and hold times.



Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Times

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8245.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low-level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

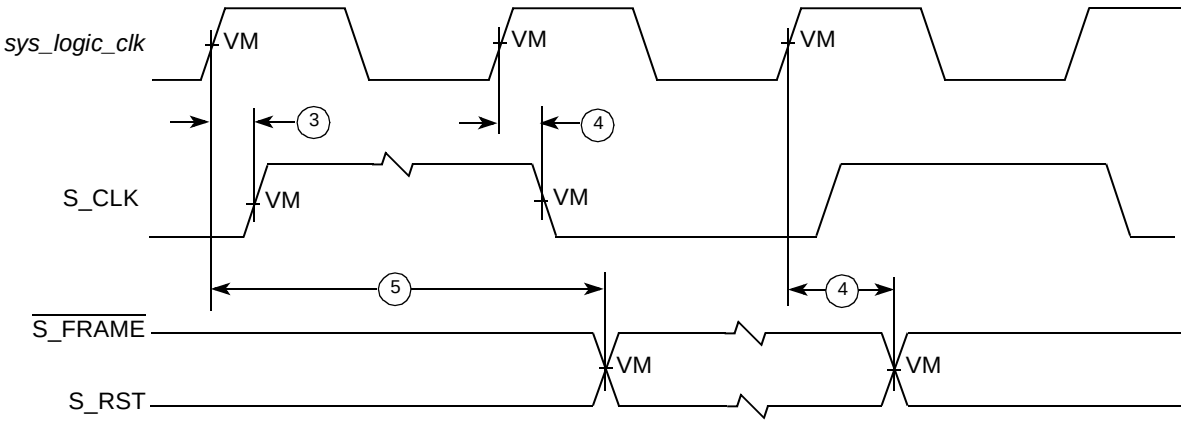


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

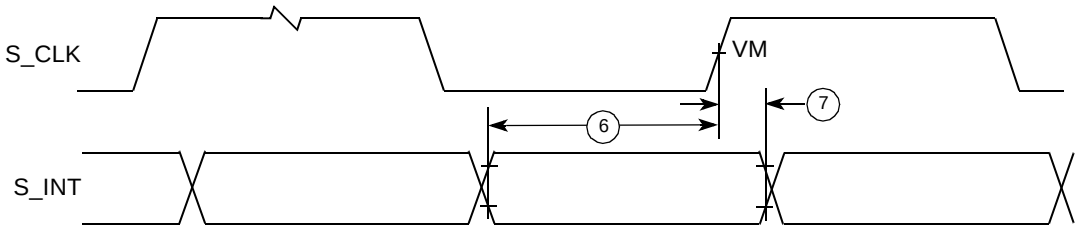


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.8 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8245 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.5 V	20	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DQM[0:7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{CS}$[0:7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{FOE}$	H1	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS0}$	N4	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS1}$	N2	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{RCS2}$/TRIG_IN	AF20	I/O	OV_{DD}	6 ohms	10, 14
$\overline{RCS3}$/TRIG_OUT	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
SDMA[1:0]	W1 W2	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4, 6
SDMA[11:2]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{DRDY}$	B20	Input	OV_{DD}	—	9, 10
SDMA12/$\overline{SRESET}$	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA13/TBEN	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA14/ $\overline{CHKSTOP\_IN}$	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDBA1	P1	Output	GV_{DD}	DRV_MEM_CTRL	
SDBA0	P2	Output	GV_{DD}	DRV_MEM_CTRL	
PAR[0:7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GV_{DD}	DRV_STD_MEM	6
$\overline{SDRAS}$	AD1	Output	GV_{DD}	DRV_MEM_CTRL	3
$\overline{SDCAS}$	AD2	Output	GV_{DD}	DRV_MEM_CTRL	3
CKE	H2	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{WE}$	AA1	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{AS}$	Y1	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
PIC Control Signals					
IRQ0/S_INT	C19	Input	OV_{DD}	—	
IRQ1/S_CLK	B21	I/O	OV_{DD}	DRV_PCI	
IRQ2/S_RST	AC22	I/O	OV_{DD}	DRV_PCI	
IRQ3/$\overline{S\_FRAME}$	AE24	I/O	OV_{DD}	DRV_PCI	
IRQ4/$\overline{L\_INT}$	A23	I/O	OV_{DD}	DRV_PCI	
I^2C Control Signals					
SDA	AE20	I/O	OV_{DD}	DRV_STD_MEM	10, 16
SCL	AF21	I/O	OV_{DD}	DRV_STD_MEM	10, 16

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DUART Control Signals					
SOUT1/PCI_CLK0	AC25	Output	GV_{DD}	DRV_MEM_CTRL	13, 14
SIN1/PCI_CLK1	AB25	I/O	GV_{DD}	DRV_MEM_CTRL	13, 14, 26
SOUT2/$\overline{\text{RTS1}}$/ PCI_CLK2	AE26	Output	GV_{DD}	DRV_MEM_CTRL	13, 14
SIN2/$\overline{\text{CTS1}}$/ PCI_CLK3	AF25	I	GV_{DD}	DRV_MEM_CTRL	13, 14, 26
Clock-Out Signals					
PCI_CLK0/SOUT1	AC25	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_CLK1/SIN1	AB25	Output	GV_{DD}	DRV_PCI_CLK	13, 14, 26
PCI_CLK2/$\overline{\text{RTS1}}$/ SOUT2	AE26	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_CLK3/$\overline{\text{CTS1}}$/ SIN2	AF25	Output	GV_{DD}	DRV_PCI_CLK	13, 14, 26
PCI_CLK4/DA3	AF26	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_SYNC_OUT	AD25	Output	GV_{DD}	DRV_PCI_CLK	
PCI_SYNC_IN	AB23	Input	GV_{DD}	—	
SDRAM_CLK [0:3]	D1 G1 G2 E1	Output	GV_{DD}	DRV_MEM_CTRL or DRV_MEM_CLK	6, 21
SDRAM_SYNC_OUT	C1	Output	GV_{DD}	DRV_MEM_CTRL or DRV_MEM_CLK	21
SDRAM_SYNC_IN	H3	Input	GV_{DD}	—	
CKO/DA1	B15	Output	OV_{DD}	DRV_STD_MEM	14
OSC_IN	AD21	Input	OV_{DD}	—	19
Miscellaneous Signals					
$\overline{\text{HRST\_CTRL}}$	A20	Input	OV_{DD}	—	27
$\overline{\text{HRST\_CPU}}$	A19	Input	OV_{DD}	—	27
$\overline{\text{MCP}}$	A17	Output	OV_{DD}	DRV_STD_MEM	3, 4, 17
NMI	D16	Input	OV_{DD}	—	
$\overline{\text{SMI}}$	A18	Input	OV_{DD}	—	10
$\overline{\text{SRESET}}$/SDMA12	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TBEN/SDMA13	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
$\overline{\text{QACK}}$/DA0	F2	Output	OV_{DD}	DRV_STD_MEM	4, 14, 25
$\overline{\text{CHKSTOP\_IN}}$/ SDMA14	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TRIG_IN/$\overline{\text{RCS2}}$	AF20	I/O	OV_{DD}	—	10, 14
TRIG_OUT/$\overline{\text{RCS3}}$	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
MAA[0:2]	AF2 AF1 AE1	Output	GV_{DD}	DRV_STD_MEM	3, 4, 6
$\overline{\text{MIV}}$	A16	Output	OV_{DD}	—	24
PMAA[0:1]	AD18 AF18	Output	OV_{DD}	DRV_STD_MEM	3, 4, 6, 15
PMAA[2]	AE19	Output	OV_{DD}	DRV_STD_MEM	4, 6, 15
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
$\overline{\text{TEST0}}$	AD22	Input	OV_{DD}	—	1, 9
RTC	Y2	Input	GV_{DD}	—	11
TCK	AF22	Input	OV_{DD}	—	9, 12
TDI	AF23	Input	OV_{DD}	—	9, 12
TDO	AC21	Output	OV_{DD}	—	24
TMS	AE22	Input	OV_{DD}	—	9, 12
$\overline{\text{TRST}}$	AE23	Input	OV_{DD}	—	9, 12
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground	—	—	
LV_{DD}	AC20 AC23 D20 D23 G23 P23 Y23	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	
GV_{DD}	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for memory drivers 3.3 V	GV_{DD}	—	
OV_{DD}	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3 V	OV_{DD}	—	

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
V_{DD}	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for core 1.8/2.0 V	V_{DD}	—	22
No Connect	D17	—	—	—	23
AV_{DD}	C17	Power for PLL (CPU core logic) 1.8/2.0 V	AV_{DD}	—	22
$AV_{DD}2$	AF24	Power for PLL (peripheral logic) 1.8/2.0 V	$AV_{DD}2$	—	22
Debug/Manufacturing Pins					
DA0/$\overline{\text{QACK}}$	F2	Output	OV_{DD}	DRV_STD_MEM	4, 10, 25
DA1/CKO	B15	Output	OV_{DD}	DRV_STD_MEM	14
DA2	C25	Output	OV_{DD}	DRV_PCI	2
DA3/PCI_CLK4	AF26	Output	GV_{DD}	DRV_PCI_CLK	14
DA4/$\overline{\text{REQ4}}$	Y26	I/O	OV_{DD}	—	12, 14
DA5/$\overline{\text{GNT4}}$	W26	Output	OV_{DD}	DRV_PCI	7, 15, 14
DA[10:6]/ PLL_CFG[0:4]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
DA[11]	AD26	Output	OV_{DD}	DRV_PCI	2
DA[12:13]	AF17 AF19	Output	OV_{DD}	DRV_STD_MEM	2, 6

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DA[14:15]	F1 J2	Output	GV_{DD}	DRV_MEM_CTRL	2, 6

Notes:

1. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
2. Treat these pins as no connects (NC) unless debug address functionality is used.
3. This pin has an internal pull-up resistor that is enabled only in the reset state. The value of the internal pull-up resistor is not guaranteed but is sufficient to ensure that a logic 1 is read into configuration bits during reset if the signal is left unterminated.
4. This pin is a reset configuration pin.
5. DL[0] is a reset configuration pin with an internal pull-up resistor that is enabled only in the reset state. The value of the internal pull-up resistor is not guaranteed but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
6. Multi-pin signals such as AD[31:0] and MDL[0:31] have their physical package pin numbers listed in an order corresponding to the signal names. Example: AD0 is on pin C22, AD1 is on pin D22, ..., AD31 is on pin V25.
7. $\overline{\text{GNT4}}$ is a reset configuration pin with an internal pull-up resistor that is enabled only in the reset state.
8. A weak pull-up resistor (2–10 kΩ) should be placed on this PCI control pin to LV_{DD}.
9. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
10. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
11. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to GV_{DD}.
12. This pin has an internal pull-up resistor that is enabled at all times. The value of the internal pull-up resistor is not guaranteed but is sufficient to prevent unused inputs from floating.
13. An external PCI clocking source or fan-out buffer may be required for the MPC8245 DUART functionality since PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
14. This pin is a multiplexed signal and appears more than once in this table.
15. This pin is affected by the programmable PCI_HOLD_DEL parameter.
16. This pin is an open-drain signal.
17. This pin can be programmed as driven (default) or as open-drain (in MIOCR 1).
18. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification.*
19. OSC_IN uses the 3.3-V PCI interface driver, which is 5-V tolerant. See Table 2 for details.
20. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.
21. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev 1.1 (A). These signals use DRV_MEM_CLK for chip Rev 1.2 (B).
22. The 266- and 300-MHz part offerings can run at a source voltage of 1.8 ± 100 mV or 2.0 ± 100 mV. Source voltage should be 2.0 ± 100 mV for 333- and 350-MHz parts.
23. This pin is LAVDD on the MPC8240. It is an NC on the MPC8245, which should not pose a problem when an MPC8240 is replaced with an MPC8245.
24. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.
25. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD} so that a 1 can be detected at reset if an external memory clock is not used and PLL[0:4] does not select a half-clock frequency ratio.
26. Typically, the serial port has sufficient drivers in the RS232 transceiver to drive the $\overline{\text{CTS}}$ pin actively as an input. No pullups are needed in this case.
27. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state

7.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Tie unused active-low inputs to OV_{DD}. Connect unused active-high inputs tie to GND. All NC signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND pins.

The PCI_SYNC_OUT signal is to be routed halfway out to the PCI devices and returned to the PCI_SYNC_IN input of the MPC8245.

The SDRAM_SYNC_OUT signal is to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8245. The trace length can be used to skew or adjust the timing window as needed. See the Tundra *Tsi107™ Design Guide* (AN1849) and Freescale application notes AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1* and AN2746, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part* 2 for details. Note that there is an SDRAM_SYNC_IN to PCI_SYNC_IN time requirement (refer to Table 10 for the input AC timing specifications).

7.4 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) are disabled, and their outputs drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to OV_{DD}.

RTC should have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}.

The following signals should be pulled up to OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP\_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, $\overline{\text{INTA}}$, $\overline{\text{QACK}}$/DA0 and $\overline{\text{DRDY}}$. Note that $\overline{\text{QACK}}$/DA0 should be left without a pull-up resistor only if an external clock is used because this signal enables internal clock flipping logic when it is low on reset, which is necessary when the PLL[0:4] signals select a half-clock frequency ratio and an external PLL is used to drive the SDRAM device.

It is recommended that the following PCI control signals be pulled up to LV_{DD} (the clamping voltage) with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16.

The following pins have internal pull-up resistors enabled only while device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], and PMAA[0:2]. See Table 16.

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

7.8 Thermal Management

This section provides thermal management information for the tape ball grid array (TBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, heat sinks may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly. Figure 27 displays a package-exploded cross-sectional view of a TBGA package with several heat sink options.

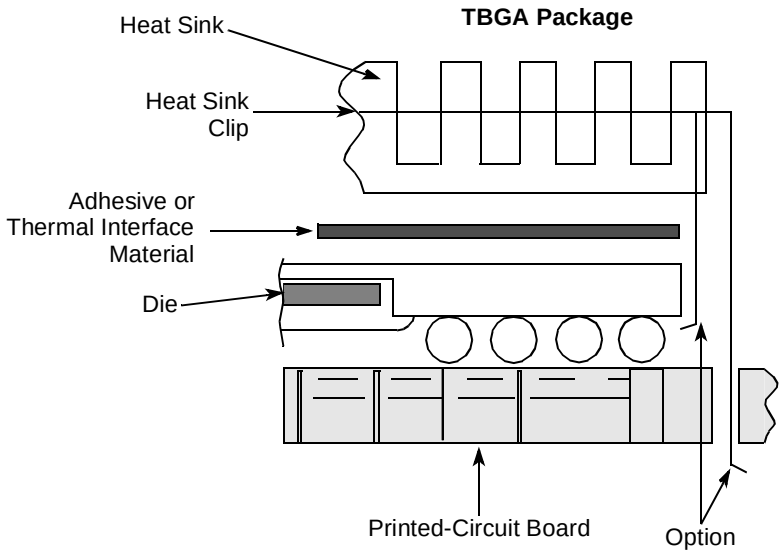


Figure 27. Package-Exploded Cross-Sectional View with Several Heat Sink Options

Figure 28 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the TBGA package, and there exists high board-level thermal loading from adjacent components.
- A heat sink is not attached to the TBGA package, and there is low board-level thermal loading from adjacent components.
- A heat sink (for example, ChipCoolers) is attached to the TBGA package, and there is high board-level thermal loading from adjacent components.
- A heat sink (for example, ChipCoolers) is attached to the TBGA package, and there is low board-level thermal loading from adjacent components.

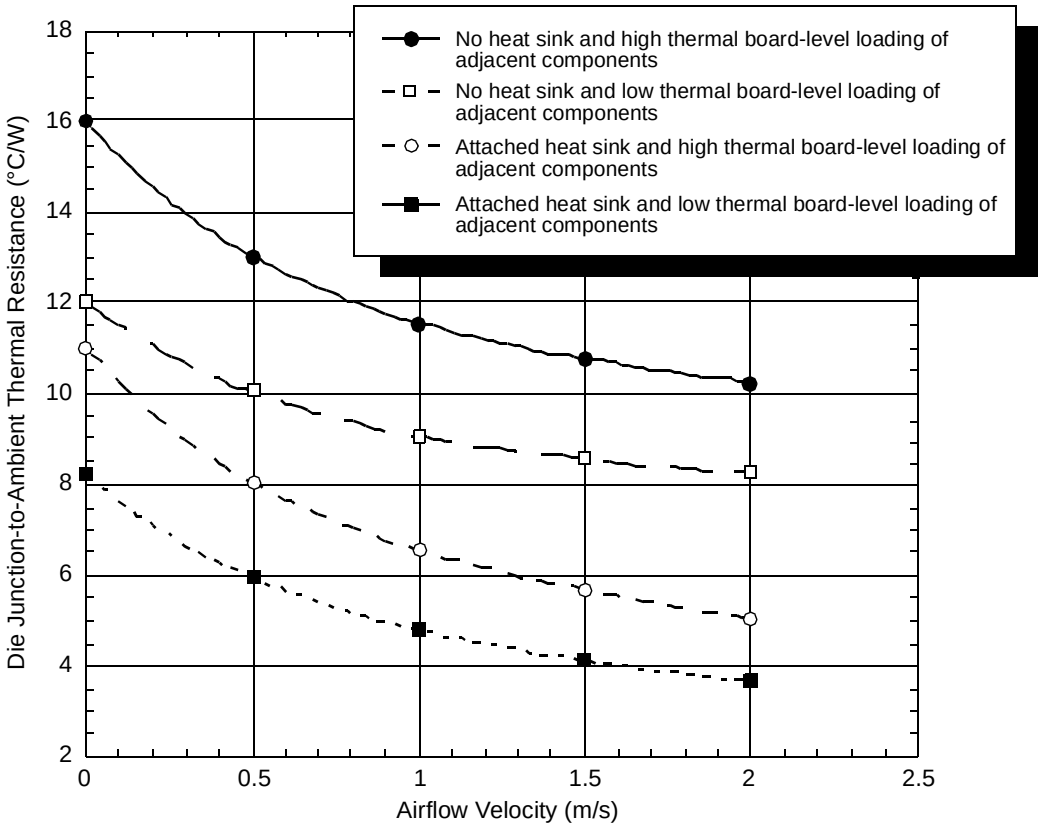


Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances and may or may not need airflow.

7.8.1 Internal Package Conduction Resistance

The intrinsic conduction thermal resistance paths for the TBGA cavity-down packaging technology shown in Figure 29 are as follows:

- Die junction-to-case thermal resistance
- Die junction-to-ball thermal resistance

Figure 29 depicts the primary heat transfer path for a package with an attached heat sink mounted on a printed-circuit board.

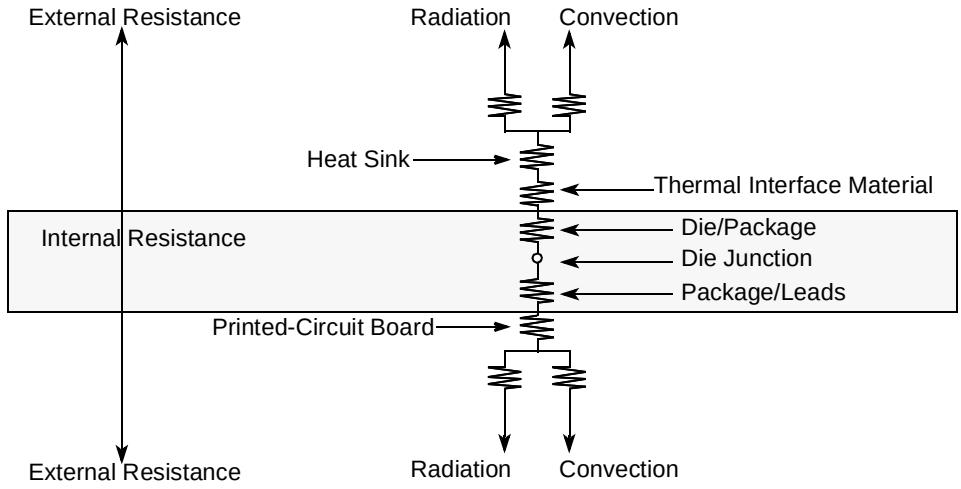


Figure 29. TBGA Package with Heat Sink Mounted to a Printed-Circuit Board

In a TBGA package, the active side of the die faces the printed-circuit board. Most of the heat travels through the die, across the die attach layer, and into the copper spreader. Some of the heat is removed from the top surface of the spreader through convection and radiation. Another percentage of the heat enters the printed-circuit board through the solder balls. The heat is then removed from the exposed surfaces of the board through convection and radiation. If a heat sink is used, a larger percentage of heat leaves through the top side of the spreader.

7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material placed between the top of the package and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 30 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 30). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

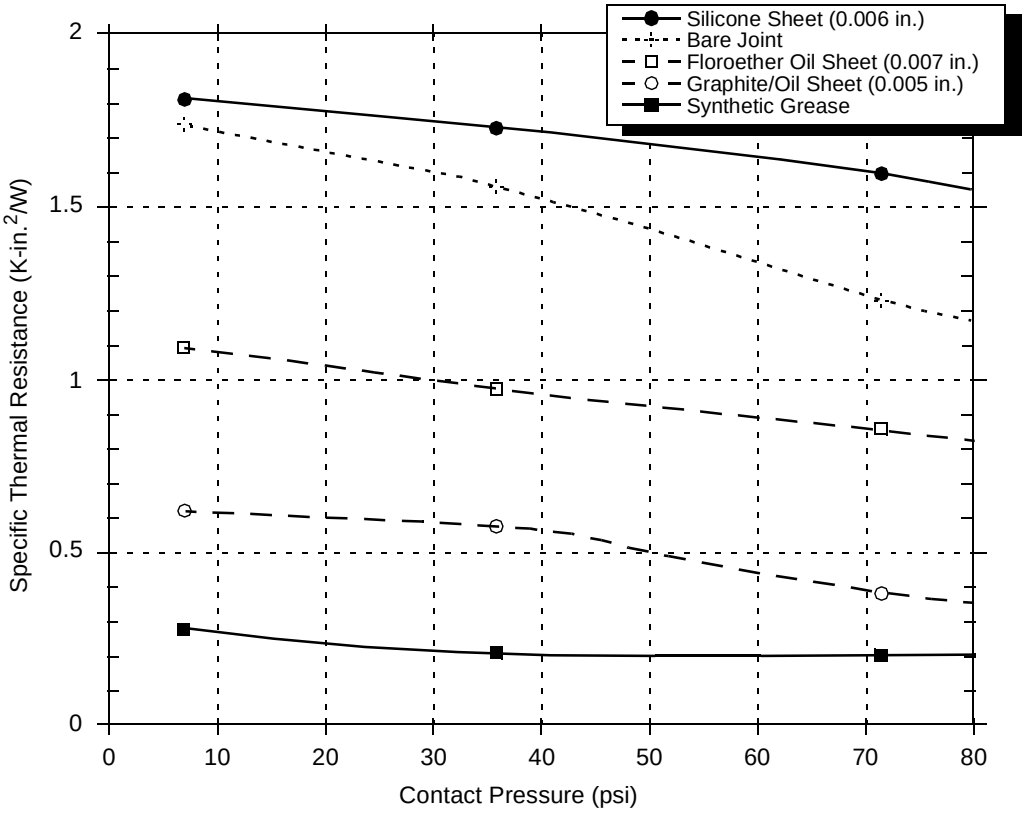


Figure 30. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.1	—	Made $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V ± 100 mV information for 133-MHz memory interface operation to Section 1.3, Table 2, Table 5, Table 9, Table 17, and Section 1.7.2. Pin D17, formerly LAV_{DD} (supply voltage for DLL), is a NC on the MPC8245 since the DLL voltage is supplied internally. Eliminated all references to LAV_{DD}; updated Section 1.7.1. Previous Note 4 of Table 2 did not apply to the MPC8245 (MPC8240 document legacy). New Note 4 added in reference to maximum CPU speed at reduced V_{DD} voltage. Updated the Programmable Output Impedance of DEV_MEM_ADDR in Table 4 to 6 Ω to reflect characterization data. Updated Table 5 to reflect reduced power consumption when operating $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V ± 100 mV. Changed Notes 2, 3, and 4 to reflect V_{DD} at 1.9 V. Changed Note 5 to represent $V_{DD} = AV_{DD}$ = 1.8 V. Updated Table 7 to reflect $V_{DD}/AV_{DD}/AV_{DD}2$ voltage level operating frequency dependencies; changed 250 MHz device column to 266 MHz; modified Note 1 eliminating VCO references; added Note 2. Changed 250 MHz processor frequency offering to 266 MHz. Changed Spec 12b for memory output valid time in Table 11 from 5.5 ns to 4.5 ns; this is a key specification change to enable 133-MHz memory interface designs. Updated Pinout Table 16 with the following changes: • Pin types for $\overline{\text{RCS0}}$, $\overline{\text{RCS3}}$/TRIG_OUT and DA[11:15] were erroneously listed as I/O, changed Pin Types to Output. • Pin types for $\overline{\text{REQ}}$4/DA4, $\overline{\text{RCS2}}$/TRIG_IN, and PLL_CFG[0:4]/DA[10:6] were erroneously listed as Input, changed Pin Types to I/O. • Changed Pin D17 from LAV_{DD} to No Connect; deleted Note 21 and references. • Notes 3, 5, and 7 contained references to the MPC8240 (MPC8240 document legacy); changed these references to MPC8245. • Previous Notes 13 and 14 did not apply to the MPC8245 (MPC8240 document legacy), these notes were deleted; moved Note 19 to become new Note 13; moved Note 20 to become new Note 14; updated associated references. • Added Note 3 to SDMA[1:0] signals about internal pull-up resistors during reset state. • Reversed vector ordering for the PCI Interface Signals: $\overline{\text{C/BE}}$[0:3] changed to $\overline{\text{C/BE}}$[3:0], AD[0:31] changed to AD[31:0], $\overline{\text{GNT}}$[0:3] changed to $\overline{\text{GNT}}$[3:0], and $\overline{\text{REQ}}$[0:3] changed to $\overline{\text{REQ}}$[3:0]. The package pin number orderings were also reversed meaning that pin functionality did NOT change. For example, AD0 is still on signal C22, AD1 is still on signal D22,..., AD31 is still on signal V25. This change was made to make the vectored PCI signals in this hardware specification consistent with the *PCI Local Bus Specification* and the *MPC8245 Integrated Processor Reference Manual* vector ordering. • Changed $\overline{\text{TEST1}}/\overline{\text{DRDY}}$ signal on pin B20 to $\overline{\text{DRDY}}$. • Changed $\overline{\text{TEST2}}$ signal on pin Y2 to RTC for performance monitor use. Updated PLL Table 17 with the following changes for 133-MHz memory interface operation: • Added Ref. 9 (01001) and Ref. 17 (10111) details; removed these settings from Note 10 (reserved settings list). • Enhanced range of Ref. 10 (10000). • Updated Note 13, changed bits 16–20 erroneous information to correct bits 23–19. • Added Notes 16 and 17. Added information to Section 1.7.8 in reference to $\overline{\text{CHKSTOP\_IN}}$ and $\overline{\text{SRESET}}$ being unavailable in extended ROM mode.
0.0	—	Initial release.

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