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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8245lzu333d

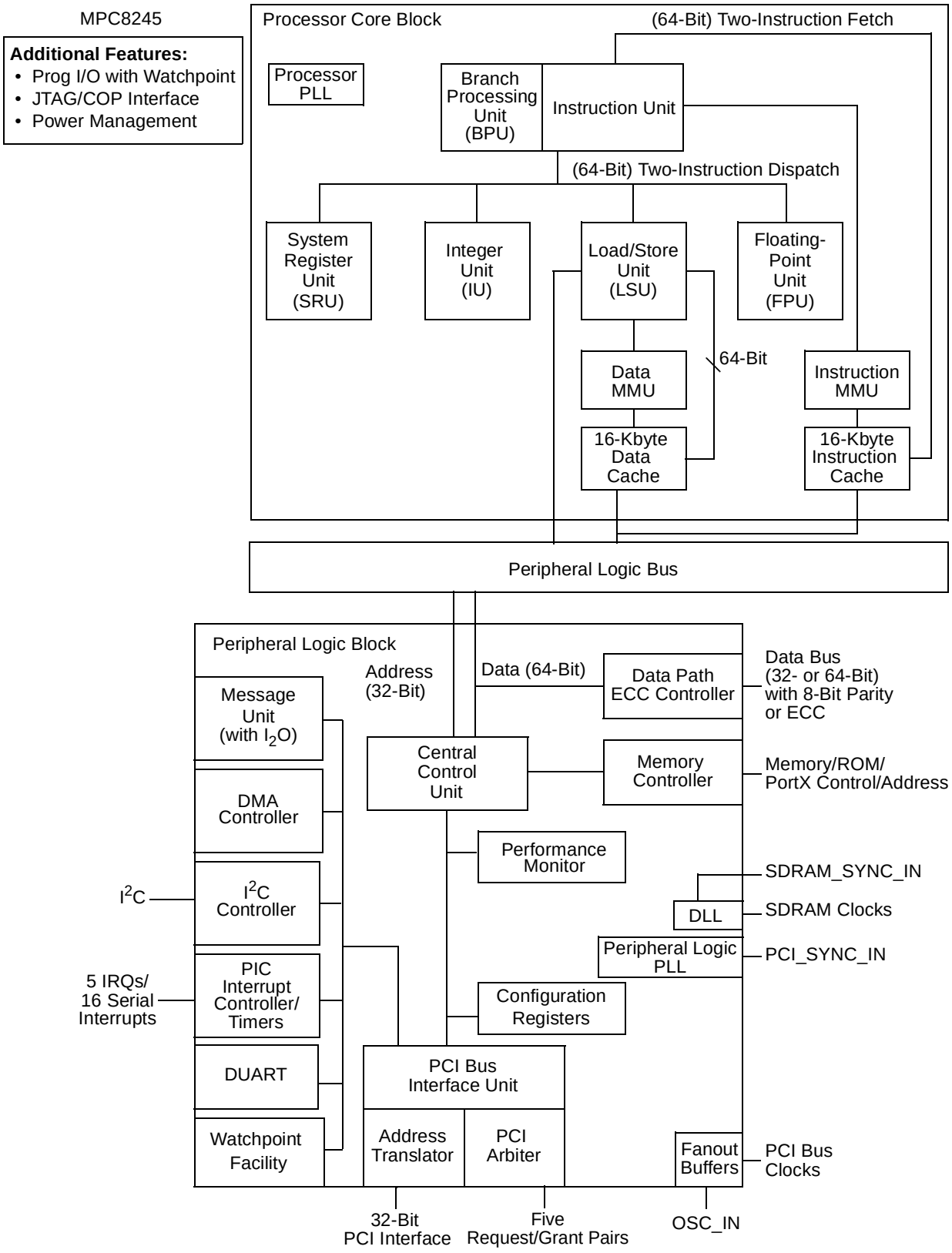
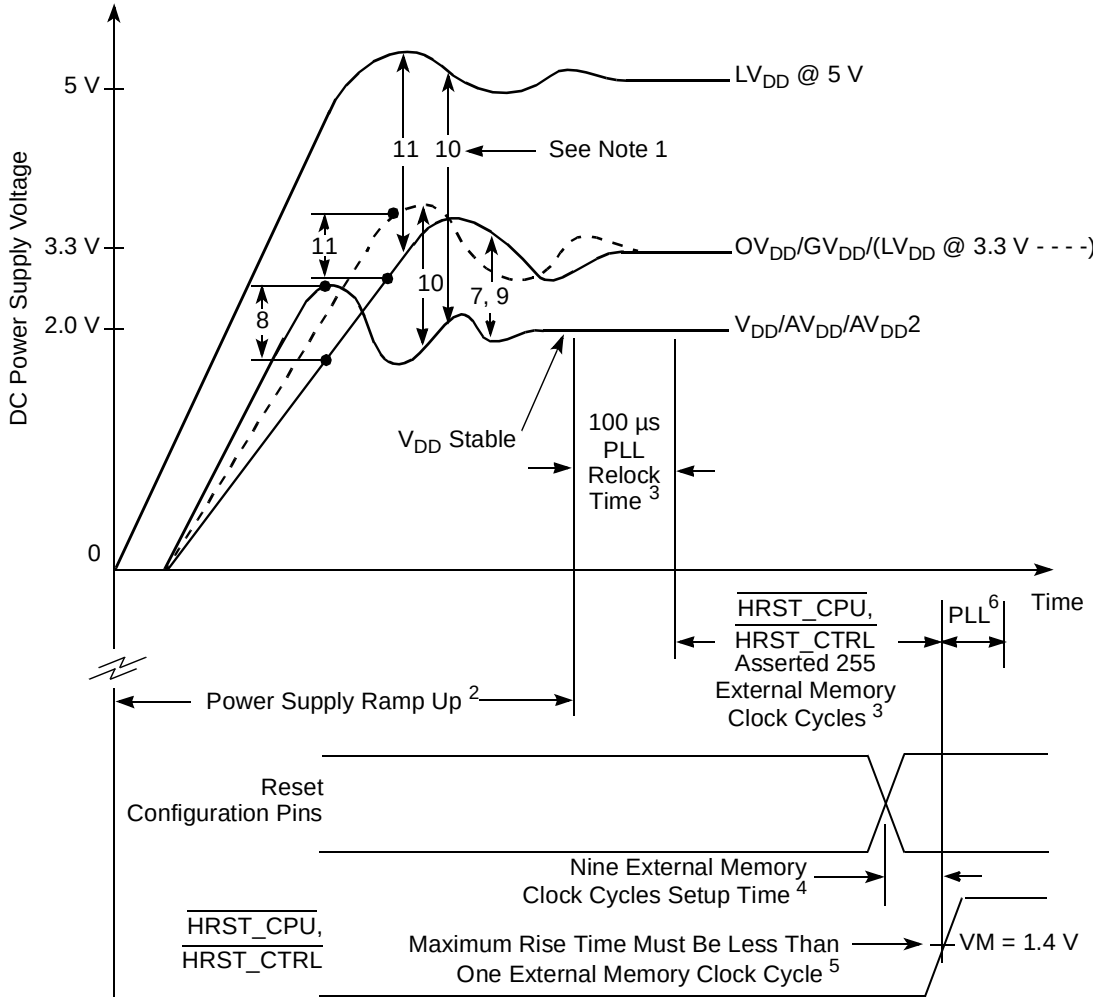


Figure 1. MPC8245 Block Diagram

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. See Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for additional information on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface.

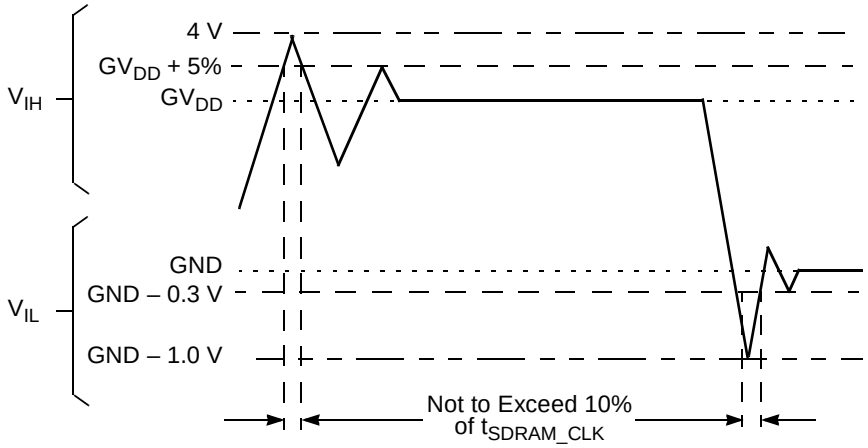


Figure 3. Overshoot/Undershoot Voltage

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the PCI interface for the 3.3- and 5-V signals, respectively.

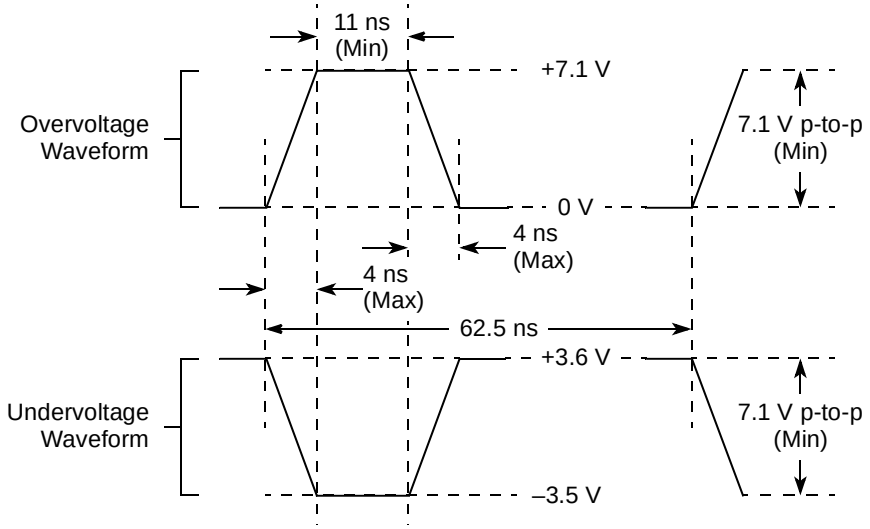


Figure 4. Maximum AC Waveforms for 3.3-V Signaling

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL; that is, the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Note that keeping a DLL mode that is locked below tap point decimal 12 is not recommended.

Figure 13 shows the input timing diagram for mode select signals.

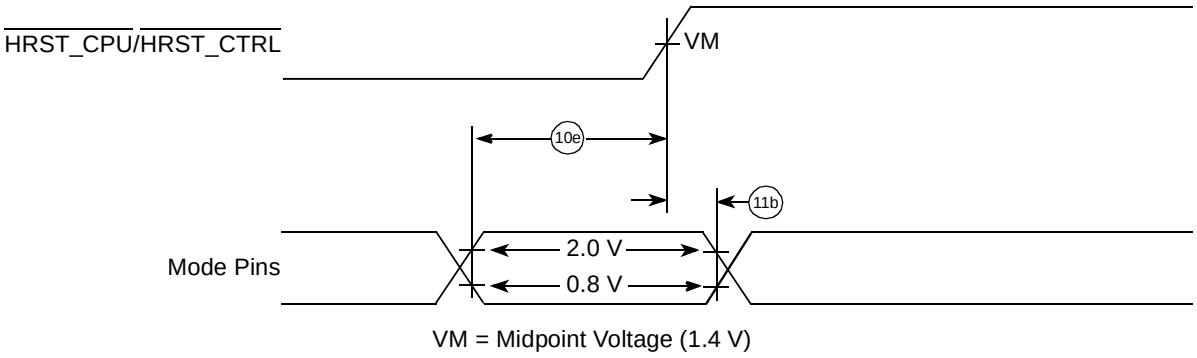


Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 for the input/output timing diagram referenced to *sys_logic_clk*. All output timings assume a purely resistive 50-Ω load (see Figure 14 for the AC test load for the MPC8245). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths indicated in Table 4.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory control, address, and data signals)	—	4.0	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/PortX)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66-MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33-MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	*sys_logic_clk* to output high impedance (for all others)	—	4.0	ns	2

Notes:

1. All PCI signals are measured from $GV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times OV_{DD}$ or $0.615 \times OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[3:0], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[31:0], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], IDSEL, and $\overline{\text{INTA}}$.
4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8245 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals; the values on these two signals are inverted and stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Since $\overline{\text{MCP}}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. Figure 15 shows the PCI_HOLD_DEL effect on output valid and hold times.

Figure 14 provides the AC test load for the MPC8245.

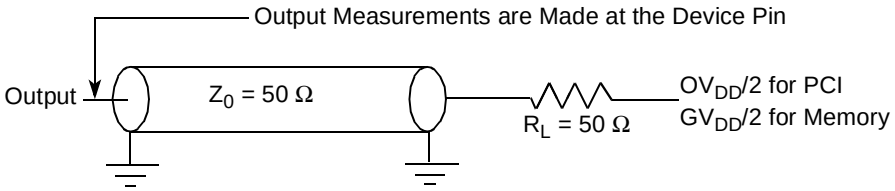


Figure 14. AC Test Load for the MPC8245

Table 13. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8245 provides a delay time of at least 300 ns for the SDA signal (referred to as the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the MPC8245acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA is balanced, the MPC8245 does not cause the unintended generation of a Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8245 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved. It is assumed that the desired I²C SCL clock frequency is 400 KHz and the digital filter sampling rate register (DFFSR bits in I2CFDR) is programmed with its default setting of 0x10 (decimal 16):

SDRAM Clock Frequency	100 MHz	133 MHz
FDR Bit Setting	0x00	0x2A
Actual FDR Divider Selected	384	896
Actual I²C SCL Frequency Generated	260.4 KHz	148.4 KHz

   For details on I²C frequency calculation, refer to the application note AN2919 “Determining the I²C Frequency Divider Ratio for SCL”.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design.

Figure 16 provides the AC test load for the I²C.

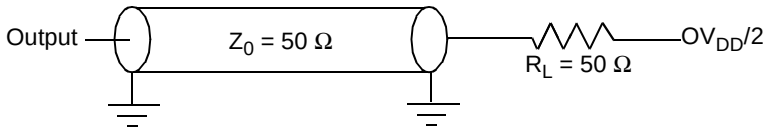


Figure 16. I²C AC Test Load

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN) (continued)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams.

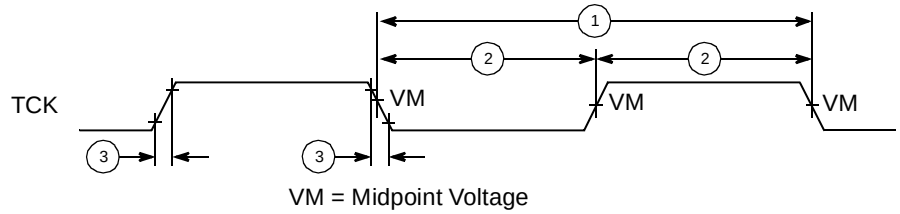


Figure 20. JTAG Clock Input Timing Diagram

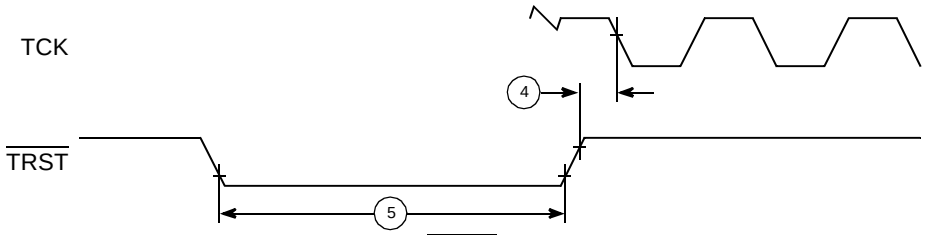


Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

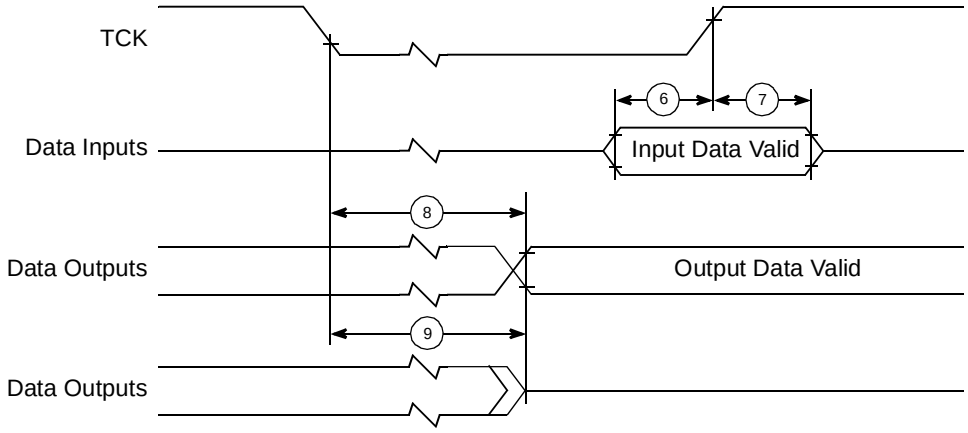


Figure 22. JTAG Boundary Scan Timing Diagram

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DQM[0:7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{CS}$[0:7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{FOE}$	H1	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS0}$	N4	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS1}$	N2	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{RCS2}$/TRIG_IN	AF20	I/O	OV_{DD}	6 ohms	10, 14
$\overline{RCS3}$/TRIG_OUT	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
SDMA[1:0]	W1 W2	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4, 6
SDMA[11:2]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{DRDY}$	B20	Input	OV_{DD}	—	9, 10
SDMA12/$\overline{SRESET}$	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA13/TBEN	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA14/ $\overline{CHKSTOP\_IN}$	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDBA1	P1	Output	GV_{DD}	DRV_MEM_CTRL	
SDBA0	P2	Output	GV_{DD}	DRV_MEM_CTRL	
PAR[0:7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GV_{DD}	DRV_STD_MEM	6
$\overline{SDRAS}$	AD1	Output	GV_{DD}	DRV_MEM_CTRL	3
$\overline{SDCAS}$	AD2	Output	GV_{DD}	DRV_MEM_CTRL	3
CKE	H2	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{WE}$	AA1	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{AS}$	Y1	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
PIC Control Signals					
IRQ0/S_INT	C19	Input	OV_{DD}	—	
IRQ1/S_CLK	B21	I/O	OV_{DD}	DRV_PCI	
IRQ2/S_RST	AC22	I/O	OV_{DD}	DRV_PCI	
IRQ3/$\overline{S\_FRAME}$	AE24	I/O	OV_{DD}	DRV_PCI	
IRQ4/$\overline{L\_INT}$	A23	I/O	OV_{DD}	DRV_PCI	
I^2C Control Signals					
SDA	AE20	I/O	OV_{DD}	DRV_STD_MEM	10, 16
SCL	AF21	I/O	OV_{DD}	DRV_STD_MEM	10, 16

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
V_{DD}	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for core 1.8/2.0 V	V_{DD}	—	22
No Connect	D17	—	—	—	23
AV_{DD}	C17	Power for PLL (CPU core logic) 1.8/2.0 V	AV_{DD}	—	22
$AV_{DD}2$	AF24	Power for PLL (peripheral logic) 1.8/2.0 V	$AV_{DD}2$	—	22
Debug/Manufacturing Pins					
DA0/$\overline{\text{QACK}}$	F2	Output	OV_{DD}	DRV_STD_MEM	4, 10, 25
DA1/CKO	B15	Output	OV_{DD}	DRV_STD_MEM	14
DA2	C25	Output	OV_{DD}	DRV_PCI	2
DA3/PCI_CLK4	AF26	Output	GV_{DD}	DRV_PCI_CLK	14
DA4/$\overline{\text{REQ4}}$	Y26	I/O	OV_{DD}	—	12, 14
DA5/$\overline{\text{GNT4}}$	W26	Output	OV_{DD}	DRV_PCI	7, 15, 14
DA[10:6]/ PLL_CFG[0:4]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
DA[11]	AD26	Output	OV_{DD}	DRV_PCI	2
DA[12:13]	AF17 AF19	Output	OV_{DD}	DRV_STD_MEM	2, 6

6 PLL Configurations

The internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (266- and 300-MHz Parts)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–35[5]	75–105	188–263	25–40[5,7]	75–120	188–300	3 (2)	2.5 (2)
1	00001[12]	25–29[5]	75–88	225–264	25–33[5]	75–99	225–297	3 (2)	3 (2)
2	00010[11]	50[18]–59[5,7]	50–59	225–266	50[18]–66[1]	50–66	225–297	1 (4)	4.5 (2)
3	00011[11,14]	50[17]–66[1]	50–66	100–133	50[17]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100[12]	25–46[4]	50–92	100–184	25–46[4]	50–92	100–184	2 (4)	2 (4)
6	00110[15]	Bypass			Bypass			Bypass	
7 Rev B	00111[14]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (Bypass)	3 (2)
7 Rev D	00111[14]	Not available							
8	01000[12]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (4)	3 (2)
9	01001[12]	45[6]–66[1]	90–132	180–264	45[6]–66[1]	90–132	180–264	2 (2)	2 (2)
A	01010[12]	25–29[5]	50–58	225–261	25–33[5]	50–66	225–297	2 (4)	4.5 (2)
B	01011[12]	45[3]–59[5]	68–88	204–264	45[3]–66[1]	68–99	204–297	1.5 (2)	3 (2)
C	01100[12]	36[6]–46[4]	72–92	180–230	36[6]–46[4]	72–92	180–230	2 (4)	2.5 (2)
D	01101[12]	45[3]–50[5]	68–75	238–263	45[3]–57[5]	68–85	238–298	1.5 (2)	3.5 (2)
E	01110[12]	30[6]–44[5]	60–88	180–264	30[6]–46[4]	60–92	180–276	2 (4)	3 (2)
F	01111[12]	25[5]	75	263	25–28[5]	75–85	263–298	3 (2)	3.5 (2)
10	10000[12]	30[6]–44[2,5]	90–132	180–264	30[6]–44[2]	90–132	180–264	3 (2)	2 (2)
11	10001[12]	25–26[5,7]	100–106	250–266	25–29[2]	100–116	250–290	4 (2)	2.5 (2)
12	10010[12]	60[6]–66[1]	90–99	180–198	60[6]–66[1]	90–99	180–198	1.5 (2)	2 (2)

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Not usable			Off	Off

Notes:

1. Limited by the maximum PCI input frequency (66 MHz).
2 Limited by the maximum system memory interface operating frequency (100 MHz @ 300 MHz CPU).
3. Limited by the minimum memory VCO frequency (133 MHz).
4. Limited due to the maximum memory VCO frequency (372 MHz).
5. Limited by the maximum CPU operating frequency.
6. Limited by the minimum CPU VCO frequency (360 MHz).
7. Limited by the maximum CPU VCO frequency (maximum marked CPU speed X 2).
8. In clock-off mode, no clocking occurs inside the MPC8245, regardless of the PCI_SYNC_IN input.
9. Range values are rounded down to the nearest whole number (decimal place accuracy removed).
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting differ from the MPC8240 and are not backward-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting differs from or does not exist on the MPC8240 and may not be fully backward-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
16. Limited by the maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).
17. Limited by the minimum CPU operating frequency (100 MHz).
18. Limited by the minimum memory bus frequency (50 MHz).

Table 18. PLL Configurations (333- and 350-MHz Parts)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–44[16]	75–132	188–330	25–44[16]	75–132	188–330	3 (2)	2.5 (2)
1	00001[12]	25–37[5,7]	75–111	225–333	25–38[5]	75–114	225–342	3 (2)	3 (2)

Table 18. PLL Configurations (333- and 350-MHz Parts) (continued)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1E Rev B	11110[8]	Not usable			Not usable			Off	Off
1E Rev D	11110	33[3]–47[5]	66–94	231–329	33[3]–50[2,5,7]	66–100	231–350	2(2)	3.5(2)
1F	11111[8]	Not usable			Not usable			Off	Off

Notes:

1. Limited by the maximum PCI input frequency (66 MHz).
2. Limited by the maximum system memory interface operating frequency (100 MHz @ 350 MHz CPU).
3. Limited by the minimum memory VCO frequency (132 MHz).
4. Limited due to the maximum memory VCO frequency (372 MHz).
5. Limited by the maximum CPU operating frequency.
6. Limited by the minimum CPU VCO frequency (360 MHz).
7. Limited by the maximum CPU VCO frequency (Maximum marked CPU speed X 2).
8. In clock-off mode, no clocking occurs inside the MPC8245, regardless of the PCI_SYNC_IN input.
9. Range values are rounded down to the nearest whole number (decimal place accuracy removed).
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting differ from or do not exist on the MPC8240 and are not backward-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting differs from the MPC8240 and may not be fully backward-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
16. Limited by the maximum system memory interface operating frequency (133 MHz @ 333 MHz CPU).
17. Limited by the minimum CPU operating frequency (100 MHz).
18. Limited by the minimum memory bus frequency (50 MHz).

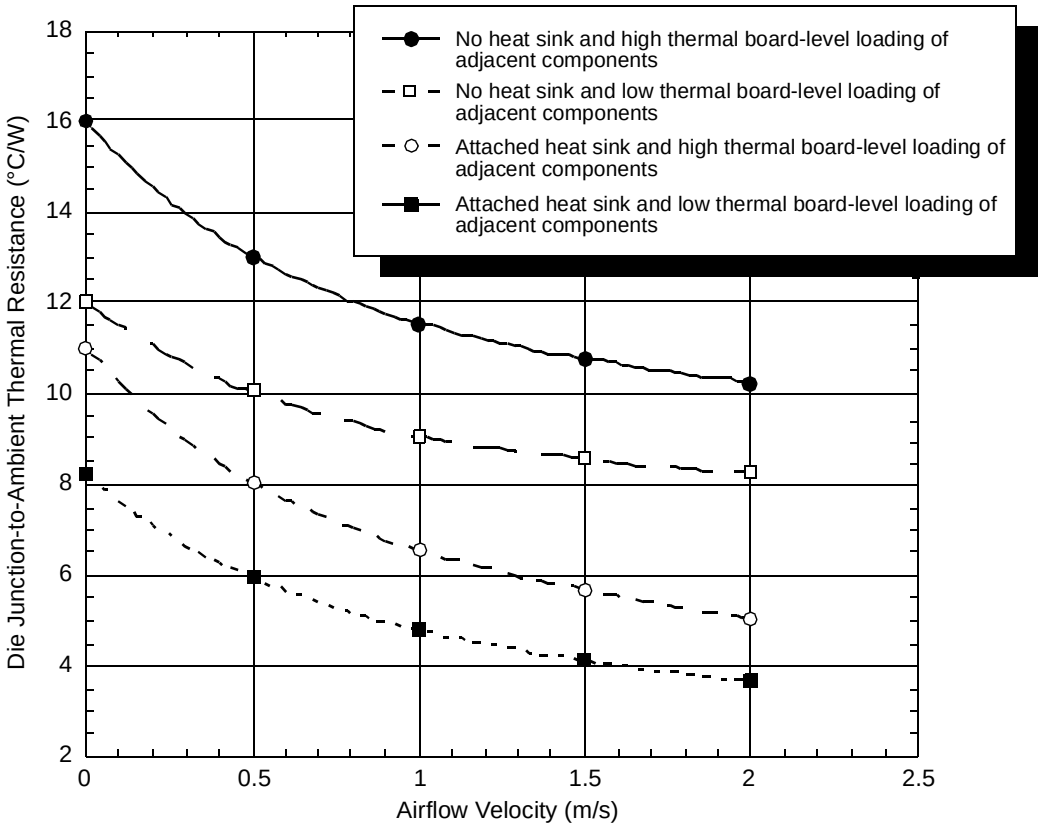


Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

7.8.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application without a heat sink, the thermal characterization parameter (Ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.9 References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

8 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Revision History Table

Revision	Date	Substantive Change(s)
10	8/07	Section 3, Table 3, and Table 7—Changed format of recommended voltage supply values so that delta to the chosen nominal does not exceed ± 100 mV. Completely replaced Section 4.6 with compliant I^2C specifications as with other related integrated processor devices.
9	12/27/05	Document—Added Power Architecture information. Section 4.1—Changed increased absolute maximum range for V_{DD} in Table 1. Updated format of nominal voltage listings in Table 2. Section 9.2—Removed Note 3 from Table 21. Updated back page information.
8	11/15/2005	Document—Imported new template and made minor editorial changes. Removed references to a 466 MHz part since it is not available for new orders. Section 4.3.2—Added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated the section to reflect what we offer for new orders. Section 9.3—Added new section, “Part Marking.” Updated Figure 33 to match with current part marking format.
7	10/07/2004	Section 4.1.2—Table 2: Corrected range of AV_{DD} and $AVDD_2$. Section 9.1—Table 21: Corrected voltage range under Process Descriptor column. Minor reformatting.
6.1	05/24/2004	Section 4.5.3—Table 11: Spec 12b was improved from 4.5 ns to 4.0 ns. This improvement is guaranteed on devices marked after work week (WW) 28 of 2004. A device's work week may be determined from the “YYWW” portion of the devices trace ability code which is marked on the top of the device. So for WW28 in 2004, the device’s YYWW is marked as 0428. For more information refer to Figure 33
6	05/11/2004	Section 4.1.2—Table 2: Corrected range of GV_{DD} to 3.3 ± 5%. Section 4.2.1—Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.5.1—Table 8: Changed the wording description for item 15. Section 4.5.2—Table 10: Changed T_{os} range and wording in note; Figure 11:changed wording for SDRAM_SYNC_IN description relative to T_{OS}. Section 4.5.3—Table 11: Changed timing specification for *sys_logic_clk* to output valid (memory control, address, and data signals).
5.1	—	Section 4.3.1—Table 9: Corrected last row to state the correct description for the bit setting. Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
2	—	Globally changed EPIC to PIC. Section 1.4.1.4—Note 5: Changed register reference from 0x72 to 0x73. Section 1.4.1.5—Table 5: Updated power dissipation numbers based on latest characterization data. Section 1.4.2—Table 6: Updated table to show more thermal specifications. Section 1.4.3—Table 7: Updated minimum memory bus value to 50 MHz. Section 1.4.3.1—Changed equations for DLL locking range based on characterization data. Added updates and reference to AN2164 for note 6. Added table defining Tdp parameters. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Table 10: Changed bit definitions for tap points. Updated note on Tos and added reference to AN2164 for note 7. Updated Figure 9 to show significance of Tos. Section 1.4.3.4—Added column for SDRAM_CLK @ 133 MHz Sections 1.5.1 and 1.5.2—Corrected packaging information to state TBGA packaging. Section 1.5.3—Corrected some signals in Table 16 which were missing overbars in the Rev 1.0 release of the document. Section 1.6—Updated Note 10 of Tables 18 and 19. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.9—Updated format of tables in Ordering Information section.
1	—	Updated document template. Section 1.4.1.4—Changed the driver type names in Table 6 to match with the names used in the MPC8245 Reference Manual. Section 1.5.3—Updated driver type names for signals in Table 16 to match with names used in the MPC8245 Integrated Processor Reference Manual. Section 1.4.1.2—Updated Table 7 to refer to new PLL Tables for VCO limits. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid timing. Section 1.5.1—Updated solder balls information to 62Sn/36PB/2Ag. Section 1.6—Updated PLL Tables 17 and 18 and appropriate notes to reflect changes of VCO ranges for memory and CPU frequencies. Section 1.7—Updated voltage sequencing requirements in Table 2 and removed Section 1.7.2. Section 1.7.8—Updated TRST information and Figure 26. New Section 1.7.2—Updated the range of I/O power consumption numbers for OV_{DD} and GV_{DD} to correct values as in Table 5. Updated fastest frequency combination to 66:100:350 MHz. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of Ordering Information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.
0.5	—	Corrected labels for Figures 5 through 8.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.4	—	Section 1.2—Changed Features list (format) to match with the features list of the *MPC8245 Integrated Processor Reference Manual*. Section 1.4.1.2—Updated Table 2 to include 1.8 ± 100mV numbers. Section 1.4.3—Changed Table 7 to include new part offerings of 333 and 350 MHz. Added rows to include VCO frequency ranges for all parts for both memory VCO and CPU VCO. Section 1.4.1.5—Updated power consumption table to include 1.8 V (V_{DD}) and higher frequency numbers. Section 1.4.3—Updated Table 7 to include higher frequency offerings and CPU VCO frequency range. Section 1.4.3.1—Changed lettering to caps for DLL_EXTEND and DLL_MAX_DELAY in graph description section. Section 1.4.3.2—Changed name of item 11 from T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* Offset Time. Changed name to T_{os} in Note 7 as well. Section 1.6—Updated notes in Table 17. Included minimum and maximum VCO numbers for memory VCO. Changed Note 13 for location of PLL_CFG[0:4] to correct bits location. Bits 7–4 of register offset <0xE2>. Added Table 18 to cover PLL configuration of higher frequency part offerings. Section: 1.7—Changed frequency ranges for reference numbers 0, 9, 10, and 17, for the 300-MHz part to include the higher memory bus frequencies when operating at lower CPU bus frequencies. Added Table 18 to include PLL configurations for the 333 MHz and the 350 MHz CPU part offerings. Added VCO multipliers in Tables 17 and 18. Section 1.7.8—Changed T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_ SYNC_IN to *sys_logic_clk* Offset Time." Section 1.7.10—Added vendor (Cool Innovations, Inc.) to list of heat sink vendors.
0.3	—	Section 1.4.1.5—Changed Max-FP value for 33/133/266 of Table 5 from 2.3 to 2.1 watts to represent characterization data. Changed Note 4 to say V_{DD} = 2.1 for power measurements (for 2-V part). Changed numbers for maximum I/O power supplies for OV_{DD} and GV_{DD} to represent characterization data. Section 1.4.3.1—Added four graphs (Figures 5–8) and description for DLL Locking Range vs. Frequency of Operation to replace Figure 5 of Rev 0.2 document. Section 1.4.3.2—Added row (item 11: T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN timing) to Table 9 to include offset change requirement. Section 1.5.3—Changed Note 4 of PLL_CFG pins in Table 16 to Note 20. Section 1.7.2—Added diode (MUR420) to Figure 27, Voltage Sequencing Circuit, to compensate for voltage extremes in design. Section 1.7.5—Added sentence with regards to SDRAM_SYNC_IN to PCI_SYNC_IN timing requirement (T_{su}) as a connection recommendation. Section 1.7.8—Mention of T_{su} offset timing and driver capability differences between the MPC8240 and the MPC8245.

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