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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8245lzu350d

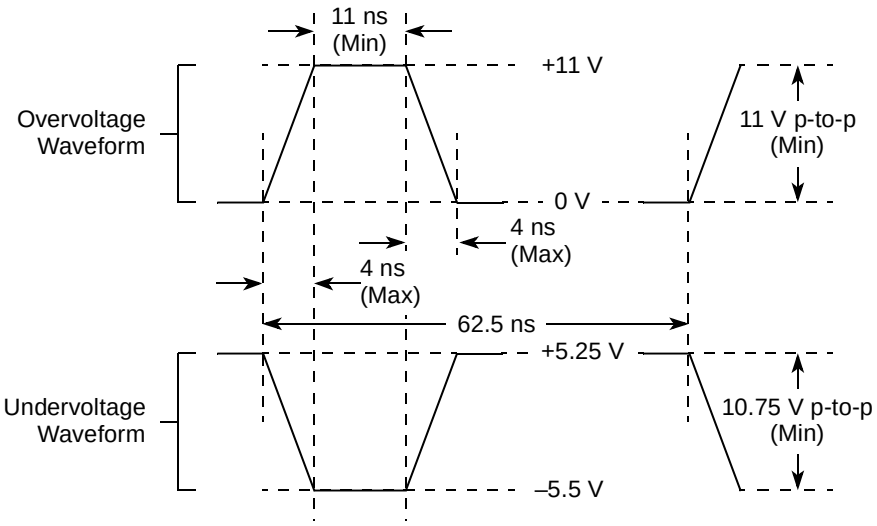

Figure 5. Maximum AC Waveforms for 5-V Signaling

4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8245 at recommended operating conditions.

Table 3. DC Electrical Specifications

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only, except PCI_SYNC_IN	V_{IH}	$0.65 \times OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only, except PCI_SYNC_IN	V_{IL}	—	$0.3 \times OV_{DD}$	V	
Input high voltage	All other pins, including PCI_SYNC_IN (GV_{DD} = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs, including PCI_SYNC_IN	V_{IL}	GND	0.8	V	
Input leakage current for pins using DRV_PCI driver	$0.5\ V \le V_{in} \le 2.7\ V$ @ LV_{DD} = 4.75 V	I_L	—	±70	μA	4
Input leakage current for all others	LV_{DD} = 3.6 V $GV_{DD} \le 3.465$ V	I_L	—	±10	μA	4
Output high voltage	I_{OH} = driver-dependent (GV_{DD} = 3.3 V)	V_{OH}	2.4	—	V	2
Output low voltage	I_{OL} = driver-dependent (GV_{DD} = 3.3 V)	V_{OL}	—	0.4	V	2

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8245. For details, see Section 7.8, "Thermal Management."

Table 6. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection (Single-layer board—1s)	$R_{\theta JA}$	16.1	°C/W	1, 2
Junction-to-ambient natural convection (Four-layer board—2s2p)	$R_{\theta JMA}$	12.0	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Single-layer board—1s)	$R_{\theta JMA}$	11.6	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Four layer board—2s2p)	$R_{\theta JMA}$	9.0	°C/W	1, 3
Junction-to-board	$R_{\theta JB}$	4.8	°C/W	4
Junction-to-case	$R_{\theta JC}$	1.8	°C/W	5
Junction-to-package top (natural convection)	Ψ_{JT}	1.0	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate used for case temperature.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 9, "Ordering Information," for details on ordering parts.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for details on MPC8245 memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

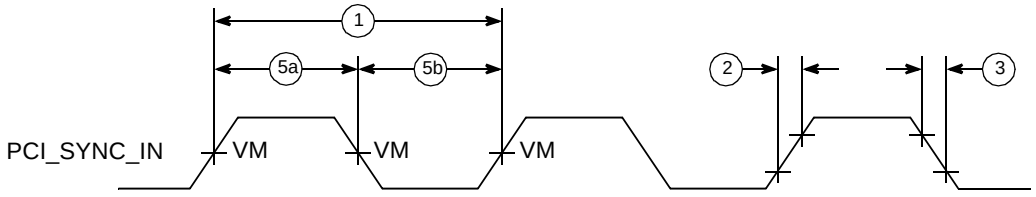

Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The gray areas show where the DLL locks.

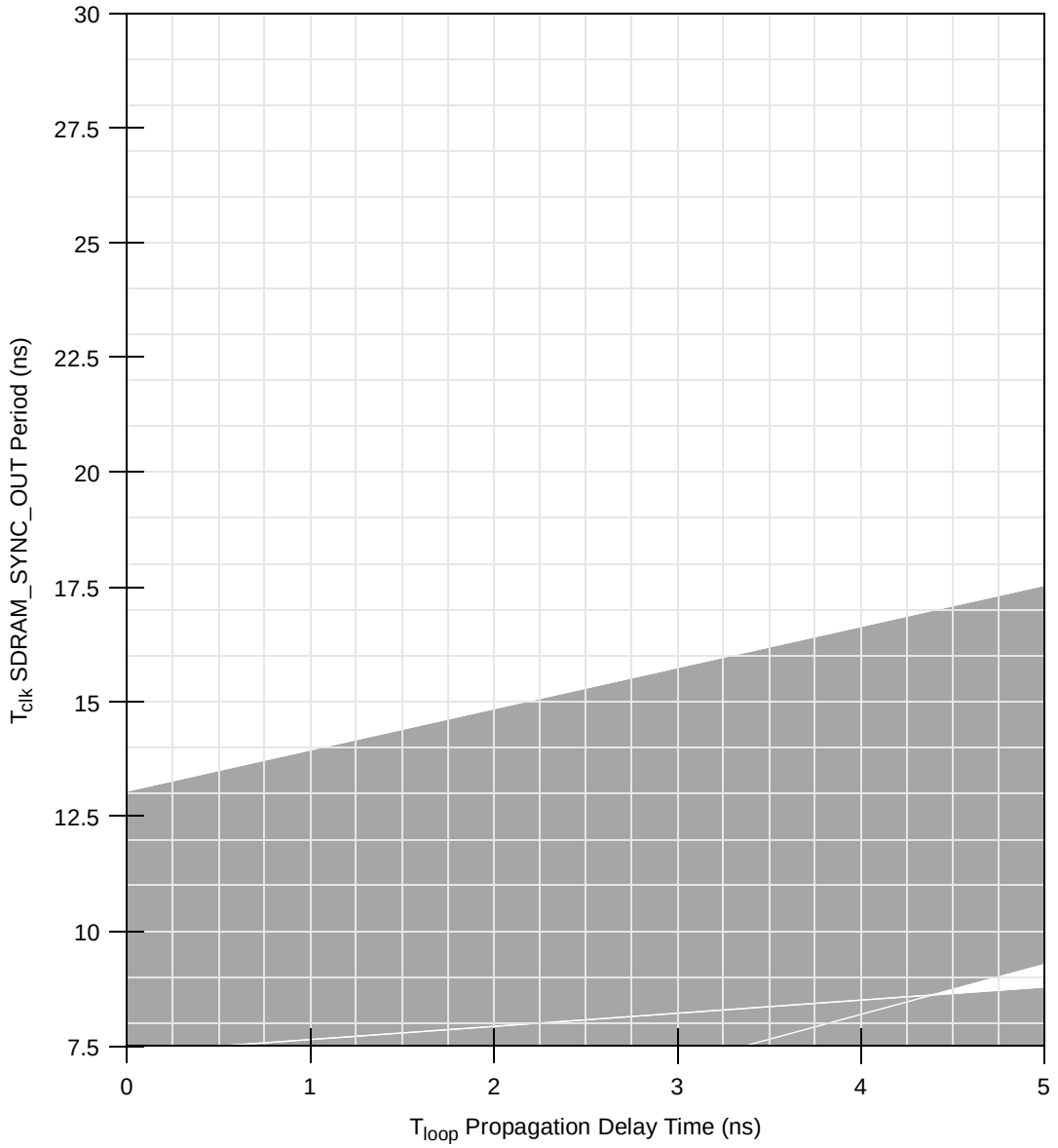

Figure 7. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=0 and Normal Tap Delay

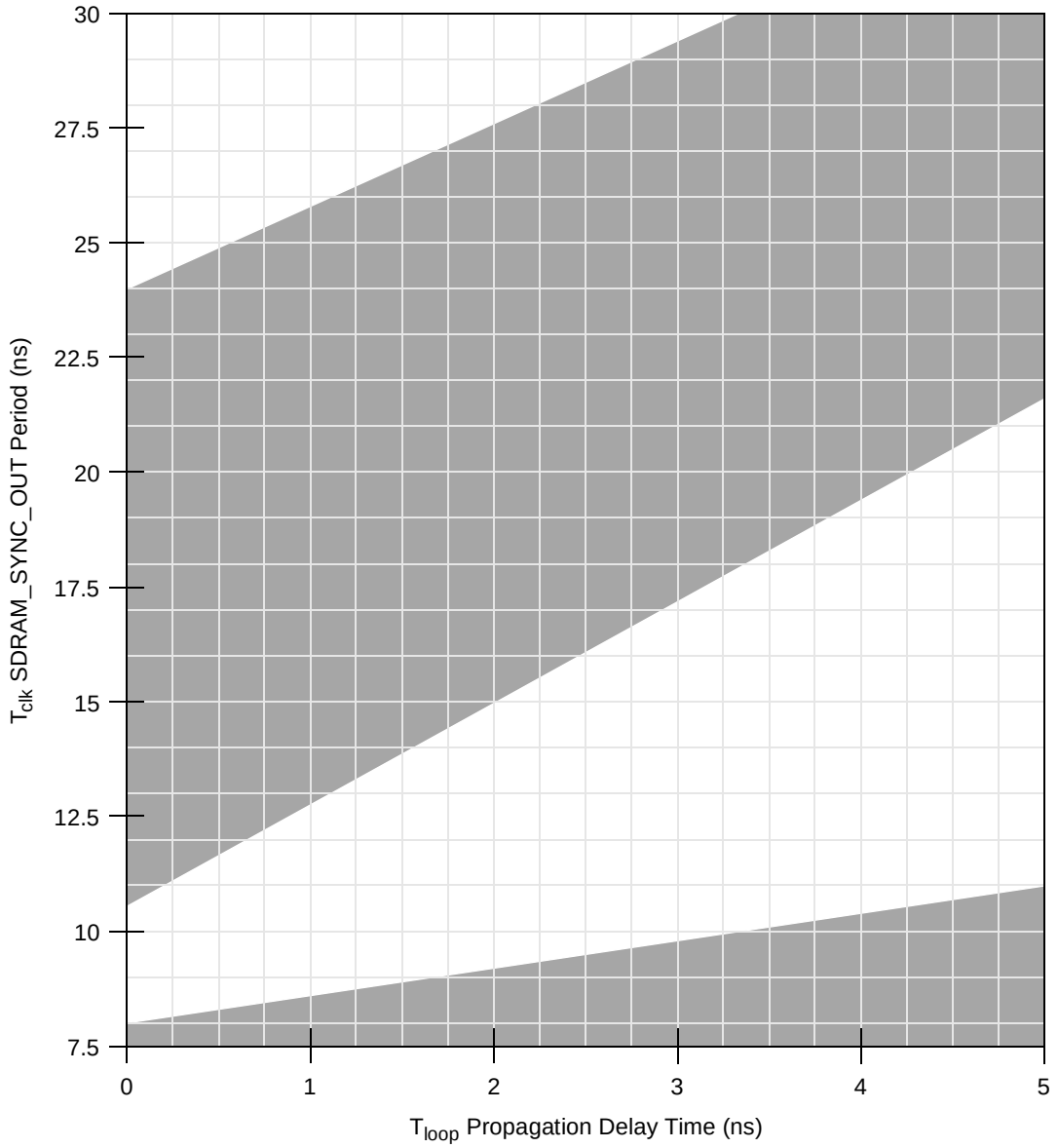

Figure 8. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

Figure 13 shows the input timing diagram for mode select signals.

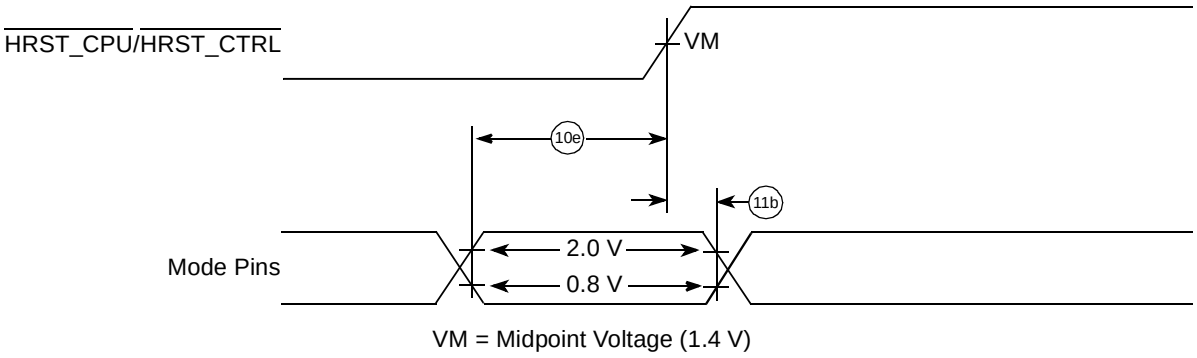

Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 for the input/output timing diagram referenced to *sys_logic_clk*. All output timings assume a purely resistive 50-Ω load (see Figure 14 for the AC test load for the MPC8245). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths indicated in Table 4.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory control, address, and data signals)	—	4.0	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/PortX)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66-MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33-MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Figure 17 shows the AC timing diagram for the I^2C bus.

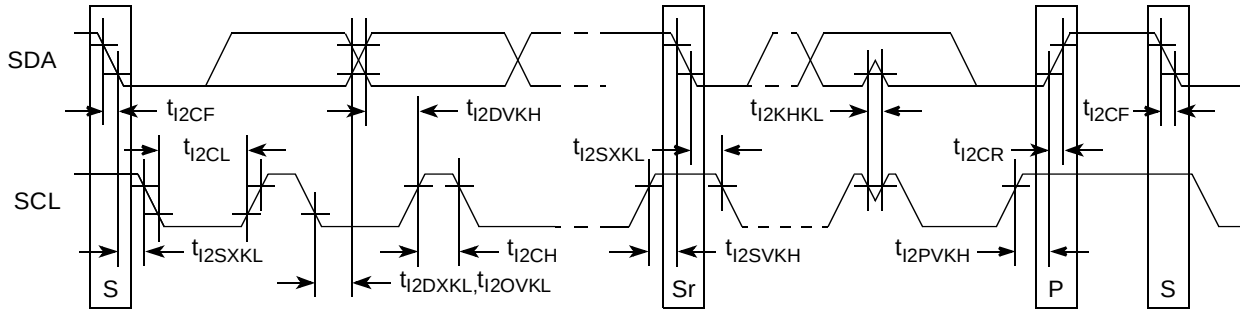

Figure 17. I^2C Bus AC Timing Diagram

4.7 PIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the PIC serial interrupt mode AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with GV_{DD} = 3.3 V ± 5% and LV_{DD} = 3.3 V ± 0.3 V.

Table 14. PIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	—
3	S_CLK output valid time	—	6	ns	—
4	Output hold time	0	—	ns	—
5	$\overline{\text{S\_FRAME}}$, S_RST output valid time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT input setup time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:

1. See the *MPC8245 Integrated Processor Reference Manual* for a description of the PIC interrupt control register (ICR) and S_CLK frequency programming.
2. S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 18 and Figure 19, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. The *MPC8245 Integrated Processor Reference Manual* describes the functional relationships between these signals.
3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor Reference Manual* for a complete clocking description.

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN) (continued)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams.

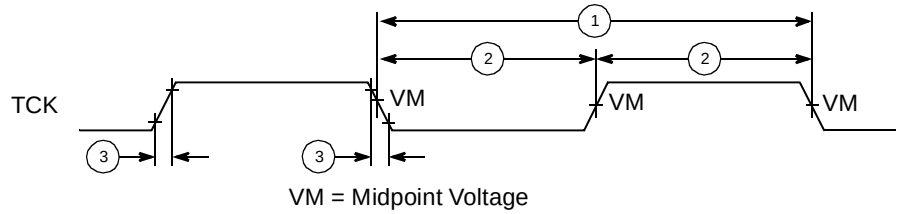

Figure 20. JTAG Clock Input Timing Diagram

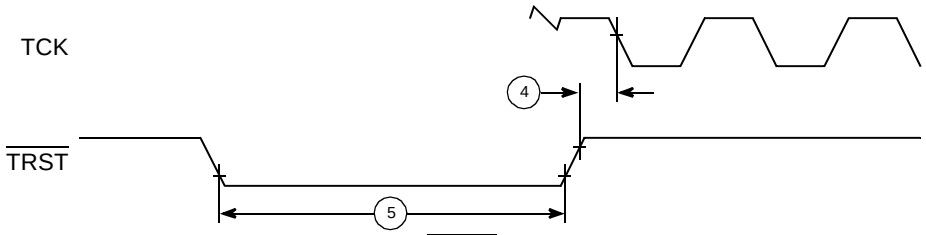

Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

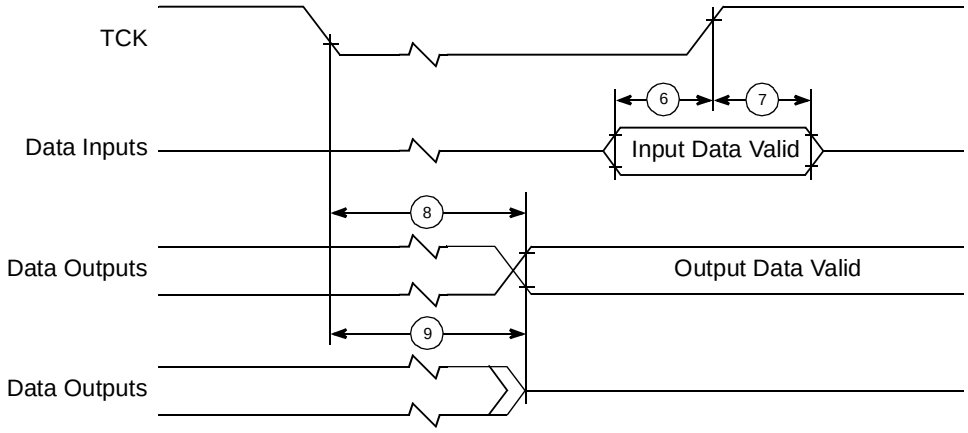

Figure 22. JTAG Boundary Scan Timing Diagram

Table 18. PLL Configurations (333- and 350-MHz Parts) (continued)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1E Rev B	11110[8]	Not usable			Not usable			Off	Off
1E Rev D	11110	33[3]–47[5]	66–94	231–329	33[3]–50[2,5,7]	66–100	231–350	2(2)	3.5(2)
1F	11111[8]	Not usable			Not usable			Off	Off

Notes:

1. Limited by the maximum PCI input frequency (66 MHz).
2. Limited by the maximum system memory interface operating frequency (100 MHz @ 350 MHz CPU).
3. Limited by the minimum memory VCO frequency (132 MHz).
4. Limited due to the maximum memory VCO frequency (372 MHz).
5. Limited by the maximum CPU operating frequency.
6. Limited by the minimum CPU VCO frequency (360 MHz).
7. Limited by the maximum CPU VCO frequency (Maximum marked CPU speed X 2).
8. In clock-off mode, no clocking occurs inside the MPC8245, regardless of the PCI_SYNC_IN input.
9. Range values are rounded down to the nearest whole number (decimal place accuracy removed).
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting differ from or do not exist on the MPC8240 and are not backward-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting differs from the MPC8240 and may not be fully backward-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
16. Limited by the maximum system memory interface operating frequency (133 MHz @ 333 MHz CPU).
17. Limited by the minimum CPU operating frequency (100 MHz).
18. Limited by the minimum memory bus frequency (50 MHz).

7 System Design

This section provides electrical and thermal design recommendations for successful application of the MPC8245.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8245 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500-kHz to 10-MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 25 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), using multiple small capacitors of equal value is recommended over using multiple values.

Place the circuits as closely as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing from the capacitors to the input signal pins should be as direct as possible with minimal inductance of vias.

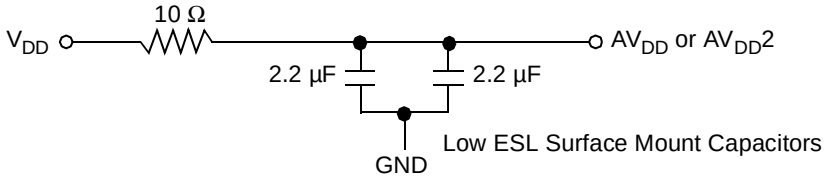

Figure 25. PLL Power Supply Filter Circuit

7.2 Decoupling Recommendations

Due to its dynamic power management feature, large address and data buses, and high operating frequencies, the MPC8245 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8245 system, and the MPC8245 itself requires a clean, tightly regulated source of power. Therefore, place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin. These decoupling capacitors should receive their power from dedicated power planes in the PCB, with short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic 0 level is read into the configuration bits during reset if the default logic 1 level is not desired.

Any other unused active low input pins should be tied to a logic-one level through weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND through weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8245 PCI reference voltage (LV_{DD}) pins should be connected to a 3.3 ± 0.3 V power supply if interfacing the MPC8245 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to a 5.0 V ± 5% power supply if interfacing the MPC8245 into a 5-V PCI bus system. For either reference voltage, the MPC8245 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8245 tolerates 5-V signals when interfaced into a 5-V PCI bus system.

7.6 MPC8245 Compatibility with MPC8240

The MPC8245 AC timing specifications are backward-compatible with those of the MPC8240, except for the requirements of item 11 in Table 10. Timing adjustments are needed as specified for T_{os} (SDRAM_SYNC_IN to *sys_logic_clk* offset) time requirements.

The MPC8245 does not support the SDRAM flow-through memory interface.

The nominal core V_{DD} power supply changes from 2.5 V on the MPC8240 to 1.8/2.0 V on the MPC8245. See Table 2.

For example, the MPC8245 PLL_CFG[0:4] setting 0x02 (0b00010) has a different PCI-to-Mem and Mem-to-CPU multiplier ratio than the same setting on the MPC8240, so it is not backward-compatible. See Table 17.

Most of the MPC8240 PLL_CFG[0:4] settings are subsets of the PCI_SYNC_IN input frequency range accepted by the MPC8245. However, the parts are not fully backward-compatible since the ranges of the two parts do not always match. Modes 0x8 and 0x18 of the MPC8245 are not compatible with settings 0x8 and 0x18 on the MPC8240. See Table 17 and Table 18.

Two reset configuration signals on the MPC8245 are not used as reset configuration signals on the MPC8240: SDMA0 and SDMA1.

The SDMA0 reset configuration pin selects between the MPC8245 DUART and the MPC8240 backward-compatible mode PCI_CLK[0:4] functionality on these multiplexed signals. The default state (logic 1) of SDMA0 selects the MPC8240 backward-compatible mode of PCI_CLK[0:4] functionality while a logic 0 state on the SDMA0 signal selects DUART functionality. In DUART mode, four of the five PCI clocks, PCI_CLK[0:3], are not available.

The SDMA1 reset configuration pin selects between MPC8245 extended ROM functionality and MPC8240 backward-compatible functionality on the multiplexed signals: TBEN, $\overline{\text{CHKSTOP\_IN}}$,

$\overline{\text{SRESET}}$, TRIG_IN, and TRIG_OUT. The default state (logic 1) of SDMA1 selects the MPC8240 backward-compatible mode functionality, while a logic 0 state on the SDMA1 signal selects extended ROM functionality. In extended ROM mode, the TBEN, $\overline{\text{CHKSTOP\_IN}}$, $\overline{\text{SRESET}}$, TRIG_IN, and TRIG_OUT functionalities are not available.

The driver names and pin capability of the MPC8245 and the MPC8240 differ slightly. Refer to the drive capability table (for the ODCR register at 0x73) in the *MPC8240 Integrated Processor Hardware Specifications* and Table 4.

The programmable PCI output valid and output hold feature controlled by bits in the power management configuration register 2 (PMCR2) <0x72> differs slightly in the MPC8245. For the MPC8240, three bits, PMCR2[6:4] = PCI_HOLD_DEL, are used to select 1 of 8 possible PCI output timing configurations. PMCR2[6:5] are software-controllable but are initially set by the reset configuration state of the $\overline{\text{MCP}}$ and CKE signals, respectively. Software can change PMCR2[4]. The default configuration for PMCR2[6:4] = 0b110 since the $\overline{\text{MCP}}$ and CKE signals have internal pull-up resistors, but this default configuration does not select 33- or 66-MHz PCI operation output timing parameters for the MPC8240. Software makes this selection. For the MPC8245, only two bits in the power management configuration register 2 (PMCR2), PMCR2[5:4] = PCI_HOLD_DEL, control the variable PCI output timing. PMCR2[5:4] are software controllable but are initially set by the inverted reset configuration state of the $\overline{\text{MCP}}$ and CKE signals, respectively. The default configuration for PMCR2[5:4] = 0b00 since the $\overline{\text{MCP}}$ and CKE signals have internal pull-up resistors and the values from these signals are inverted; this default configuration selects 66-MHz PCI operation output timing parameters. There are four programmable PCI output timing configurations on the MPC8245. See Table 11.

Voltage sequencing requirements for the MPC8245 are similar to those for the MPC8240, with two exceptions in the MPC8245. In the MPC8245, the non-PCI input voltages (V_{in}) must not be greater than GV_{DD} or OV_{DD} by more than 0.6 V at all times, including during power-on reset (see Caution 5 in Table 2). Second, LV_{DD} must not exceed OV_{DD} by more than 3.0 V at any time, including during power-on reset (see Caution 10 in Table 2); the allowable separation between LV_{DD} and OV_{DD} is 3.6 V for the MPC8240.

There is no LAV_{DD} input voltage supply signal on the MPC8245 since the SDRAM clock delay-locked loop (DLL) has power supplied internally. Signal D17 should be treated as a NC for the MPC8245. Application note AN2128 highlights the differences between the MPC8240 and the MPC8245.

7.7 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the Power Architecture technology. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, more reliable power-on reset performance can be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG, with additional status monitoring signals. The COP port must independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to control the processor. If the target system has independent

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

7.8 Thermal Management

This section provides thermal management information for the tape ball grid array (TBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, heat sinks may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly. Figure 27 displays a package-exploded cross-sectional view of a TBGA package with several heat sink options.

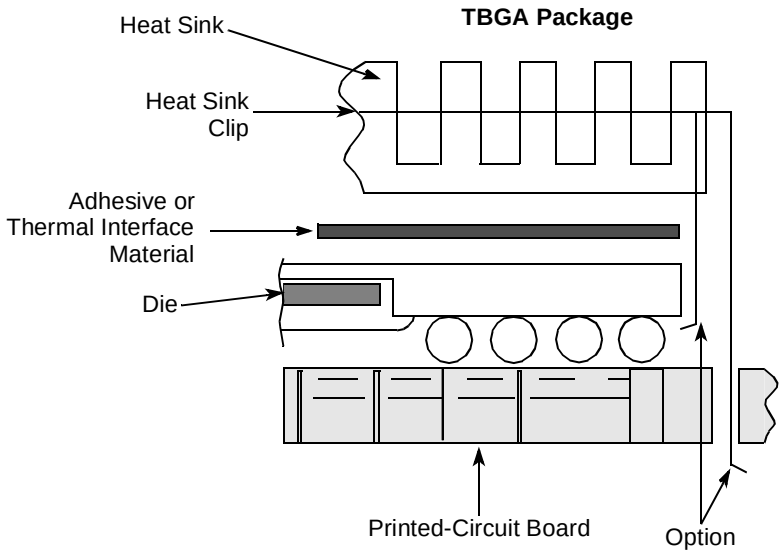

Figure 27. Package-Exploded Cross-Sectional View with Several Heat Sink Options

Figure 28 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the TBGA package, and there exists high board-level thermal loading from adjacent components.
- A heat sink is not attached to the TBGA package, and there is low board-level thermal loading from adjacent components.
- A heat sink (for example, ChipCoolers) is attached to the TBGA package, and there is high board-level thermal loading from adjacent components.
- A heat sink (for example, ChipCoolers) is attached to the TBGA package, and there is low board-level thermal loading from adjacent components.

7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material placed between the top of the package and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 30 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 30). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

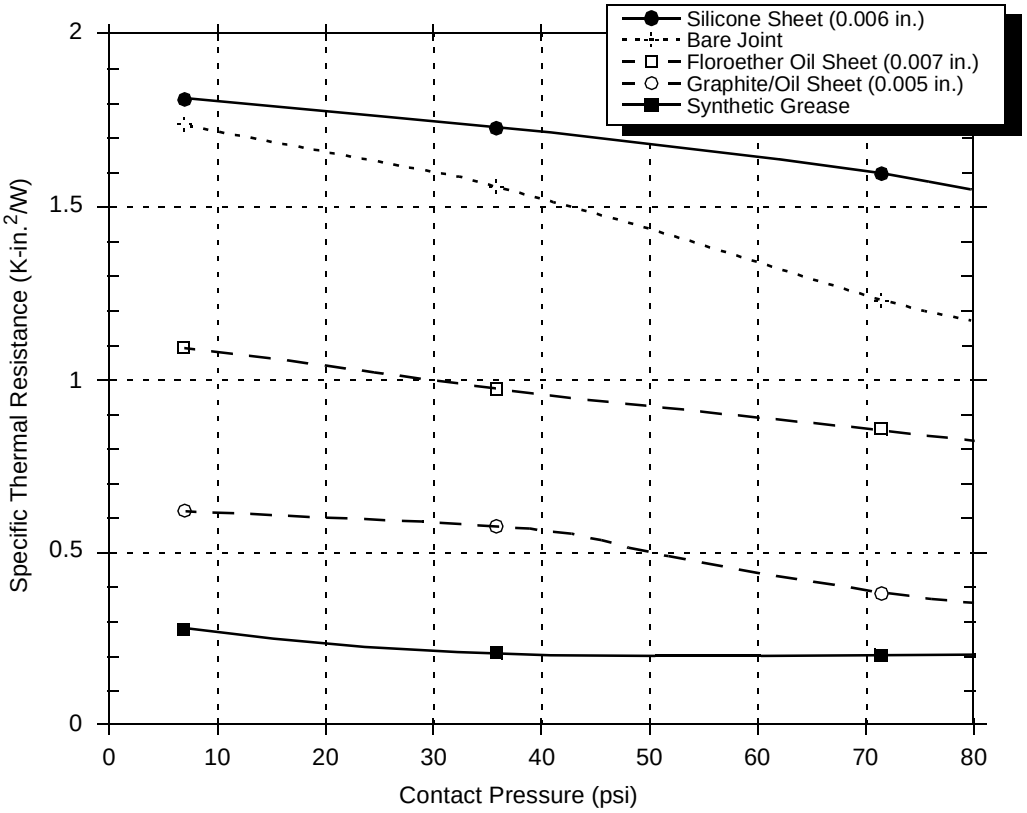

Figure 30. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.4	—	Section 1.2—Changed Features list (format) to match with the features list of the *MPC8245 Integrated Processor Reference Manual*. Section 1.4.1.2—Updated Table 2 to include 1.8 ± 100mV numbers. Section 1.4.3—Changed Table 7 to include new part offerings of 333 and 350 MHz. Added rows to include VCO frequency ranges for all parts for both memory VCO and CPU VCO. Section 1.4.1.5—Updated power consumption table to include 1.8 V (V_{DD}) and higher frequency numbers. Section 1.4.3—Updated Table 7 to include higher frequency offerings and CPU VCO frequency range. Section 1.4.3.1—Changed lettering to caps for DLL_EXTEND and DLL_MAX_DELAY in graph description section. Section 1.4.3.2—Changed name of item 11 from T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* Offset Time. Changed name to T_{os} in Note 7 as well. Section 1.6—Updated notes in Table 17. Included minimum and maximum VCO numbers for memory VCO. Changed Note 13 for location of PLL_CFG[0:4] to correct bits location. Bits 7–4 of register offset <0xE2>. Added Table 18 to cover PLL configuration of higher frequency part offerings. Section: 1.7—Changed frequency ranges for reference numbers 0, 9, 10, and 17, for the 300-MHz part to include the higher memory bus frequencies when operating at lower CPU bus frequencies. Added Table 18 to include PLL configurations for the 333 MHz and the 350 MHz CPU part offerings. Added VCO multipliers in Tables 17 and 18. Section 1.7.8—Changed T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_ SYNC_IN to *sys_logic_clk* Offset Time." Section 1.7.10—Added vendor (Cool Innovations, Inc.) to list of heat sink vendors.
0.3	—	Section 1.4.1.5—Changed Max-FP value for 33/133/266 of Table 5 from 2.3 to 2.1 watts to represent characterization data. Changed Note 4 to say V_{DD} = 2.1 for power measurements (for 2-V part). Changed numbers for maximum I/O power supplies for OV_{DD} and GV_{DD} to represent characterization data. Section 1.4.3.1—Added four graphs (Figures 5–8) and description for DLL Locking Range vs. Frequency of Operation to replace Figure 5 of Rev 0.2 document. Section 1.4.3.2—Added row (item 11: T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN timing) to Table 9 to include offset change requirement. Section 1.5.3—Changed Note 4 of PLL_CFG pins in Table 16 to Note 20. Section 1.7.2—Added diode (MUR420) to Figure 27, Voltage Sequencing Circuit, to compensate for voltage extremes in design. Section 1.7.5—Added sentence with regards to SDRAM_SYNC_IN to PCI_SYNC_IN timing requirement (T_{su}) as a connection recommendation. Section 1.7.8—Mention of T_{su} offset timing and driver capability differences between the MPC8240 and the MPC8245.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.2	—	Changed core supply voltage to 2.0 ± 100 mV in Section 1.3. (Supply voltage of 1.8 ± 100 mV is no longer recommended.) Changed rows 2, 5, and 6 of Table 2 to 2.0 ± 100 mV in the “Recommended Value” column. Changed the power consumption numbers in Table 5 to reflect the power values for V_{DD} = 2.0 V. (Notes 2, 3, 4, and 5 of the table were also updated to reflect the new value of V_{DD}.) Updated Table 9 for $V_{DD}/AV_{DD}/AV_{DD}2$ to 2.0 ± 100 mV. Table 8: $V_{DD}/AV_{DD}/AV_{DD}2$ was changed to 2.0 V for both CPU frequency offerings. Note 2 was updated by removing the “at reduced voltage...” statement. Table 10: Update maximum time of the rows 12a0 through 12a3. Table 16: Fixed overbars for the active-low signals. Changed pin type information for V_{DD}, AV_{DD}, and $AV_{DD}2$ to 2.0 V. Changed Note 16 of Table 17 to a value of 2.0 V for $V_{DD}/AV_{DD}/AV_{DD}2$. Removed second sentence of the second paragraph in Section 1.7.2 because it referenced information about a 1.8-V design. Removed reference to 1.8 V in third sentence of Section 1.7.7.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.1	—	Made $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V ± 100 mV information for 133-MHz memory interface operation to Section 1.3, Table 2, Table 5, Table 9, Table 17, and Section 1.7.2. Pin D17, formerly LAV_{DD} (supply voltage for DLL), is a NC on the MPC8245 since the DLL voltage is supplied internally. Eliminated all references to LAV_{DD}; updated Section 1.7.1. Previous Note 4 of Table 2 did not apply to the MPC8245 (MPC8240 document legacy). New Note 4 added in reference to maximum CPU speed at reduced V_{DD} voltage. Updated the Programmable Output Impedance of DEV_MEM_ADDR in Table 4 to 6 Ω to reflect characterization data. Updated Table 5 to reflect reduced power consumption when operating $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V ± 100 mV. Changed Notes 2, 3, and 4 to reflect V_{DD} at 1.9 V. Changed Note 5 to represent $V_{DD} = AV_{DD}$ = 1.8 V. Updated Table 7 to reflect $V_{DD}/AV_{DD}/AV_{DD}2$ voltage level operating frequency dependencies; changed 250 MHz device column to 266 MHz; modified Note 1 eliminating VCO references; added Note 2. Changed 250 MHz processor frequency offering to 266 MHz. Changed Spec 12b for memory output valid time in Table 11 from 5.5 ns to 4.5 ns; this is a key specification change to enable 133-MHz memory interface designs. Updated Pinout Table 16 with the following changes: • Pin types for $\overline{\text{RCS0}}$, $\overline{\text{RCS3}}$/TRIG_OUT and DA[11:15] were erroneously listed as I/O, changed Pin Types to Output. • Pin types for $\overline{\text{REQ}}$4/DA4, $\overline{\text{RCS2}}$/TRIG_IN, and PLL_CFG[0:4]/DA[10:6] were erroneously listed as Input, changed Pin Types to I/O. • Changed Pin D17 from LAV_{DD} to No Connect; deleted Note 21 and references. • Notes 3, 5, and 7 contained references to the MPC8240 (MPC8240 document legacy); changed these references to MPC8245. • Previous Notes 13 and 14 did not apply to the MPC8245 (MPC8240 document legacy), these notes were deleted; moved Note 19 to become new Note 13; moved Note 20 to become new Note 14; updated associated references. • Added Note 3 to SDMA[1:0] signals about internal pull-up resistors during reset state. • Reversed vector ordering for the PCI Interface Signals: $\overline{\text{C/BE}}$[0:3] changed to $\overline{\text{C/BE}}$[3:0], AD[0:31] changed to AD[31:0], $\overline{\text{GNT}}$[0:3] changed to $\overline{\text{GNT}}$[3:0], and $\overline{\text{REQ}}$[0:3] changed to $\overline{\text{REQ}}$[3:0]. The package pin number orderings were also reversed meaning that pin functionality did NOT change. For example, AD0 is still on signal C22, AD1 is still on signal D22,..., AD31 is still on signal V25. This change was made to make the vectored PCI signals in this hardware specification consistent with the *PCI Local Bus Specification* and the *MPC8245 Integrated Processor Reference Manual* vector ordering. • Changed $\overline{\text{TEST1}}/\overline{\text{DRDY}}$ signal on pin B20 to $\overline{\text{DRDY}}$. • Changed $\overline{\text{TEST2}}$ signal on pin Y2 to RTC for performance monitor use. Updated PLL Table 17 with the following changes for 133-MHz memory interface operation: • Added Ref. 9 (01001) and Ref. 17 (10111) details; removed these settings from Note 10 (reserved settings list). • Enhanced range of Ref. 10 (10000). • Updated Note 13, changed bits 16–20 erroneous information to correct bits 23–19. • Added Notes 16 and 17. Added information to Section 1.7.8 in reference to $\overline{\text{CHKSTOP\_IN}}$ and $\overline{\text{SRESET}}$ being unavailable in extended ROM mode.
0.0	—	Initial release.

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