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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8245lvv266d

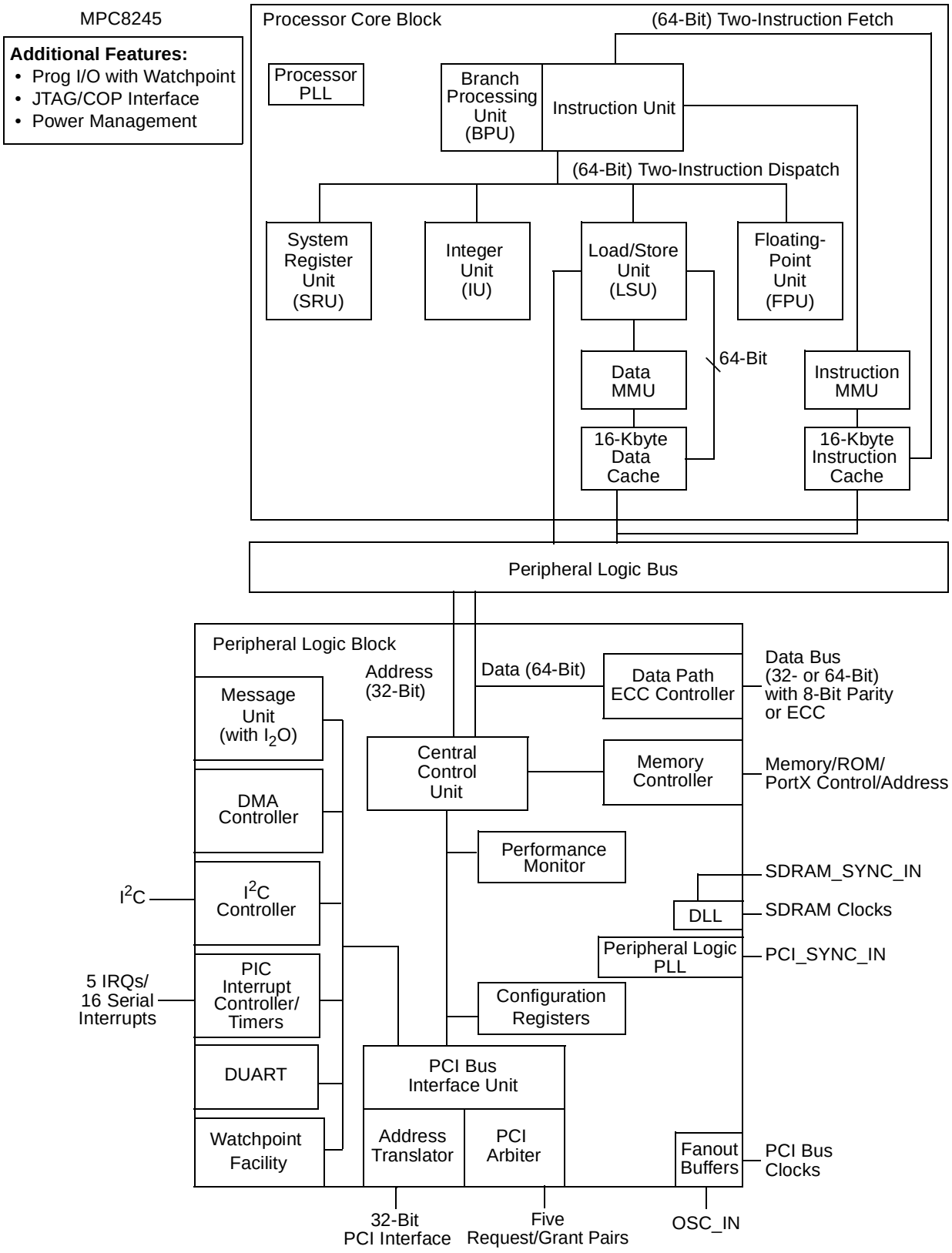


Figure 1. MPC8245 Block Diagram

  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System-level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—Marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std 1149.1® (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8245:

Technology	0.25-µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully-static
Packages	Surface-mount 352 tape ball grid array (TBGA)
Core power supply	1.7 V to 2.1 V DC for 266 and 300 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 1.8/1.9/2.0 volts. 1.9 V to 2.2 V DC for 333 and 350 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 2.0/2.1 volts. See Table 2 for details of recommended operating conditions)
I/O power supply	3.0- to 3.6-V DC

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8245.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other DC electrical characteristics.

4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC8245 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.25	V
Supply voltage—memory bus drivers	GV_{DD}	–0.3 to 3.6	V
Supply voltage—PCI and standard I/O buffers	OV_{DD}	–0.3 to 3.6	V
Supply voltage—PLLs	AV_{DD}/AV_{DD} 2	–0.3 to 2.25	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105[3]	°C
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.
3. Note that this temperature range does not apply to the 400 MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8245. Some voltage values do not apply to the 400-MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

Table 2. Recommended Operating Conditions[1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply voltage	V_{DD}	1.8/1.9/2.0 V ± 100 mV	V	4, 7
		2.0/2.1 V ± 100 mV	V	5, 7
I/O buffer supply for PCI and standard	OV_{DD}	3.3 ± 0.3	V	7
Supply voltages for memory bus drivers	GV_{DD}	3.3 ± 5%	V	9
CPU PLL supply voltage	AV_{DD}	1.8/1.9/2.0 V ±	V	4, 7, 12
		2.0/2.1 V ±	V	5, 7, 12

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for details on MPC8245 memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

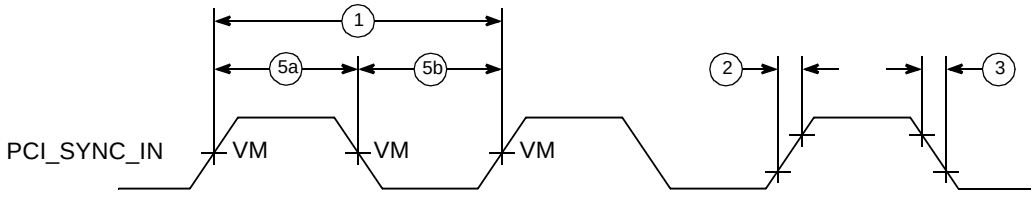


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The gray areas show where the DLL locks.

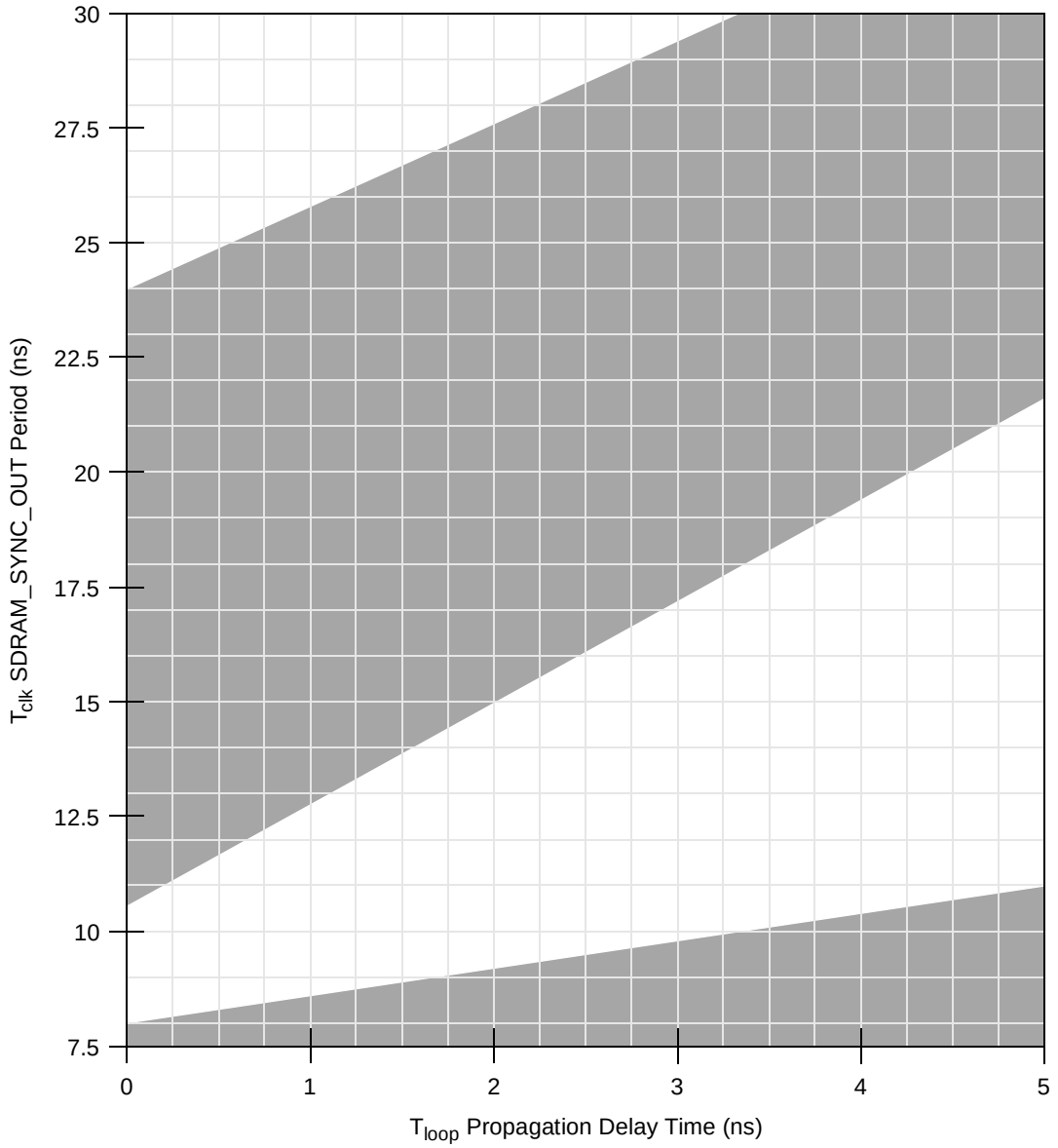


Figure 8. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

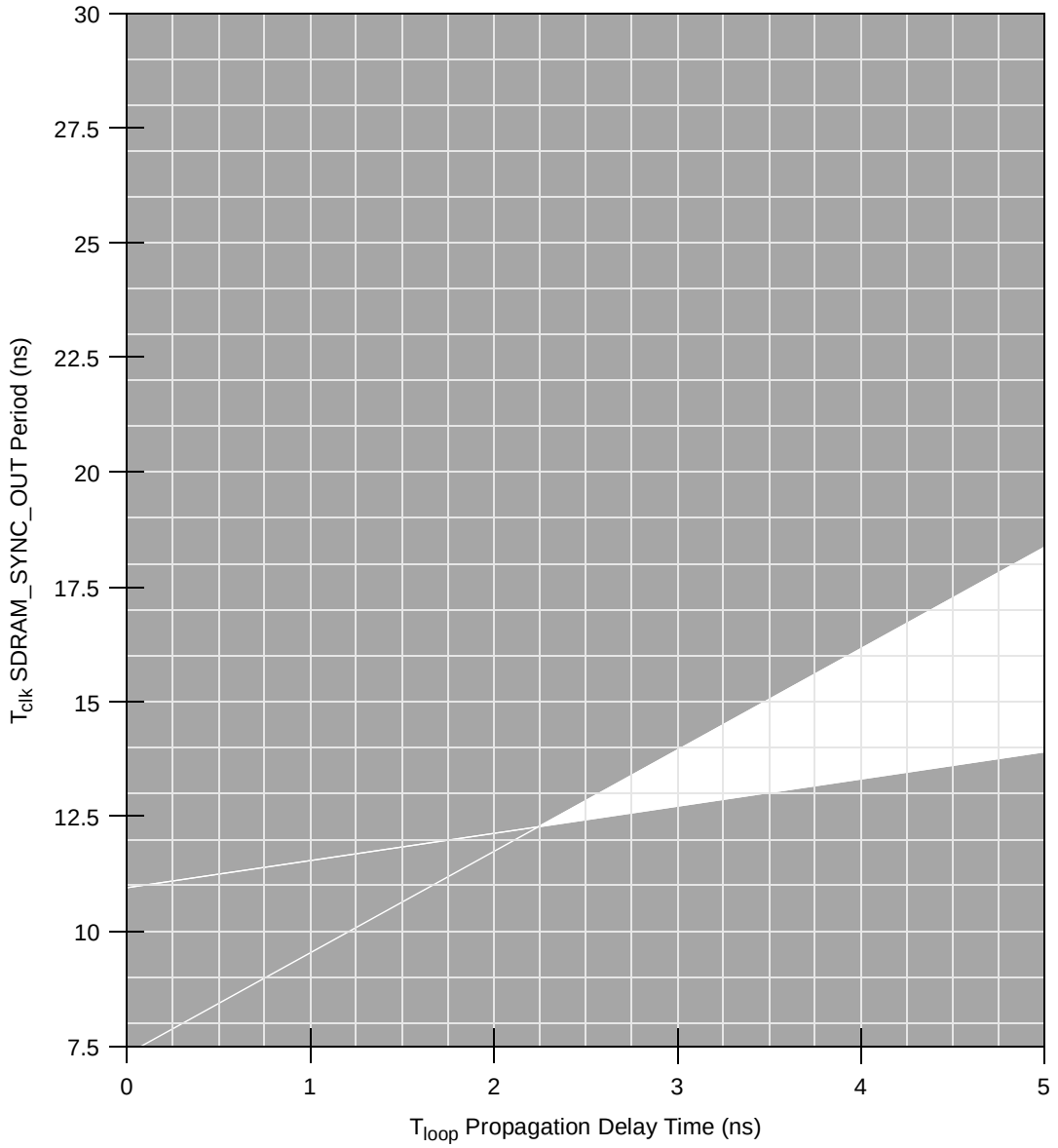
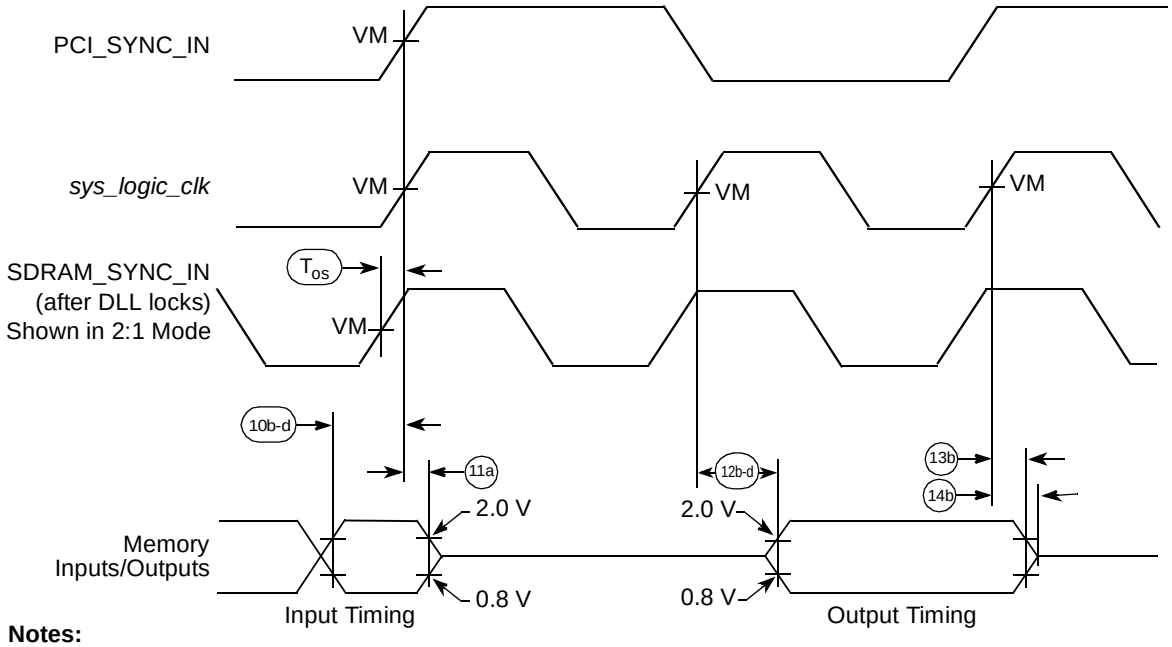


Figure 10. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=1 and Max Tap Delay

4.5.2 Input AC Timing Specifications

Table 10 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V.

Figure 11 and Figure 12 show the input/output timing diagrams referenced to SDRAM_SYNC_IN and PCI_SYNC_IN, respectively.



Notes:
VM = Midpoint voltage (1.4 V).
10b-d = Input signals valid timing.
11a = Input hold time of SDRAM_SYNC_IN to memory.
12b-d = *sys_logic_clk* to output valid timing.
13b = Output hold time for non-PCI signals.
14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.
T_{os} = Offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to appear before *sys_logic_clk* once the DLL locks.

Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN

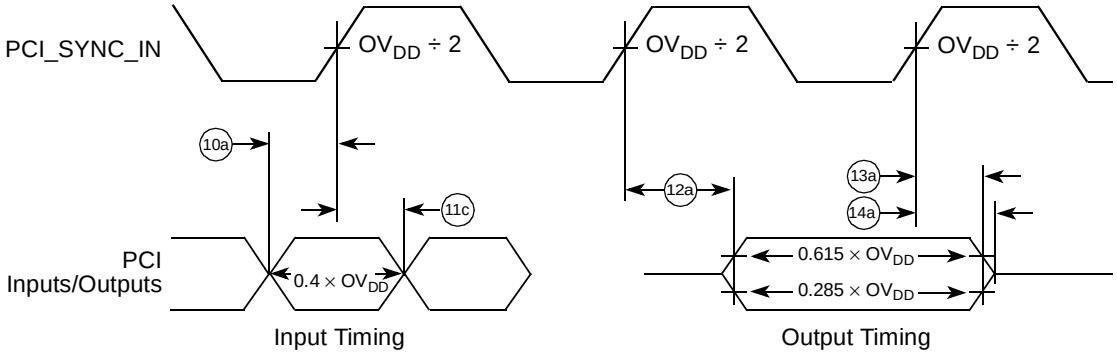


Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

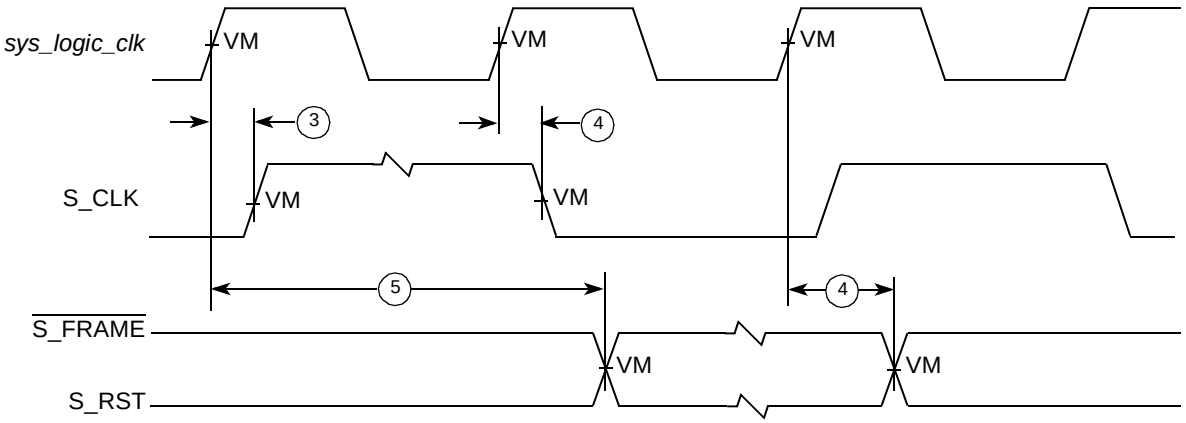


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

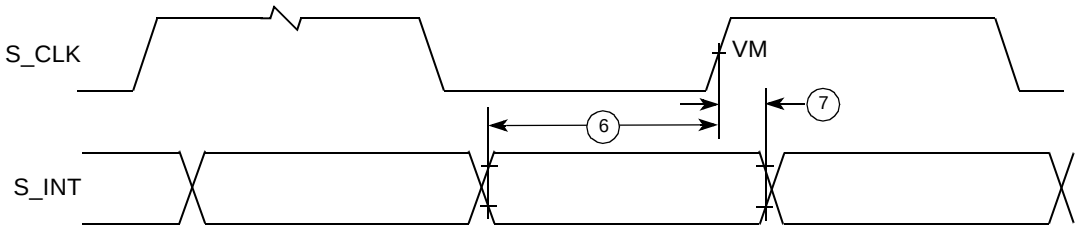


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.8 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8245 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.5 V	20	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN) (continued)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams.

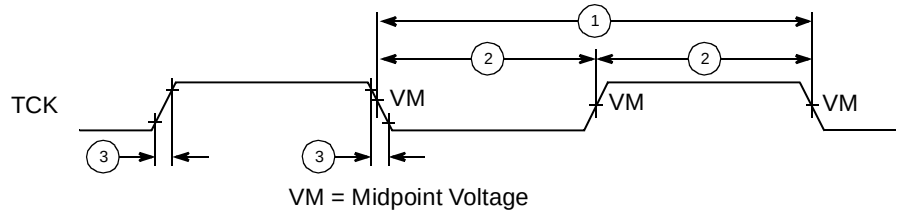


Figure 20. JTAG Clock Input Timing Diagram

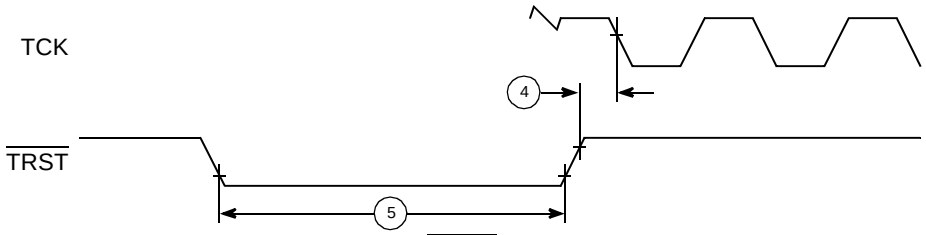


Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

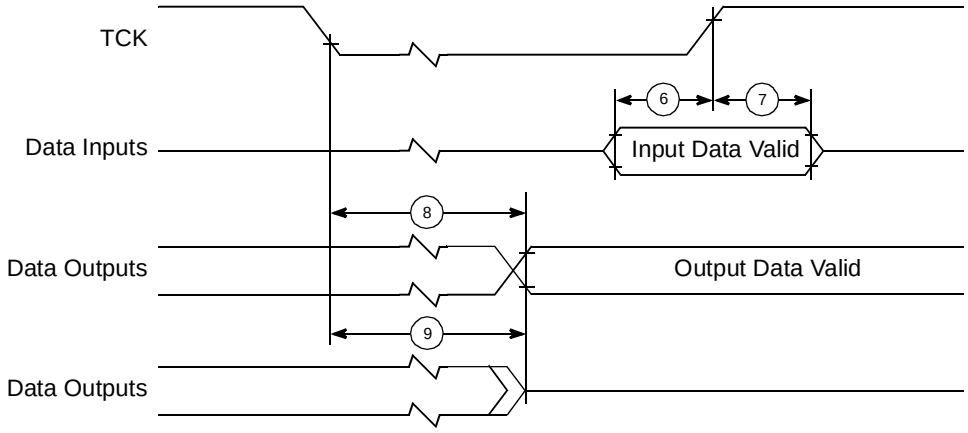


Figure 22. JTAG Boundary Scan Timing Diagram

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
$\overline{\text{QACK}}$/DA0	F2	Output	OV_{DD}	DRV_STD_MEM	4, 14, 25
$\overline{\text{CHKSTOP\_IN}}$/ SDMA14	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TRIG_IN/$\overline{\text{RCS2}}$	AF20	I/O	OV_{DD}	—	10, 14
TRIG_OUT/$\overline{\text{RCS3}}$	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
MAA[0:2]	AF2 AF1 AE1	Output	GV_{DD}	DRV_STD_MEM	3, 4, 6
$\overline{\text{MIV}}$	A16	Output	OV_{DD}	—	24
PMAA[0:1]	AD18 AF18	Output	OV_{DD}	DRV_STD_MEM	3, 4, 6, 15
PMAA[2]	AE19	Output	OV_{DD}	DRV_STD_MEM	4, 6, 15
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
$\overline{\text{TEST0}}$	AD22	Input	OV_{DD}	—	1, 9
RTC	Y2	Input	GV_{DD}	—	11
TCK	AF22	Input	OV_{DD}	—	9, 12
TDI	AF23	Input	OV_{DD}	—	9, 12
TDO	AC21	Output	OV_{DD}	—	24
TMS	AE22	Input	OV_{DD}	—	9, 12
$\overline{\text{TRST}}$	AE23	Input	OV_{DD}	—	9, 12
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground	—	—	
LV_{DD}	AC20 AC23 D20 D23 G23 P23 Y23	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	
GV_{DD}	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for memory drivers 3.3 V	GV_{DD}	—	
OV_{DD}	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3 V	OV_{DD}	—	

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

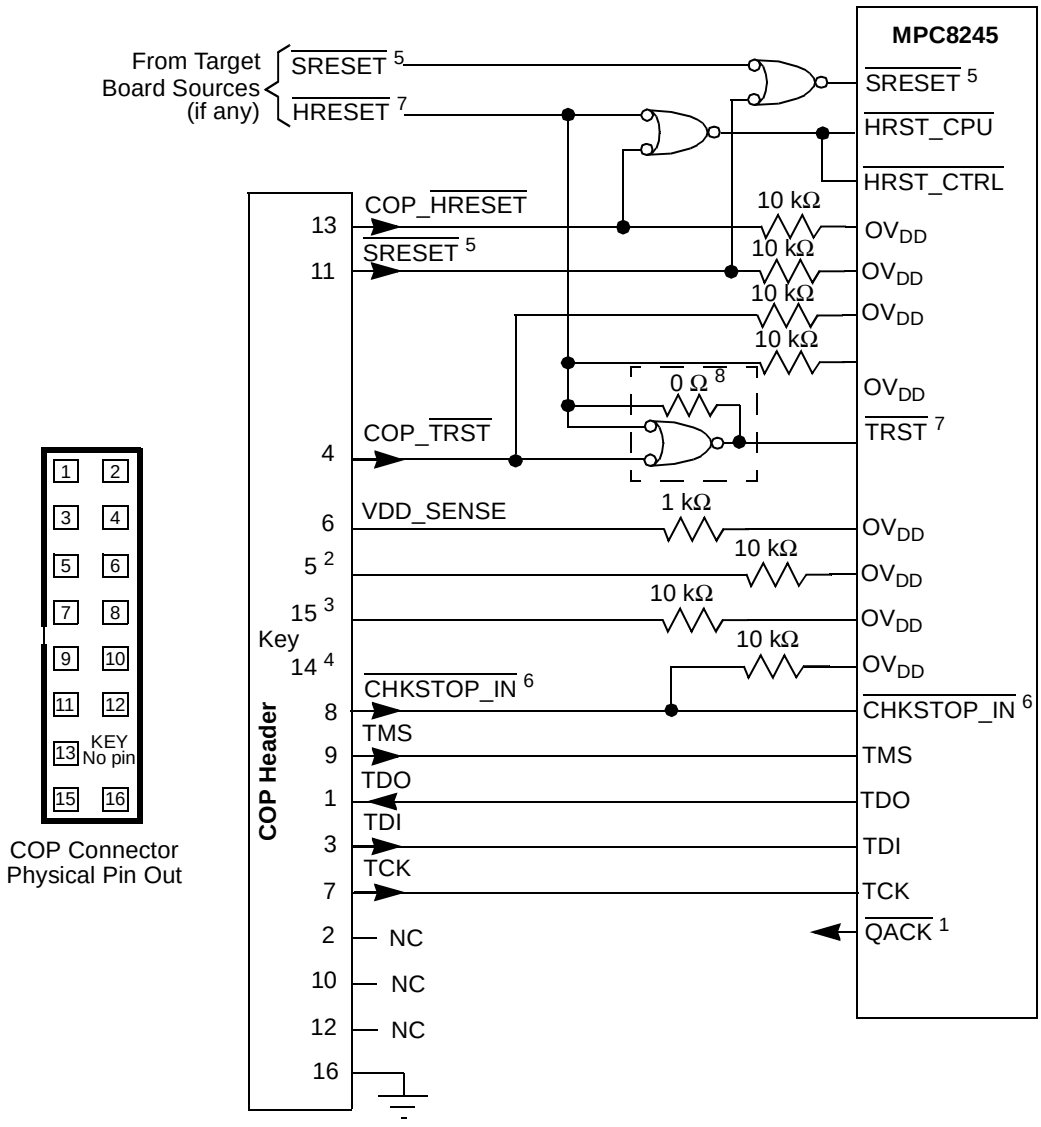
Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
13	10011[12]	Not available			25[2,7]	100	300	4 (2)	3 (2)
14	10100[12]	26[6]–38[5]	52–76	182–266	26[6]–42[5]	52–84	182–294	2 (4)	3.5 (2)
15	10101[12]	Not available			27[3]–30[5,7]	68–75	272–300	2.5 (2)	4 (2)
16	10110[12]	25–33[5]	50–66	200–264	25–37[5]	50–74	200–296	2 (4)	4 (2)
17	10111[12]	25–33[5]	100–132	200–264	25–33[2]	100–132	200–264	4 (2)	2 (2)
18	11000[12]	27[3]–35[5]	68–88	204–264	27[3]–40[5,7]	68–100	204–300	2.5 (2)	3 (2)
19	11001[12]	36[6]–53[5]	72–106	180–265	36[6]–59[2]	72–118	180–295	2 (2)	2.5 (2)
1A	11010[12]	50[18]–66[1]	50–66	200–264	50[18]–66[1]	50–66	200–264	1 (4)	4 (2)
1B	11011[12]	34[3]–44[5]	68–88	204–264	34[3]–50[5,7]	68–100	204–300	2 (2)	3 (2)
1C	11100[12]	44[3]–59[5]	66–88	198–264	44[3]–66[1]	66–99	198–297	1.5 (2)	3 (2)
1D	11101[12]	48[6]–66[1]	72–99	180–248	48[6]–66[1]	72–99	180–248	1.5 (2)	2.5 (2)
1E Rev B	11110[8]	Not usable			Not usable			Off	Off
1E Rev D	11110	33[3]–38[5]	66–76	231–266	33[3]–42[5]	66–84	231–294	2(2)	3.5(2)

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.



Note:

1. $\overline{\text{QACK}}$ is an output and is not required at the COP header for emulation.
2. RUN/$\overline{\text{STOP}}$ normally found on pin 5 of the COP header is not implemented on the MPC8245. Connect pin 5 of the COP header to OV_{DD} with a 1-kΩ pull-up resistor.
3. $\overline{\text{CKSTP\_OUT}}$ normally on pin 15 of the COP header is not implemented on the MPC8245. Connect pin 15 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. $\overline{\text{SRESET}}$ functions as output SDMA12 in extended ROM mode.
6. $\overline{\text{CHKSTOP\_IN}}$ functions as output SDMA14 in extended ROM mode.
7. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to control the processor as shown.
8. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header through an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.

Figure 26. COP Connector Diagram

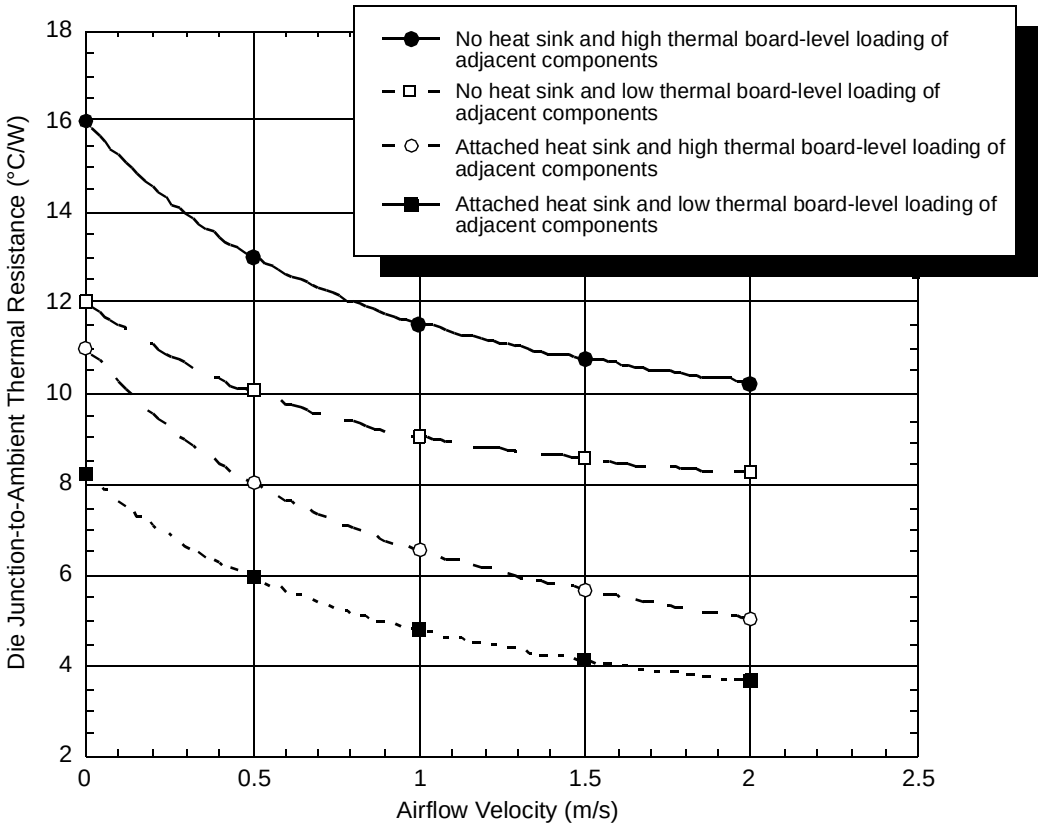


Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances and may or may not need airflow.

7.8.1 Internal Package Conduction Resistance

The intrinsic conduction thermal resistance paths for the TBGA cavity-down packaging technology shown in Figure 29 are as follows:

- Die junction-to-case thermal resistance
- Die junction-to-ball thermal resistance

Figure 29 depicts the primary heat transfer path for a package with an attached heat sink mounted on a printed-circuit board.

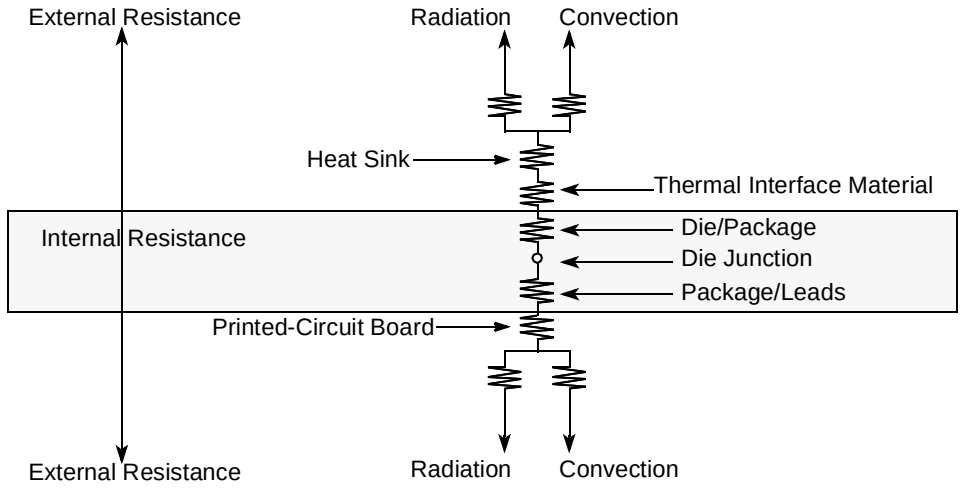


Figure 29. TBGA Package with Heat Sink Mounted to a Printed-Circuit Board

In a TBGA package, the active side of the die faces the printed-circuit board. Most of the heat travels through the die, across the die attach layer, and into the copper spreader. Some of the heat is removed from the top surface of the spreader through convection and radiation. Another percentage of the heat enters the printed-circuit board through the solder balls. The heat is then removed from the exposed surfaces of the board through convection and radiation. If a heat sink is used, a larger percentage of heat leaves through the top side of the spreader.

7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material placed between the top of the package and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 30 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 30). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

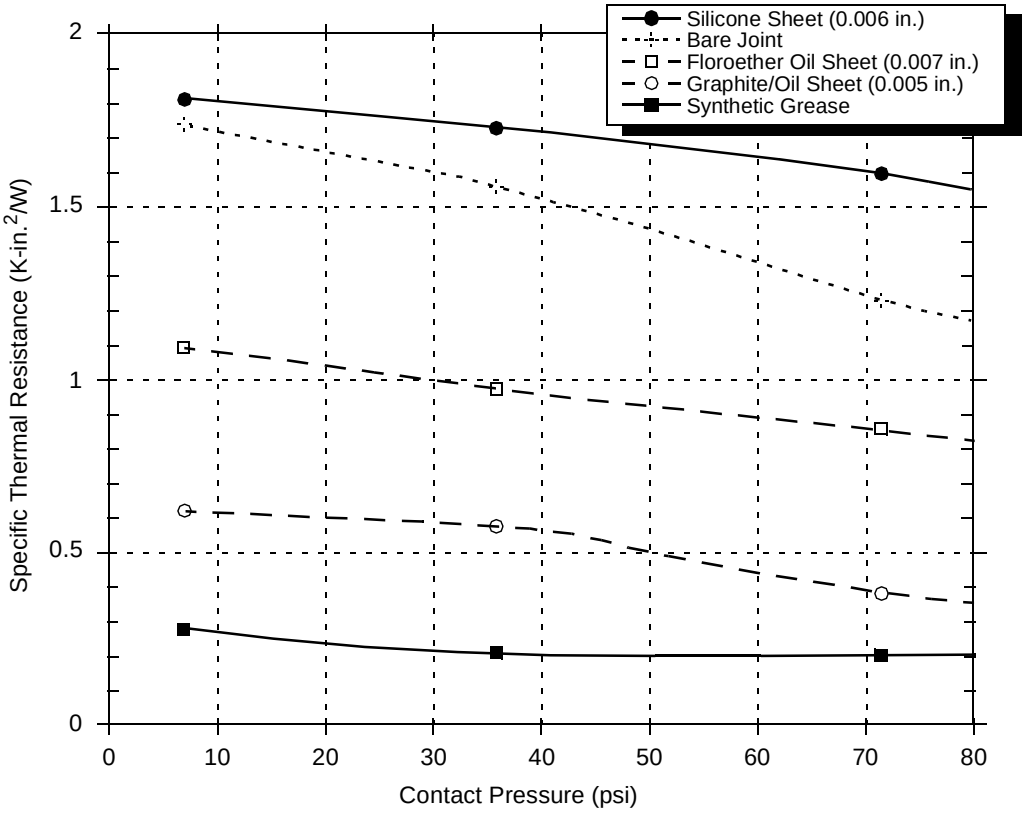


Figure 30. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

7.8.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
5	—	Section 4.1.2 — Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3 — Table 7, updated specifications for the voltage range of V_{DD} for specific CPU frequencies. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in Test/Configuration signal list and updated relevant notes for signal in Memory Interface signal listing. Updated note #20. Added note 26 for the signals of the UART interface. Section 7.6 — Added reference to AN2128 application note that highlights the differences between the MPC8240 and the MPC8245. Section 7.7 — Added relevant notes to this section and updated Figure 29.
4	—	Section 1.4.1.2—Updated notes for GV_{DD}, AV_{DD}, AV_{DD2}. Section 1.5.1—Updated solder ball information to include lead-free (V V) balls. Section 1.5.3—Updated Note 25 for $\overline{\text{QACK}}$/DA0 signal. Added a sentence to Note 3. Section 1.6 —Incorporated Note 19 into Note 12 and modified Tables 18 and 19 accordingly. Section 1.9—Updated part marking nomenclature where appropriate to include the lead-free offering. Replaced reference to PNS document MPC8245RZUPNS with MPC8245ARZUPNS.
3	—	Section 1.4.1.2—Figure 2: Updated Note 2 and removed ‘voltage regulator delay’ label since Section 1.7.2 is being deleted this revision. Added Figures 4 and 5 to show voltage overshoot and undershoot of the PCI interface on the MPC8245. Section 1.4.1.3—Table 3: Updated the maximum input capacitance from 7 to 16 pF based on characterization data. Section 1.4.3.1—Updated PCI_SYNC_IN jitter specifications to 200 ps. Section 1.4.3.3—Table 11, item 12b: added the word ‘address’ to help clarify which signals the spec applies to. Figure 15: edited timing for items 12a0 and 12a2 to correspond with Table 11. Section 1.5.3—Updated notes for the $\overline{\text{QACK}}$/DA0 signal because this signal has been found to have no internal pull resistor. Section 1.6—Corrected note numbers for reference numbers 3,10,1B, and 1C of the PLL tables. Updated PLL specifications for modes 7 and 1E. Section 1.7.2—Removed this section since the information already exists in Section 1.4.1.5. Section 1.7.4—Added the words ‘the clamping voltage’ to describe LV_{DD} in the sixth paragraph. Changed the $\overline{\text{QACK}}$/DA0 signal from the list of signals having an internal pull-up resistor to the list of signals needing a weak pull-up resistor to OV_{DD}. Section 1.9.1—Tables 21 thru 23: Added processor version register value.

9.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications that supplement and supersede this document. Table 21 shows the part numbers addressed by the MPC8245T*XXnnnx* series. The revision level can be determined by reading the Revision ID register at address offset 0x08.

Table 21. Part Numbers Addressed by MPC8245T*XXnnnx* Series
Part Number Specification Markings
(Document Order No. MPC8245ECS01AD)

MPC	*nnnn*	X	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process Descriptor	Package [1]	Processor Frequency [2]	Revision Level	Processor Version Register Value
MPC	8245	T: –40° to 105°C	ZU = TBGA V V= Lead-free TBGA	266 MHz, 300 MHz: 1.7 V to 2.1 V 333 MHz, 350 MHz: 1.9 V to 2.2 V	D:1.4 Rev ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.

Table 22 shows the part numbers addressed by the MPC8245ARZU*nnnx* series.

Table 22. Part Numbers Addressed by MPC8245ARZU*nnnx* Series
Part Number Specification Markings
(Document Order No. MPC8245ECS02AD)

MPC	*nnnn*	*X*	X	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process [3] Identifier	Process Descriptor	Package [1]	Processor Frequency [2]	Revision Level	Processor Version Register Value
MPC	8245	A	R: 0° to 85°C	ZU = TBGA V V= Lead-free TBGA	400 MHz 2.1 V ± 100 mV	D:1.4 Rev ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.
3. Process identifier ‘A’ represents parts that are manufactured under a 29-angstrom process verses the original 35-angstrom process.

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