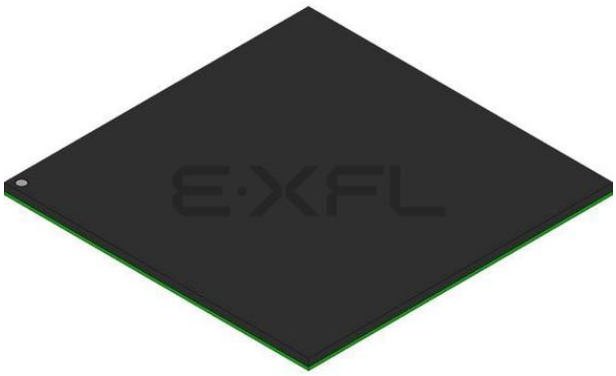

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8245lvv300d

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, a 16-Kbyte instruction cache, a 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade off performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8245 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8245 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8245 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—Entire cache or on a per-way basis up to three of four ways
  - Dynamic power management: 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing supporting SDRAM
    - One to eight banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

Table 2. Recommended Operating Conditions[1] (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8/1.9/2.0 V ±	V	4, 7, 12
			2.0/2.1 V ±	V	5, 7, 12
PCI reference		LV_{DD}	5.0 ± 5%	V	2, 10, 11
			3.3 ± 0.3	V	3, 10, 11
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	2, 3
	All other inputs		0 to 3.6	V	6
Die-junction temperature		T_j	0 to 105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PCI pins are designed to withstand LV_{DD} + 5% V DC when LV_{DD} is connected to a 5.0-V DC power supply.
3. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3-V DC power supply.
4. The voltage supply value of 1.8/1.9/2.0 V ± 100 mV applies to parts marked as having a maximum CPU speed of 266 and 300 MHz. See Table 7. For each chosen nominal value (1.8/1.9/2.0 V) the supply voltage should not exceed ± 100 mV of the nominal value.
5. The voltage supply value of 2.0/2.1 V ± 100 m V applies to parts marked as having a maximum CPU speed of 333 and 350 MHz. See Table 7. For each chosen nominal value (2.0/2.1 V) the supply voltage should not exceed ± 100 mV of the nominal value.

Cautions:

6. Input voltage (V_{in}) must not be greater than the supply voltage (V_{DD}/AV_{DD}/$AV_{DD}2$) by more than 2.5 V at all times, including during power-on reset. Input voltage (V_{in}) must not be greater than GV_{DD}/OV_{DD} by more than 0.6 V at all times, including during power-on reset.
7. OV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. V_{DD}/AV_{DD}/$AV_{DD}2$ must not exceed OV_{DD} by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. GV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. LV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
11. LV_{DD} must not exceed OV_{DD} by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
12. This voltage is the input to the filter discussed in Section 7.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

4.3 Power Characteristics

Table 5 provides power consumption data for the MPC8245.

Table 5. Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock/CPU Clock Frequency (MHz)							Unit	Notes
	66/66/266	66/133/266	66/66/300	66/100/300	33/83/333	66/133/333	66/100/350		
Typical	1.7 (1.5)	2.0 (1.8)	1.8 (1.7)	2.0 (1.8)	2.0	2.3	2.2	W	1, 5
Max—FP	2.2 (1.9)	2.4 (2.1)	2.3 (2.0)	2.5 (2.2)	2.6	2.8	2.8	W	1, 2
Max—INT	1.8 (1.6)	2.1 (1.8)	2.0 (1.8)	2.1 (1.8)	2.2	2.4	2.4	W	1, 3
Doze	1.1 (1.0)	1.4 (1.3)	1.2 (1.1)	1.4 (1.3)	1.4	1.6	1.5	W	1, 4, 6
Nap	0.4 (0.4)	0.7 (0.7)	0.4 (0.4)	0.6 (0.6)	0.5	0.7	0.6	W	1, 4, 6
Sleep	0.2 (0.2)	0.4 (0.4)	0.2 (0.4)	0.3 (0.3)	0.3	0.4	0.3	W	1, 4, 6

I/O Power Supplies [10]				
Mode	**Min**	**Max**	**Unit**	**Notes**
Typ—OV_{DD}	134 (121)	334 (301)	mW	7, 8
Typ—GV_{DD}	324 (292)	800 (720)	mW	7, 9

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power. Information on OV_{DD} and GV_{DD} supply power is captured in the I/O power supplies section of this table. Values shown in parenthesis ( ) indicate power consumption at $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V.
2. Maximum—FP power is measured at V_{DD} = 2.1 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 2.1 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 2.1 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at $V_{DD} = AV_{DD}$ = 2.0 V, OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. The typical minimum I/O power values were results of the MPC8245 performing cache resident integer operations at the slowest frequency combination of 33:66:200 (PCI:Mem:CPU) MHz.
8. The typical maximum OV_{DD} value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory.
9. The typical maximum GV_{DD} value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.
10. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW. Guaranteed by design and not tested.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for details on MPC8245 memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

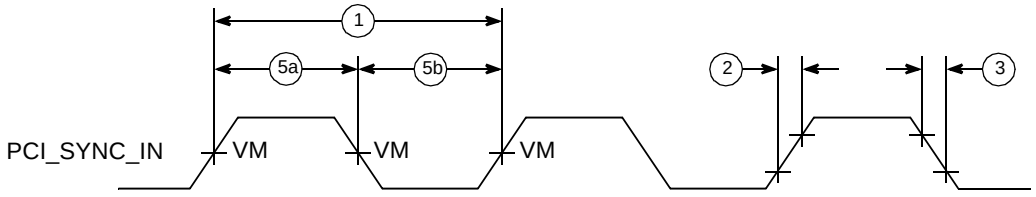


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The gray areas show where the DLL locks.

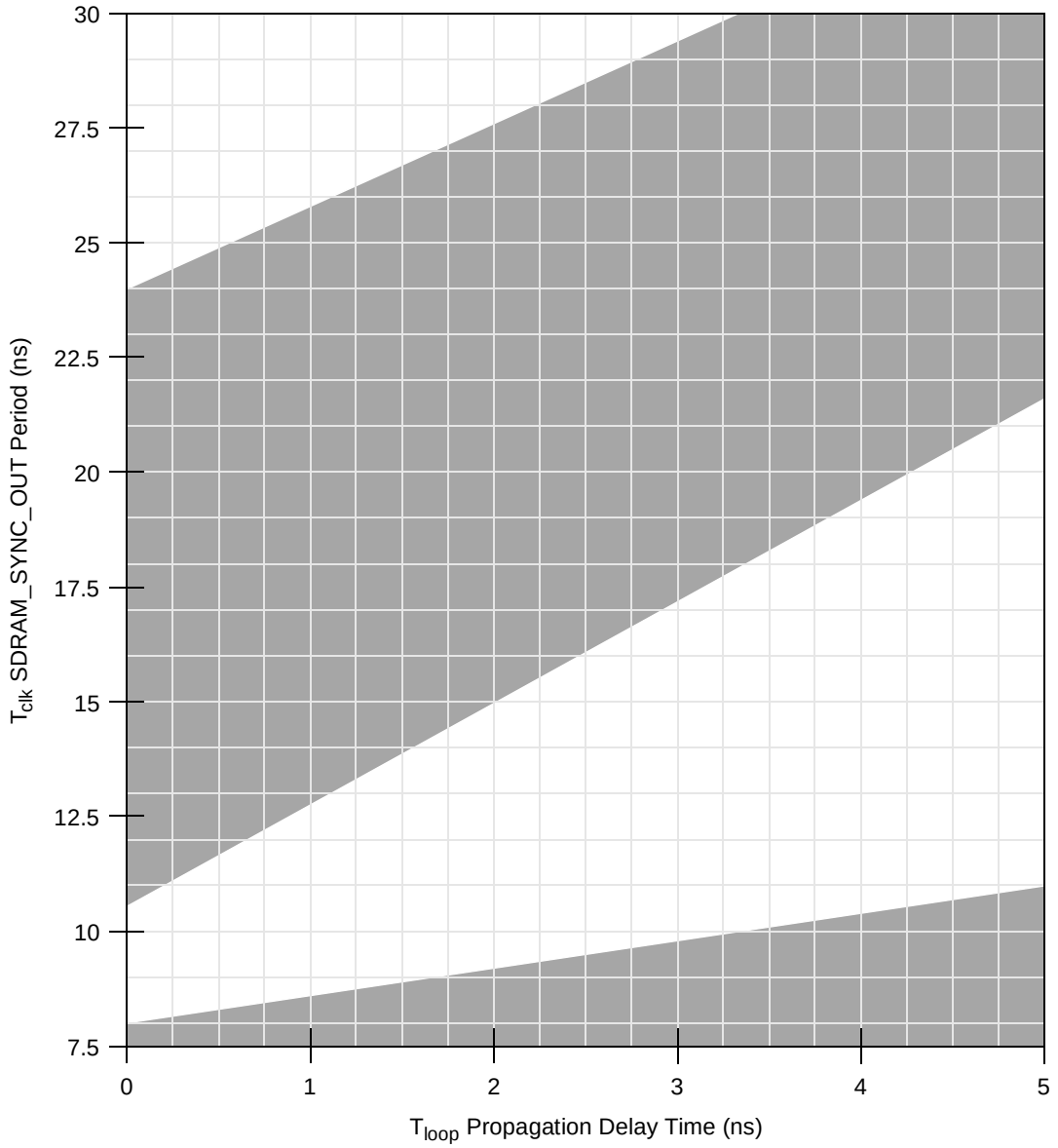


Figure 8. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

Table 13. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8245 provides a delay time of at least 300 ns for the SDA signal (referred to as the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the MPC8245acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA is balanced, the MPC8245 does not cause the unintended generation of a Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8245 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved. It is assumed that the desired I²C SCL clock frequency is 400 KHz and the digital filter sampling rate register (DFFSR bits in I2CFDR) is programmed with its default setting of 0x10 (decimal 16):

SDRAM Clock Frequency	100 MHz	133 MHz
FDR Bit Setting	0x00	0x2A
Actual FDR Divider Selected	384	896
Actual I²C SCL Frequency Generated	260.4 KHz	148.4 KHz

   For details on I²C frequency calculation, refer to the application note AN2919 “Determining the I²C Frequency Divider Ratio for SCL”.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design.

Figure 16 provides the AC test load for the I²C.

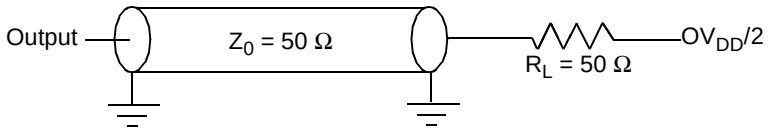


Figure 16. I²C AC Test Load

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN) (continued)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams.

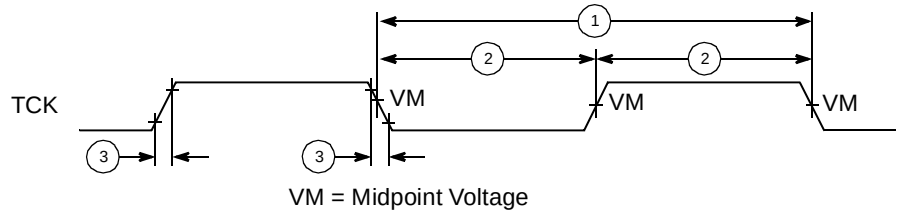


Figure 20. JTAG Clock Input Timing Diagram

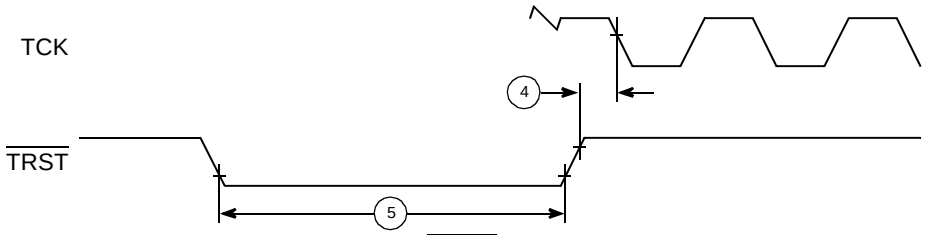


Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

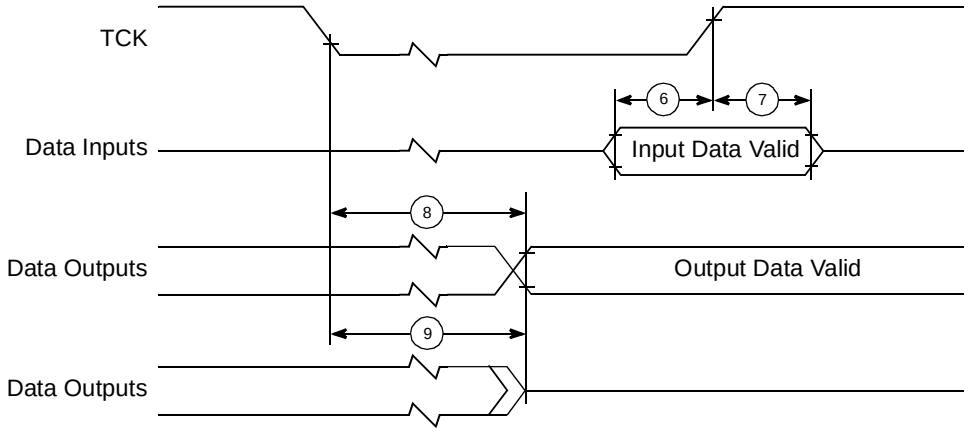


Figure 22. JTAG Boundary Scan Timing Diagram

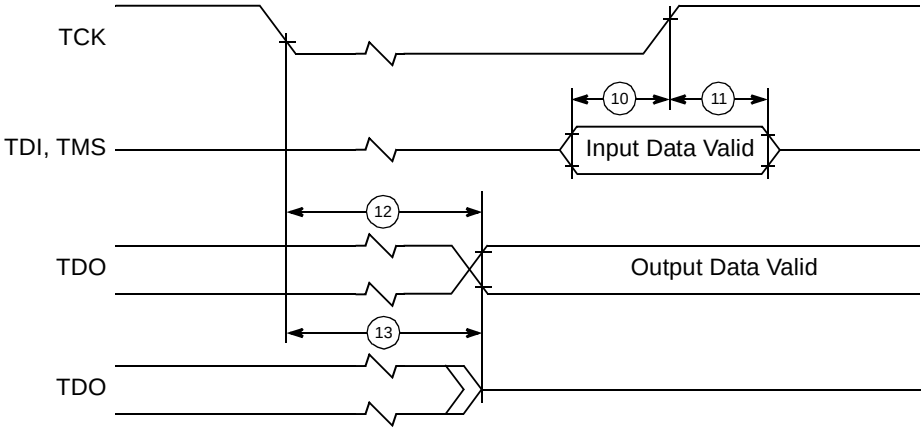


Figure 23. Test Access Port Timing Diagram

5 Package Description

This section details package parameters, pin assignments, and dimensions.

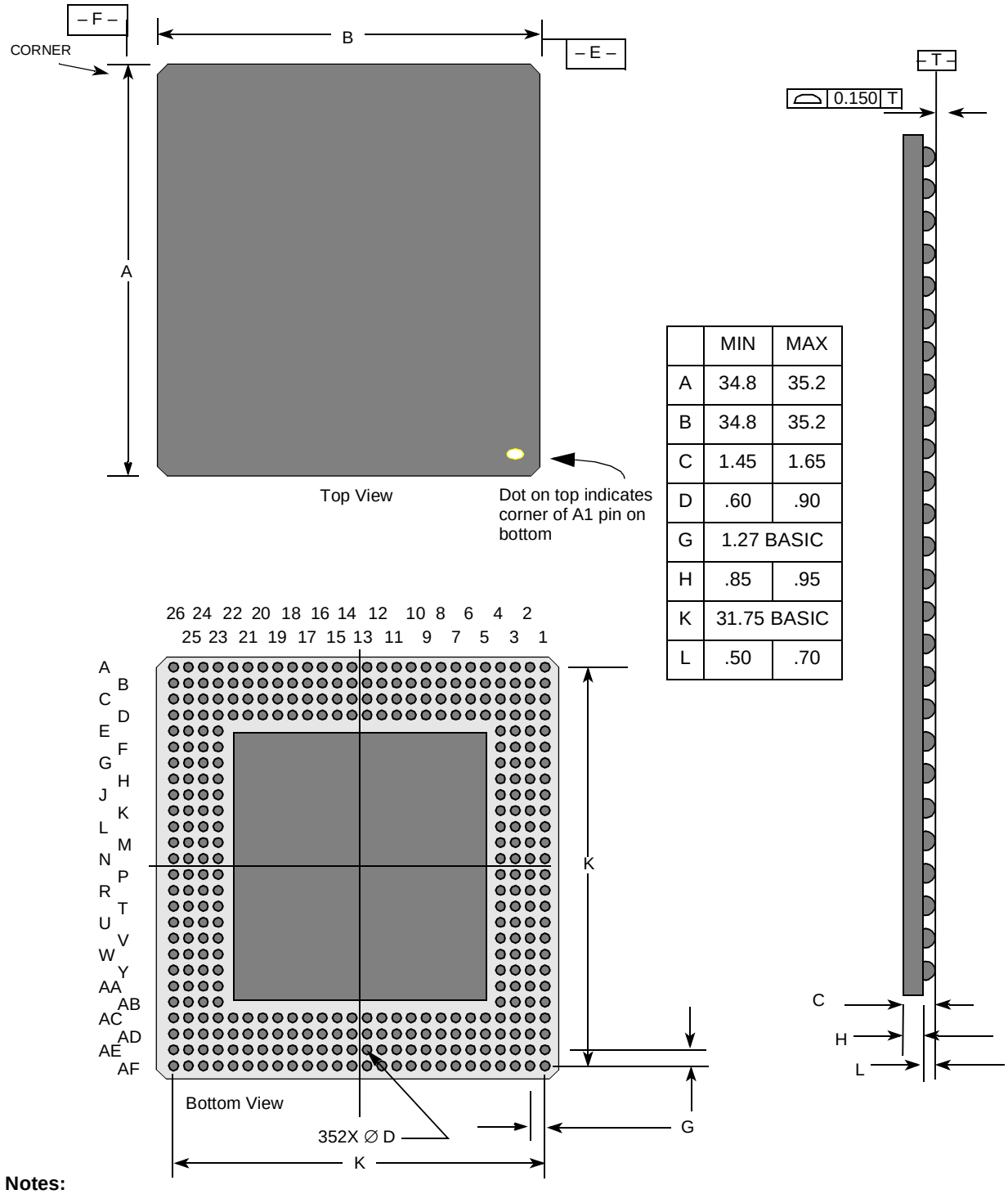
5.1 Package Parameters

The MPC8245 uses a 35 mm × 35 mm, cavity-up, 352-pin tape ball grid array (TBGA) package. The package parameters are as follows.

Package Outline	35 mm × 35 mm
Interconnects	352
Pitch	1.27 mm
Solder Balls	ZU (TBGA package)—62 Sn/36 Pb/2 Ag VV (Lead-free version of package)—95.5 Sn/4.0 Ag/0.5 Cu
Solder Ball Diameter	0.75 mm
Maximum Module Height	1.65 mm
Co-Planarity Specification	0.15 mm
Maximum Force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8245, 352 TBGA package.



	MIN	MAX
A	34.8	35.2
B	34.8	35.2
C	1.45	1.65
D	.60	.90
G	1.27 BASIC	
H	.85	.95
K	31.75 BASIC	
L	.50	.70

Notes:
1. Drawing not to scale.
2. All measurements are in millimeters (mm).

Figure 24. MPC8245 Package Dimensions and Pinout Assignments

5.3 Pinout Listings

Table 16 provides the pinout listing for the MPC8245, 352 TBGA package.

Table 16. MPC8245 Pinout Listing

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{\text{C/BE}}$[3:0]	P25 K23 F23 A25	I/O	OV_{DD}	DRV_PCI	6, 15
$\overline{\text{DEVSEL}}$	H26	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{FRAME}}$	J24	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{IRDY}}$	K25	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{LOCK}}$	J26	Input	OV_{DD}	—	8
AD[31:0]	V25 U25 U26 U24 U23 T25 T26 R25 R26 N26 N25 N23 M26 M25 L25 L26 F24 E26 E25 E23 D26 D25 C26 A26 B26 A24 B24 D19 B23 B22 D22 C22	I/O	OV_{DD}	DRV_PCI	6, 15
PAR	G25	I/O	OV_{DD}	DRV_PCI	15
$\overline{\text{GNT}}$[3:0]	W25 W24 W23 V26	Output	OV_{DD}	DRV_PCI	6, 15
$\overline{\text{GNT4}}$/DA5	W26	Output	OV_{DD}	DRV_PCI	7, 15, 14
$\overline{\text{REQ}}$[3:0]	Y25 AA26 AA25 AB26	Input	OV_{DD}	—	6, 12
$\overline{\text{REQ4}}$/DA4	Y26	I/O	OV_{DD}	—	12, 14
$\overline{\text{PERR}}$	G26	I/O	OV_{DD}	DRV_PCI	8, 15, 18
$\overline{\text{SERR}}$	F26	I/O	OV_{DD}	DRV_PCI	8, 15, 16
$\overline{\text{STOP}}$	H25	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{TRDY}}$	K26	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{INTA}}$	AC26	Output	OV_{DD}	DRV_PCI	10, 15, 16
IDSEL	P26	Input	OV_{DD}	—	
Memory Interface Signals					
MDL[0:31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GV_{DD}	DRV_STD_MEM	5, 6
MDH[0:31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GV_{DD}	DRV_STD_MEM	6

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
V_{DD}	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for core 1.8/2.0 V	V_{DD}	—	22
No Connect	D17	—	—	—	23
AV_{DD}	C17	Power for PLL (CPU core logic) 1.8/2.0 V	AV_{DD}	—	22
$AV_{DD}2$	AF24	Power for PLL (peripheral logic) 1.8/2.0 V	$AV_{DD}2$	—	22
Debug/Manufacturing Pins					
DA0/$\overline{\text{QACK}}$	F2	Output	OV_{DD}	DRV_STD_MEM	4, 10, 25
DA1/CKO	B15	Output	OV_{DD}	DRV_STD_MEM	14
DA2	C25	Output	OV_{DD}	DRV_PCI	2
DA3/PCI_CLK4	AF26	Output	GV_{DD}	DRV_PCI_CLK	14
DA4/$\overline{\text{REQ4}}$	Y26	I/O	OV_{DD}	—	12, 14
DA5/$\overline{\text{GNT4}}$	W26	Output	OV_{DD}	DRV_PCI	7, 15, 14
DA[10:6]/ PLL_CFG[0:4]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
DA[11]	AD26	Output	OV_{DD}	DRV_PCI	2
DA[12:13]	AF17 AF19	Output	OV_{DD}	DRV_STD_MEM	2, 6

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
13	10011[12]	Not available			25[2,7]	100	300	4 (2)	3 (2)
14	10100[12]	26[6]–38[5]	52–76	182–266	26[6]–42[5]	52–84	182–294	2 (4)	3.5 (2)
15	10101[12]	Not available			27[3]–30[5,7]	68–75	272–300	2.5 (2)	4 (2)
16	10110[12]	25–33[5]	50–66	200–264	25–37[5]	50–74	200–296	2 (4)	4 (2)
17	10111[12]	25–33[5]	100–132	200–264	25–33[2]	100–132	200–264	4 (2)	2 (2)
18	11000[12]	27[3]–35[5]	68–88	204–264	27[3]–40[5,7]	68–100	204–300	2.5 (2)	3 (2)
19	11001[12]	36[6]–53[5]	72–106	180–265	36[6]–59[2]	72–118	180–295	2 (2)	2.5 (2)
1A	11010[12]	50[18]–66[1]	50–66	200–264	50[18]–66[1]	50–66	200–264	1 (4)	4 (2)
1B	11011[12]	34[3]–44[5]	68–88	204–264	34[3]–50[5,7]	68–100	204–300	2 (2)	3 (2)
1C	11100[12]	44[3]–59[5]	66–88	198–264	44[3]–66[1]	66–99	198–297	1.5 (2)	3 (2)
1D	11101[12]	48[6]–66[1]	72–99	180–248	48[6]–66[1]	72–99	180–248	1.5 (2)	2.5 (2)
1E Rev B	11110[8]	Not usable			Not usable			Off	Off
1E Rev D	11110	33[3]–38[5]	66–76	231–266	33[3]–42[5]	66–84	231–294	2(2)	3.5(2)

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Not usable			Off	Off

Notes:

1. Limited by the maximum PCI input frequency (66 MHz).
2 Limited by the maximum system memory interface operating frequency (100 MHz @ 300 MHz CPU).
3. Limited by the minimum memory VCO frequency (133 MHz).
4. Limited due to the maximum memory VCO frequency (372 MHz).
5. Limited by the maximum CPU operating frequency.
6. Limited by the minimum CPU VCO frequency (360 MHz).
7. Limited by the maximum CPU VCO frequency (maximum marked CPU speed X 2).
8. In clock-off mode, no clocking occurs inside the MPC8245, regardless of the PCI_SYNC_IN input.
9. Range values are rounded down to the nearest whole number (decimal place accuracy removed).
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting differ from the MPC8240 and are not backward-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting differs from or does not exist on the MPC8240 and may not be fully backward-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
16. Limited by the maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).
17. Limited by the minimum CPU operating frequency (100 MHz).
18. Limited by the minimum memory bus frequency (50 MHz).

Table 18. PLL Configurations (333- and 350-MHz Parts)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–44[16]	75–132	188–330	25–44[16]	75–132	188–330	3 (2)	2.5 (2)
1	00001[12]	25–37[5,7]	75–111	225–333	25–38[5]	75–114	225–342	3 (2)	3 (2)

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

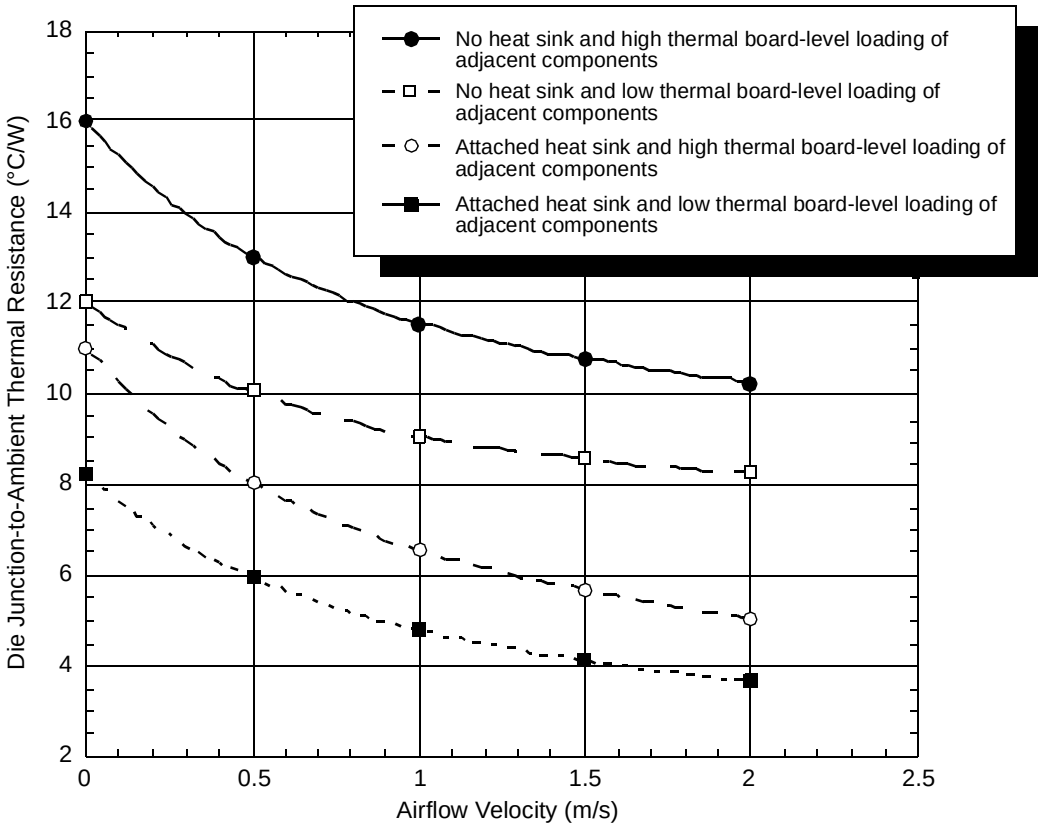


Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material placed between the top of the package and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 30 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 30). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

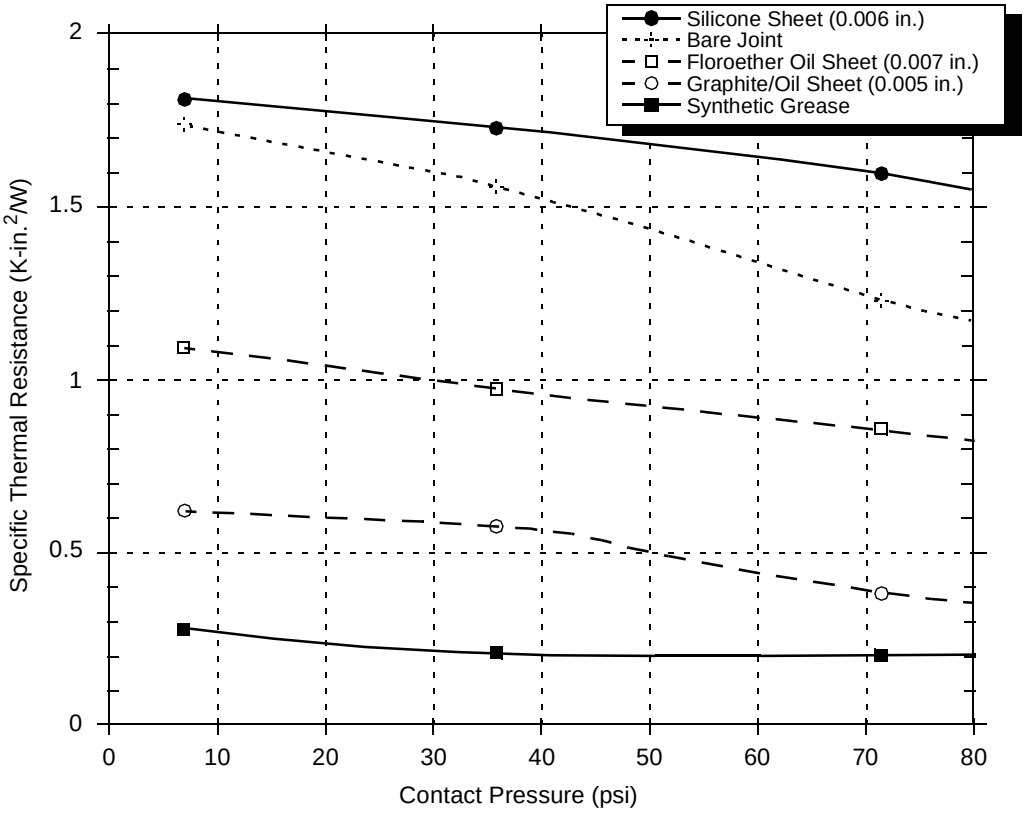


Figure 30. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

7.8.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

8 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Revision History Table

Revision	Date	Substantive Change(s)
10	8/07	Section 3, Table 3, and Table 7—Changed format of recommended voltage supply values so that delta to the chosen nominal does not exceed ± 100 mV. Completely replaced Section 4.6 with compliant I^2C specifications as with other related integrated processor devices.
9	12/27/05	Document—Added Power Architecture information. Section 4.1—Changed increased absolute maximum range for V_{DD} in Table 1. Updated format of nominal voltage listings in Table 2. Section 9.2—Removed Note 3 from Table 21. Updated back page information.
8	11/15/2005	Document—Imported new template and made minor editorial changes. Removed references to a 466 MHz part since it is not available for new orders. Section 4.3.2—Added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated the section to reflect what we offer for new orders. Section 9.3—Added new section, “Part Marking.” Updated Figure 33 to match with current part marking format.
7	10/07/2004	Section 4.1.2—Table 2: Corrected range of AV_{DD} and $AVDD_2$. Section 9.1—Table 21: Corrected voltage range under Process Descriptor column. Minor reformatting.
6.1	05/24/2004	Section 4.5.3—Table 11: Spec 12b was improved from 4.5 ns to 4.0 ns. This improvement is guaranteed on devices marked after work week (WW) 28 of 2004. A device's work week may be determined from the “YYWW” portion of the devices trace ability code which is marked on the top of the device. So for WW28 in 2004, the device’s YYWW is marked as 0428. For more information refer to Figure 33
6	05/11/2004	Section 4.1.2—Table 2: Corrected range of GV_{DD} to 3.3 ± 5%. Section 4.2.1—Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.5.1—Table 8: Changed the wording description for item 15. Section 4.5.2—Table 10: Changed T_{os} range and wording in note; Figure 11:changed wording for SDRAM_SYNC_IN description relative to T_{OS}. Section 4.5.3—Table 11: Changed timing specification for *sys_logic_clk* to output valid (memory control, address, and data signals).
5.1	—	Section 4.3.1—Table 9: Corrected last row to state the correct description for the bit setting. Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
5	—	Section 4.1.2 — Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3 — Table 7, updated specifications for the voltage range of V_{DD} for specific CPU frequencies. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in Test/Configuration signal list and updated relevant notes for signal in Memory Interface signal listing. Updated note #20. Added note 26 for the signals of the UART interface. Section 7.6 — Added reference to AN2128 application note that highlights the differences between the MPC8240 and the MPC8245. Section 7.7 — Added relevant notes to this section and updated Figure 29.
4	—	Section 1.4.1.2—Updated notes for GV_{DD}, AV_{DD}, AV_{DD2}. Section 1.5.1—Updated solder ball information to include lead-free (V V) balls. Section 1.5.3—Updated Note 25 for $\overline{\text{QACK}}$/DA0 signal. Added a sentence to Note 3. Section 1.6 —Incorporated Note 19 into Note 12 and modified Tables 18 and 19 accordingly. Section 1.9—Updated part marking nomenclature where appropriate to include the lead-free offering. Replaced reference to PNS document MPC8245RZUPNS with MPC8245ARZUPNS.
3	—	Section 1.4.1.2—Figure 2: Updated Note 2 and removed ‘voltage regulator delay’ label since Section 1.7.2 is being deleted this revision. Added Figures 4 and 5 to show voltage overshoot and undershoot of the PCI interface on the MPC8245. Section 1.4.1.3—Table 3: Updated the maximum input capacitance from 7 to 16 pF based on characterization data. Section 1.4.3.1—Updated PCI_SYNC_IN jitter specifications to 200 ps. Section 1.4.3.3—Table 11, item 12b: added the word ‘address’ to help clarify which signals the spec applies to. Figure 15: edited timing for items 12a0 and 12a2 to correspond with Table 11. Section 1.5.3—Updated notes for the $\overline{\text{QACK}}$/DA0 signal because this signal has been found to have no internal pull resistor. Section 1.6—Corrected note numbers for reference numbers 3,10,1B, and 1C of the PLL tables. Updated PLL specifications for modes 7 and 1E. Section 1.7.2—Removed this section since the information already exists in Section 1.4.1.5. Section 1.7.4—Added the words ‘the clamping voltage’ to describe LV_{DD} in the sixth paragraph. Changed the $\overline{\text{QACK}}$/DA0 signal from the list of signals having an internal pull-up resistor to the list of signals needing a weak pull-up resistor to OV_{DD}. Section 1.9.1—Tables 21 thru 23: Added processor version register value.

9.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications that supplement and supersede this document. Table 21 shows the part numbers addressed by the MPC8245T*XXnnnx* series. The revision level can be determined by reading the Revision ID register at address offset 0x08.

Table 21. Part Numbers Addressed by MPC8245T*XXnnnx* Series
Part Number Specification Markings
(Document Order No. MPC8245ECS01AD)

MPC	*nnnn*	X	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process Descriptor	Package [1]	Processor Frequency [2]	Revision Level	Processor Version Register Value
MPC	8245	T: –40° to 105°C	ZU = TBGA V V= Lead-free TBGA	266 MHz, 300 MHz: 1.7 V to 2.1 V 333 MHz, 350 MHz: 1.9 V to 2.2 V	D:1.4 Rev ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.

Table 22 shows the part numbers addressed by the MPC8245ARZU*nnnx* series.

Table 22. Part Numbers Addressed by MPC8245ARZU*nnnx* Series
Part Number Specification Markings
(Document Order No. MPC8245ECS02AD)

MPC	*nnnn*	*X*	X	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process [3] Identifier	Process Descriptor	Package [1]	Processor Frequency [2]	Revision Level	Processor Version Register Value
MPC	8245	A	R: 0° to 85°C	ZU = TBGA V V= Lead-free TBGA	400 MHz 2.1 V ± 100 mV	D:1.4 Rev ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.
3. Process identifier ‘A’ represents parts that are manufactured under a 29-angstrom process verses the original 35-angstrom process.