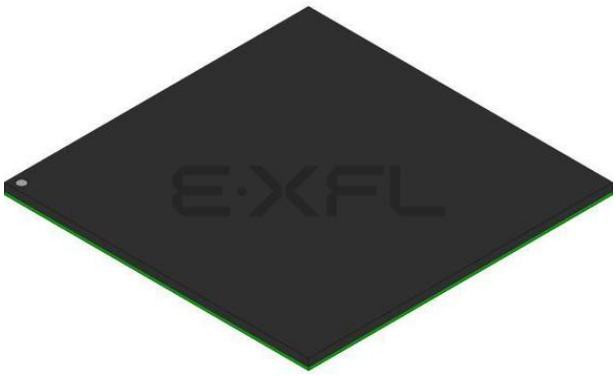

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8245lvv333d

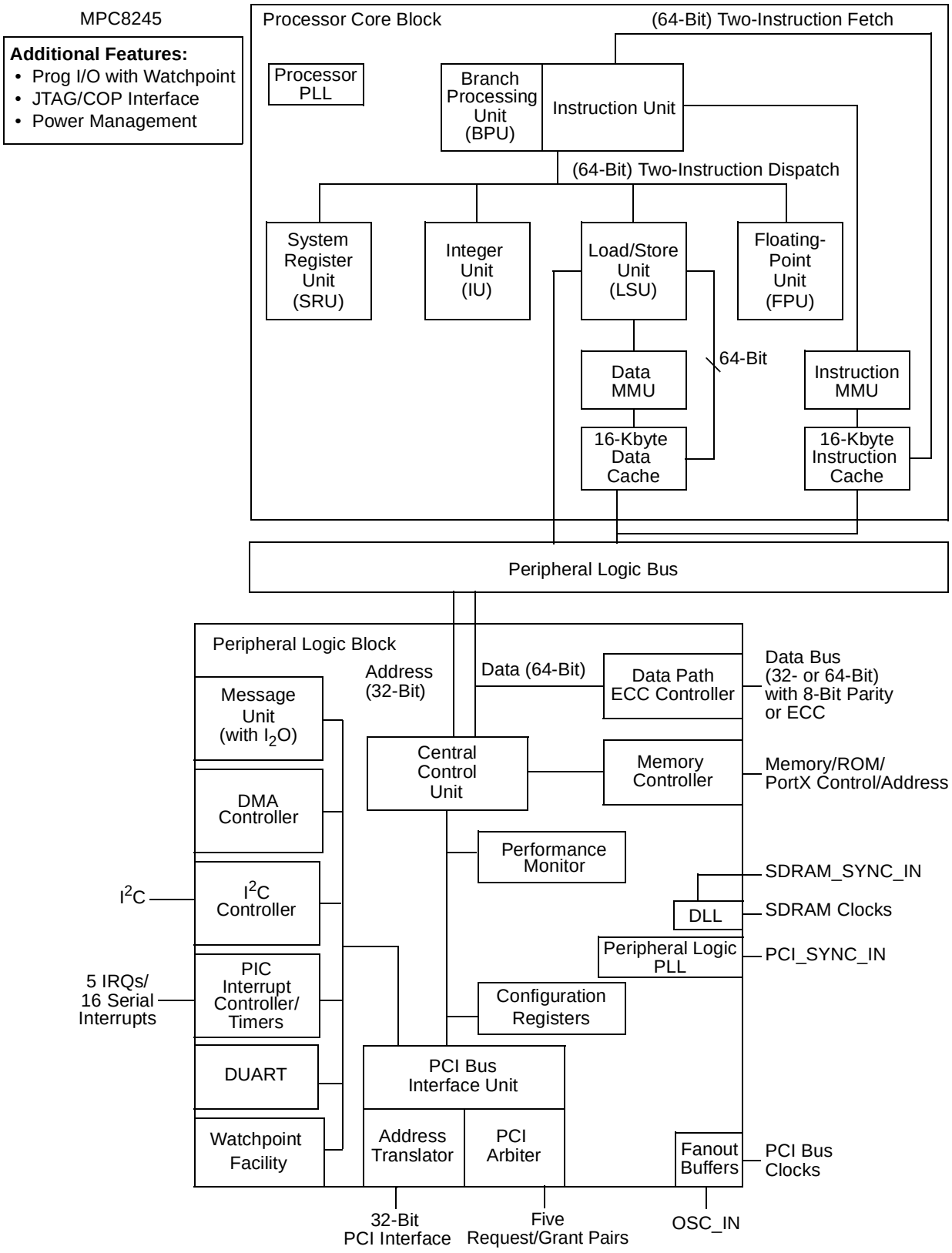


Figure 1. MPC8245 Block Diagram

  - Write buffering for PCI and processor accesses
  - Normal parity, read-modify-write (RMW), or ECC
  - Data-path buffering between memory interface and processor
  - Low-voltage TTL logic (LVTTL) interfaces
  - 272 Mbytes of base and extended ROM/Flash/PortX space
  - Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
  - Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
  - PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects
- 32-bit PCI interface
  - Operates up to 66 MHz
  - PCI 2.2-compatible
  - PCI 5.0-V tolerance
  - Dual address cycle (DAC) for 64-bit PCI addressing (master only)
  - Accesses to PCI memory, I/O, and configuration spaces
  - Selectable big- or little-endian operation
  - Store gathering of processor-to-PCI write and PCI-to-memory write accesses
  - Memory prefetching of PCI read accesses
  - Selectable hardware-enforced coherency
  - PCI bus arbitration unit (five request/grant pairs)
  - PCI agent mode capability
  - Address translation with two inbound and outbound units (ATU)
  - Internal configuration registers accessible from PCI
- Two-channel integrated DMA controller (writes to ROM/PortX not supported)
  - Direct mode or chaining mode (automatic linking of DMA transfers)
  - Scatter gathering—Read or write discontinuous memory
  - 64-byte transfer queue per channel
  - Interrupt on completed segment, chain, and error
  - Local-to-local memory
  - PCI-to-PCI memory
  - Local-to-PCI memory
  - PCI memory-to-local memory
- Message unit
  - Two doorbell registers
  - Two inbound and two outbound messaging registers
  - I_2O message interface
- I^2C controller with full master/slave support that accepts broadcast messages

4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC8245 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.25	V
Supply voltage—memory bus drivers	GV_{DD}	–0.3 to 3.6	V
Supply voltage—PCI and standard I/O buffers	OV_{DD}	–0.3 to 3.6	V
Supply voltage—PLLs	AV_{DD}/AV_{DD} 2	–0.3 to 2.25	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105[3]	°C
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.
3. Note that this temperature range does not apply to the 400 MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8245. Some voltage values do not apply to the 400-MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

Table 2. Recommended Operating Conditions[1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply voltage	V_{DD}	1.8/1.9/2.0 V ± 100 mV	V	4, 7
		2.0/2.1 V ± 100 mV	V	5, 7
I/O buffer supply for PCI and standard	OV_{DD}	3.3 ± 0.3	V	7
Supply voltages for memory bus drivers	GV_{DD}	3.3 ± 5%	V	9
CPU PLL supply voltage	AV_{DD}	1.8/1.9/2.0 V ±	V	4, 7, 12
		2.0/2.1 V ±	V	5, 7, 12

Table 2. Recommended Operating Conditions[1] (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8/1.9/2.0 V ±	V	4, 7, 12
			2.0/2.1 V ±	V	5, 7, 12
PCI reference		LV_{DD}	5.0 ± 5%	V	2, 10, 11
			3.3 ± 0.3	V	3, 10, 11
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	2, 3
	All other inputs		0 to 3.6	V	6
Die-junction temperature		T_j	0 to 105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PCI pins are designed to withstand LV_{DD} + 5% V DC when LV_{DD} is connected to a 5.0-V DC power supply.
3. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3-V DC power supply.
4. The voltage supply value of 1.8/1.9/2.0 V ± 100 mV applies to parts marked as having a maximum CPU speed of 266 and 300 MHz. See Table 7. For each chosen nominal value (1.8/1.9/2.0 V) the supply voltage should not exceed ± 100 mV of the nominal value.
5. The voltage supply value of 2.0/2.1 V ± 100 m V applies to parts marked as having a maximum CPU speed of 333 and 350 MHz. See Table 7. For each chosen nominal value (2.0/2.1 V) the supply voltage should not exceed ± 100 mV of the nominal value.

Cautions:

6. Input voltage (V_{in}) must not be greater than the supply voltage (V_{DD}/AV_{DD}/$AV_{DD}2$) by more than 2.5 V at all times, including during power-on reset. Input voltage (V_{in}) must not be greater than GV_{DD}/OV_{DD} by more than 0.6 V at all times, including during power-on reset.
7. OV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. V_{DD}/AV_{DD}/$AV_{DD}2$ must not exceed OV_{DD} by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. GV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. LV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
11. LV_{DD} must not exceed OV_{DD} by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
12. This voltage is the input to the filter discussed in Section 7.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

Figure 3 shows the undershoot and overshoot voltage of the memory interface.

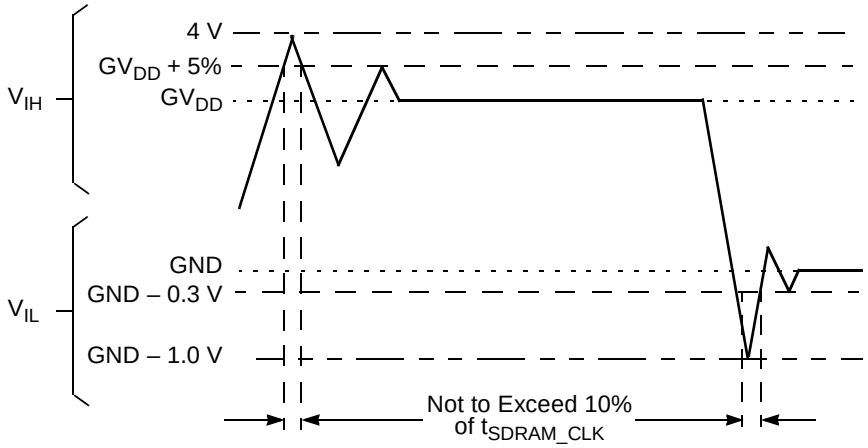


Figure 3. Overshoot/Undershoot Voltage

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the PCI interface for the 3.3- and 5-V signals, respectively.

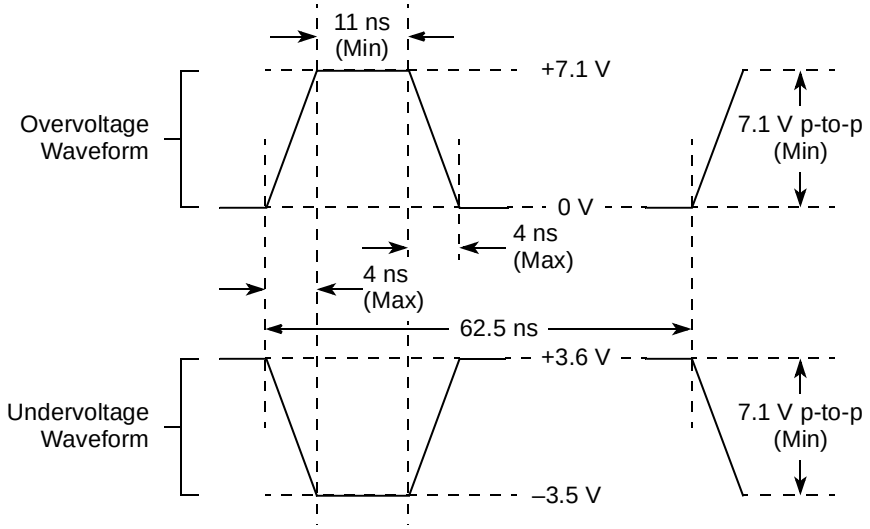


Figure 4. Maximum AC Waveforms for 3.3-V Signaling

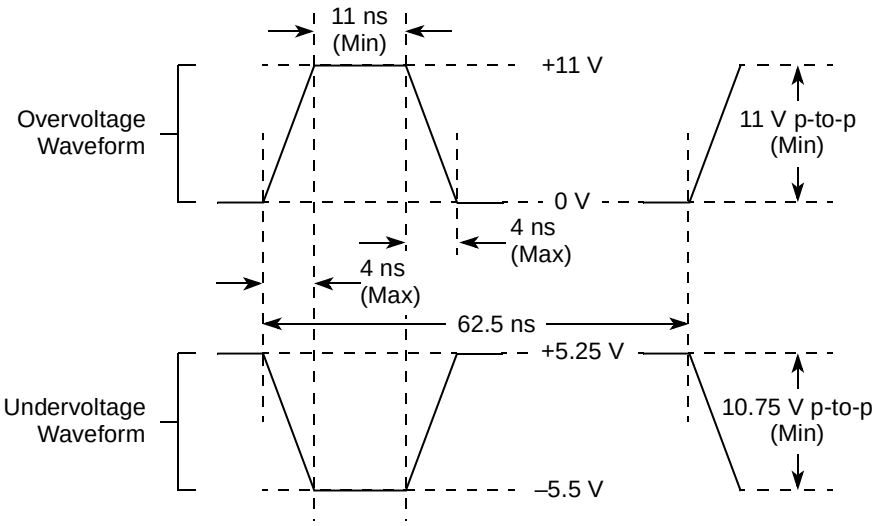


Figure 5. Maximum AC Waveforms for 5-V Signaling

4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8245 at recommended operating conditions.

Table 3. DC Electrical Specifications

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only, except PCI_SYNC_IN	V_{IH}	$0.65 \times OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only, except PCI_SYNC_IN	V_{IL}	—	$0.3 \times OV_{DD}$	V	
Input high voltage	All other pins, including PCI_SYNC_IN (GV_{DD} = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs, including PCI_SYNC_IN	V_{IL}	GND	0.8	V	
Input leakage current for pins using DRV_PCI driver	$0.5\ V \le V_{in} \le 2.7\ V$ @ LV_{DD} = 4.75 V	I_L	—	±70	μA	4
Input leakage current for all others	LV_{DD} = 3.6 V $GV_{DD} \le 3.465$ V	I_L	—	±10	μA	4
Output high voltage	I_{OH} = driver-dependent (GV_{DD} = 3.3 V)	V_{OH}	2.4	—	V	2
Output low voltage	I_{OL} = driver-dependent (GV_{DD} = 3.3 V)	V_{OL}	—	0.4	V	2

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8245. For details, see Section 7.8, "Thermal Management."

Table 6. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection (Single-layer board—1s)	$R_{\theta JA}$	16.1	°C/W	1, 2
Junction-to-ambient natural convection (Four-layer board—2s2p)	$R_{\theta JMA}$	12.0	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Single-layer board—1s)	$R_{\theta JMA}$	11.6	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Four layer board—2s2p)	$R_{\theta JMA}$	9.0	°C/W	1, 3
Junction-to-board	$R_{\theta JB}$	4.8	°C/W	4
Junction-to-case	$R_{\theta JC}$	1.8	°C/W	5
Junction-to-package top (natural convection)	Ψ_{JT}	1.0	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate used for case temperature.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 9, "Ordering Information," for details on ordering parts.

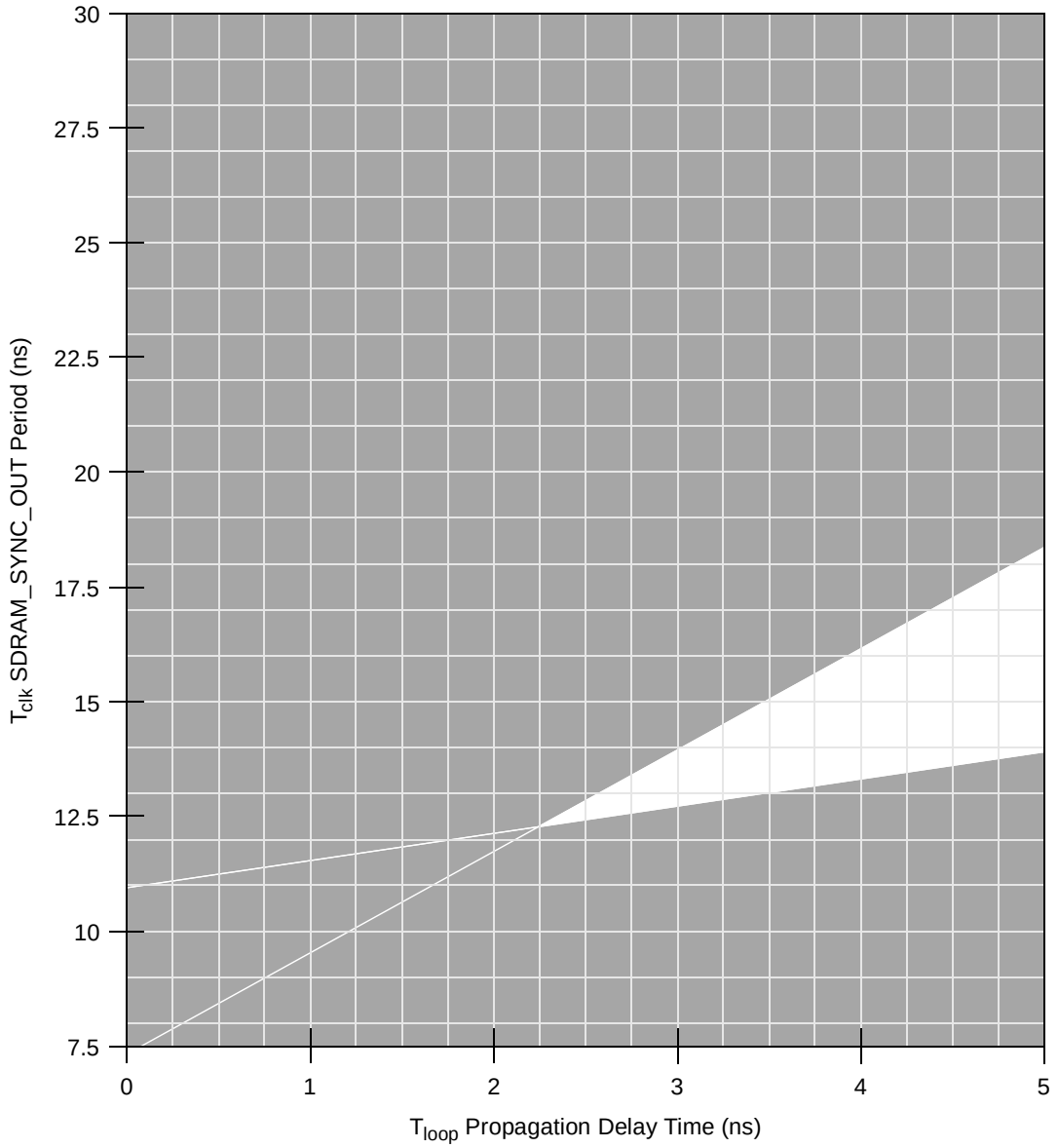
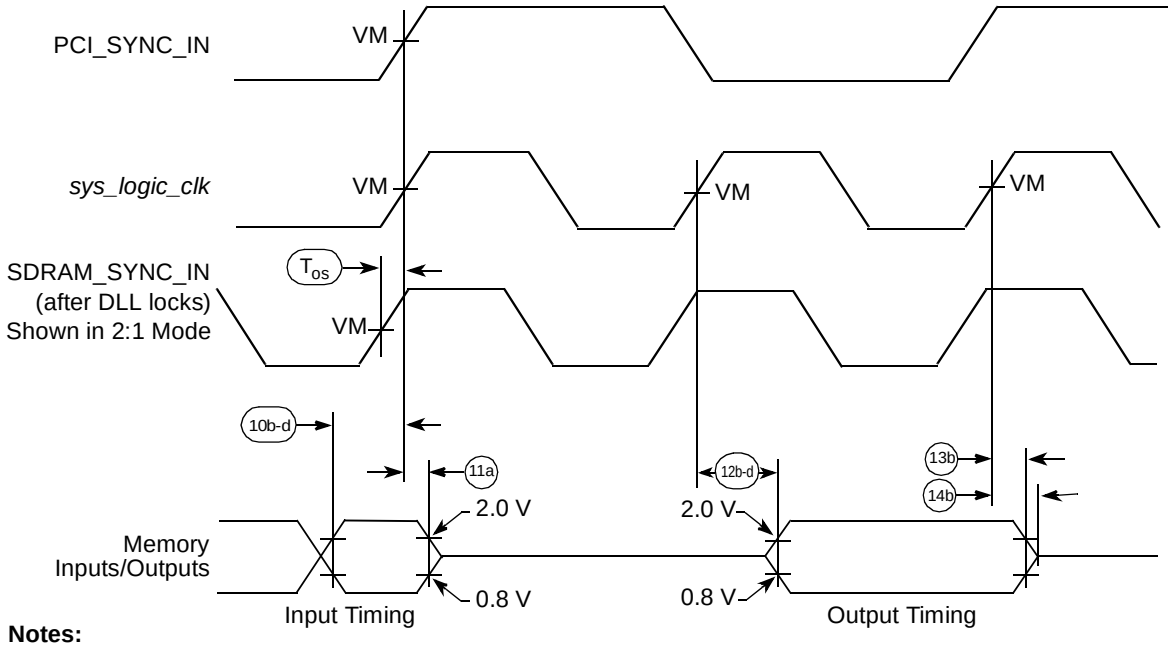


Figure 10. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=1 and Max Tap Delay

4.5.2 Input AC Timing Specifications

Table 10 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V.

Figure 11 and Figure 12 show the input/output timing diagrams referenced to SDRAM_SYNC_IN and PCI_SYNC_IN, respectively.



Notes:
VM = Midpoint voltage (1.4 V).
10b-d = Input signals valid timing.
11a = Input hold time of SDRAM_SYNC_IN to memory.
12b-d = *sys_logic_clk* to output valid timing.
13b = Output hold time for non-PCI signals.
14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.
T_{os} = Offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to appear before *sys_logic_clk* once the DLL locks.

Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN

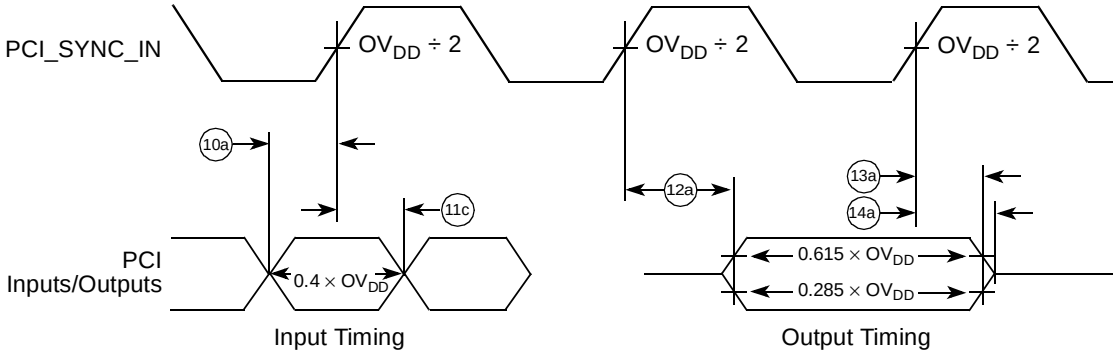


Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

Figure 13 shows the input timing diagram for mode select signals.

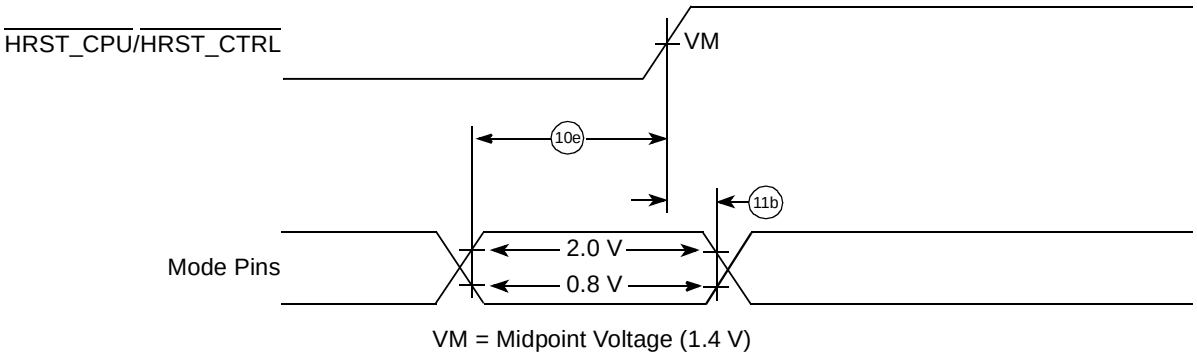


Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 for the input/output timing diagram referenced to *sys_logic_clk*. All output timings assume a purely resistive 50-Ω load (see Figure 14 for the AC test load for the MPC8245). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths indicated in Table 4.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory control, address, and data signals)	—	4.0	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/PortX)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66-MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33-MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

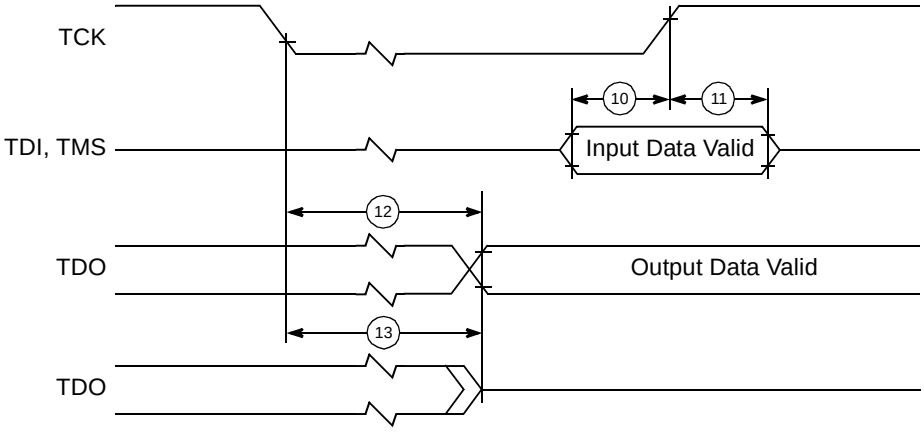


Figure 23. Test Access Port Timing Diagram

5 Package Description

This section details package parameters, pin assignments, and dimensions.

5.1 Package Parameters

The MPC8245 uses a 35 mm × 35 mm, cavity-up, 352-pin tape ball grid array (TBGA) package. The package parameters are as follows.

Package Outline	35 mm × 35 mm
Interconnects	352
Pitch	1.27 mm
Solder Balls	ZU (TBGA package)—62 Sn/36 Pb/2 Ag VV (Lead-free version of package)—95.5 Sn/4.0 Ag/0.5 Cu
Solder Ball Diameter	0.75 mm
Maximum Module Height	1.65 mm
Co-Planarity Specification	0.15 mm
Maximum Force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DA[14:15]	F1 J2	Output	GV_{DD}	DRV_MEM_CTRL	2, 6

Notes:

1. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
2. Treat these pins as no connects (NC) unless debug address functionality is used.
3. This pin has an internal pull-up resistor that is enabled only in the reset state. The value of the internal pull-up resistor is not guaranteed but is sufficient to ensure that a logic 1 is read into configuration bits during reset if the signal is left unterminated.
4. This pin is a reset configuration pin.
5. DL[0] is a reset configuration pin with an internal pull-up resistor that is enabled only in the reset state. The value of the internal pull-up resistor is not guaranteed but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
6. Multi-pin signals such as AD[31:0] and MDL[0:31] have their physical package pin numbers listed in an order corresponding to the signal names. Example: AD0 is on pin C22, AD1 is on pin D22, ..., AD31 is on pin V25.
7. $\overline{\text{GNT4}}$ is a reset configuration pin with an internal pull-up resistor that is enabled only in the reset state.
8. A weak pull-up resistor (2–10 kΩ) should be placed on this PCI control pin to LV_{DD}.
9. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
10. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
11. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to GV_{DD}.
12. This pin has an internal pull-up resistor that is enabled at all times. The value of the internal pull-up resistor is not guaranteed but is sufficient to prevent unused inputs from floating.
13. An external PCI clocking source or fan-out buffer may be required for the MPC8245 DUART functionality since PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
14. This pin is a multiplexed signal and appears more than once in this table.
15. This pin is affected by the programmable PCI_HOLD_DEL parameter.
16. This pin is an open-drain signal.
17. This pin can be programmed as driven (default) or as open-drain (in MIOCR 1).
18. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification.*
19. OSC_IN uses the 3.3-V PCI interface driver, which is 5-V tolerant. See Table 2 for details.
20. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST\_CTRL}}$ and $\overline{\text{HRST\_CPU}}$ in order to be latched.
21. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev 1.1 (A). These signals use DRV_MEM_CLK for chip Rev 1.2 (B).
22. The 266- and 300-MHz part offerings can run at a source voltage of 1.8 ± 100 mV or 2.0 ± 100 mV. Source voltage should be 2.0 ± 100 mV for 333- and 350-MHz parts.
23. This pin is LAVDD on the MPC8240. It is an NC on the MPC8245, which should not pose a problem when an MPC8240 is replaced with an MPC8245.
24. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.
25. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD} so that a 1 can be detected at reset if an external memory clock is not used and PLL[0:4] does not select a half-clock frequency ratio.
26. Typically, the serial port has sufficient drivers in the RS232 transceiver to drive the $\overline{\text{CTS}}$ pin actively as an input. No pullups are needed in this case.
27. $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic 0 level is read into the configuration bits during reset if the default logic 1 level is not desired.

Any other unused active low input pins should be tied to a logic-one level through weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND through weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8245 PCI reference voltage (LV_{DD}) pins should be connected to a 3.3 ± 0.3 V power supply if interfacing the MPC8245 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to a 5.0 V ± 5% power supply if interfacing the MPC8245 into a 5-V PCI bus system. For either reference voltage, the MPC8245 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8245 tolerates 5-V signals when interfaced into a 5-V PCI bus system.

7.6 MPC8245 Compatibility with MPC8240

The MPC8245 AC timing specifications are backward-compatible with those of the MPC8240, except for the requirements of item 11 in Table 10. Timing adjustments are needed as specified for T_{os} (SDRAM_SYNC_IN to *sys_logic_clk* offset) time requirements.

The MPC8245 does not support the SDRAM flow-through memory interface.

The nominal core V_{DD} power supply changes from 2.5 V on the MPC8240 to 1.8/2.0 V on the MPC8245. See Table 2.

For example, the MPC8245 PLL_CFG[0:4] setting 0x02 (0b00010) has a different PCI-to-Mem and Mem-to-CPU multiplier ratio than the same setting on the MPC8240, so it is not backward-compatible. See Table 17.

Most of the MPC8240 PLL_CFG[0:4] settings are subsets of the PCI_SYNC_IN input frequency range accepted by the MPC8245. However, the parts are not fully backward-compatible since the ranges of the two parts do not always match. Modes 0x8 and 0x18 of the MPC8245 are not compatible with settings 0x8 and 0x18 on the MPC8240. See Table 17 and Table 18.

Two reset configuration signals on the MPC8245 are not used as reset configuration signals on the MPC8240: SDMA0 and SDMA1.

The SDMA0 reset configuration pin selects between the MPC8245 DUART and the MPC8240 backward-compatible mode PCI_CLK[0:4] functionality on these multiplexed signals. The default state (logic 1) of SDMA0 selects the MPC8240 backward-compatible mode of PCI_CLK[0:4] functionality while a logic 0 state on the SDMA0 signal selects DUART functionality. In DUART mode, four of the five PCI clocks, PCI_CLK[0:3], are not available.

The SDMA1 reset configuration pin selects between MPC8245 extended ROM functionality and MPC8240 backward-compatible functionality on the multiplexed signals: TBEN, $\overline{\text{CHKSTOP\_IN}}$,

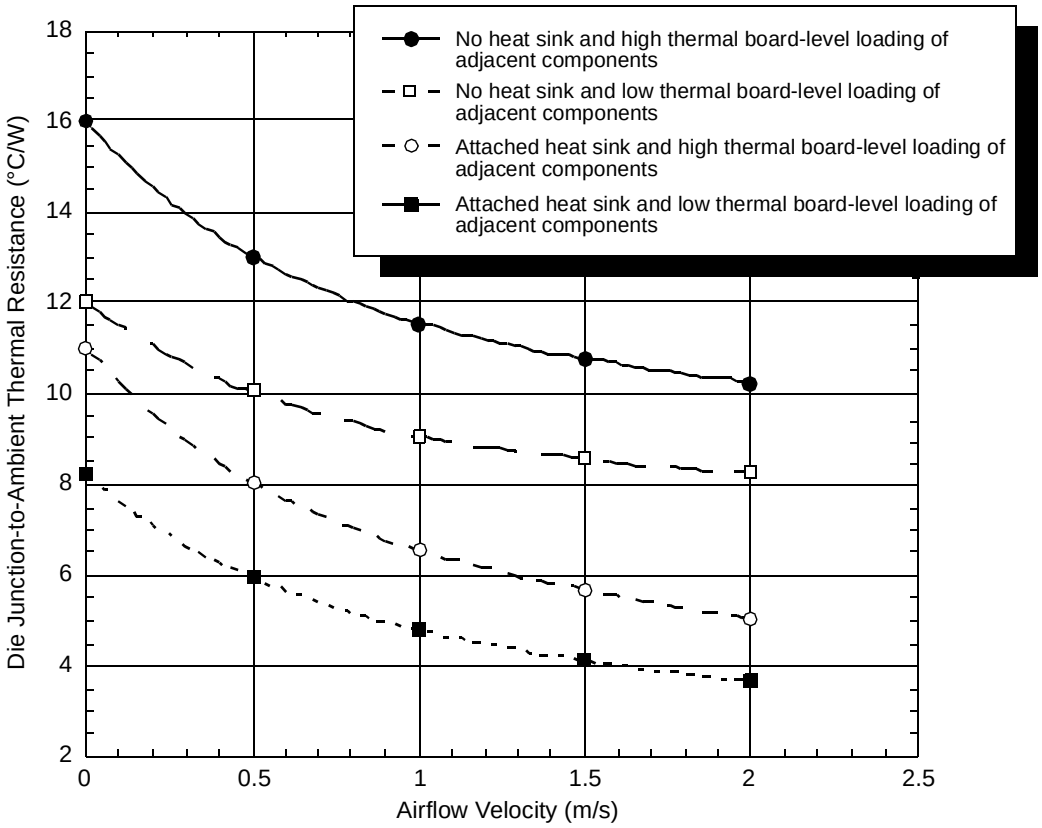


Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances and may or may not need airflow.

7.8.1 Internal Package Conduction Resistance

The intrinsic conduction thermal resistance paths for the TBGA cavity-down packaging technology shown in Figure 29 are as follows:

- Die junction-to-case thermal resistance
- Die junction-to-ball thermal resistance

Figure 29 depicts the primary heat transfer path for a package with an attached heat sink mounted on a printed-circuit board.

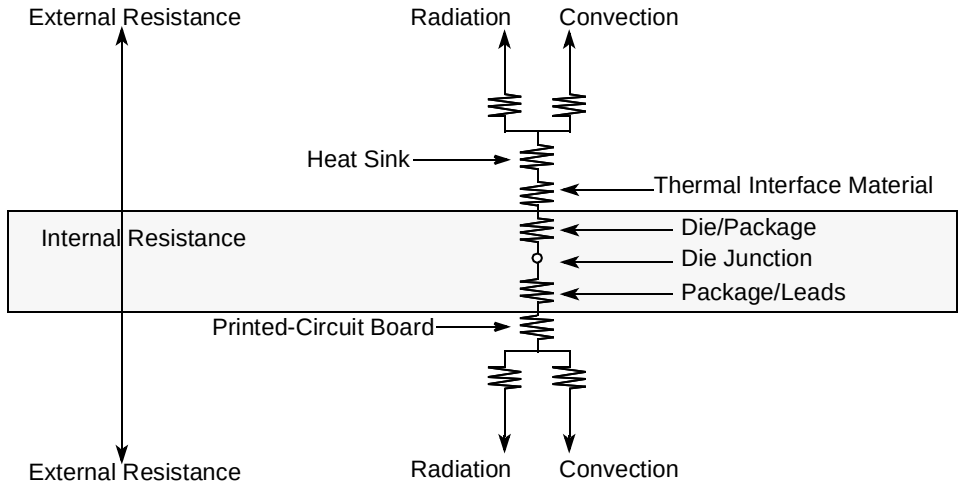


Figure 29. TBGA Package with Heat Sink Mounted to a Printed-Circuit Board

In a TBGA package, the active side of the die faces the printed-circuit board. Most of the heat travels through the die, across the die attach layer, and into the copper spreader. Some of the heat is removed from the top surface of the spreader through convection and radiation. Another percentage of the heat enters the printed-circuit board through the solder balls. The heat is then removed from the exposed surfaces of the board through convection and radiation. If a heat sink is used, a larger percentage of heat leaves through the top side of the spreader.

8 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Revision History Table

Revision	Date	Substantive Change(s)
10	8/07	Section 3, Table 3, and Table 7—Changed format of recommended voltage supply values so that delta to the chosen nominal does not exceed ± 100 mV. Completely replaced Section 4.6 with compliant I^2C specifications as with other related integrated processor devices.
9	12/27/05	Document—Added Power Architecture information. Section 4.1—Changed increased absolute maximum range for V_{DD} in Table 1. Updated format of nominal voltage listings in Table 2. Section 9.2—Removed Note 3 from Table 21. Updated back page information.
8	11/15/2005	Document—Imported new template and made minor editorial changes. Removed references to a 466 MHz part since it is not available for new orders. Section 4.3.2—Added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated the section to reflect what we offer for new orders. Section 9.3—Added new section, “Part Marking.” Updated Figure 33 to match with current part marking format.
7	10/07/2004	Section 4.1.2—Table 2: Corrected range of AV_{DD} and $AVDD_2$. Section 9.1—Table 21: Corrected voltage range under Process Descriptor column. Minor reformatting.
6.1	05/24/2004	Section 4.5.3—Table 11: Spec 12b was improved from 4.5 ns to 4.0 ns. This improvement is guaranteed on devices marked after work week (WW) 28 of 2004. A device's work week may be determined from the “YYWW” portion of the devices trace ability code which is marked on the top of the device. So for WW28 in 2004, the device’s YYWW is marked as 0428. For more information refer to Figure 33
6	05/11/2004	Section 4.1.2—Table 2: Corrected range of GV_{DD} to 3.3 ± 5%. Section 4.2.1—Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.5.1—Table 8: Changed the wording description for item 15. Section 4.5.2—Table 10: Changed T_{os} range and wording in note; Figure 11:changed wording for SDRAM_SYNC_IN description relative to T_{OS}. Section 4.5.3—Table 11: Changed timing specification for *sys_logic_clk* to output valid (memory control, address, and data signals).
5.1	—	Section 4.3.1—Table 9: Corrected last row to state the correct description for the bit setting. Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”

9.3 Part Marking

Parts are marked as the example shown in Figure 31.

Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is test traceability code.
YWWLAZ is the assembly traceability code.
CCCCC is the country code.

Figure 31. Part Marking for TBGA Device

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