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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC 603e |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 350MHz |
| Co-Processors/DSP | - |
| RAM Controllers | SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 352-LBGA Exposed Pad |
| Supplier Device Package | 352-TBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8245lvv350d |

  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System-level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—Marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std 1149.1® (JTAG)/test interface

# 3 General Parameters

The following list summarizes the general parameters of the MPC8245:

| | |
|---|---|
| Technology | 0.25-µm CMOS, five-layer metal |
| Die size | 49.2 $mm^2$ |
| Transistor count | 4.5 million |
| Logic design | Fully-static |
| Packages | Surface-mount 352 tape ball grid array (TBGA) |
| Core power supply | 1.7 V to 2.1 V DC for 266 and 300 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 1.8/1.9/2.0 volts.<br>1.9 V to 2.2 V DC for 333 and 350 MHz with the condition that the usage is “nominal” ± 100 mV where “nominal” is 2.0/2.1 volts.<br>See Table 2 for details of recommended operating conditions) |
| I/O power supply | 3.0- to 3.6-V DC |

# 4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8245.

## 4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other DC electrical characteristics.

Figure 3 shows the undershoot and overshoot voltage of the memory interface.

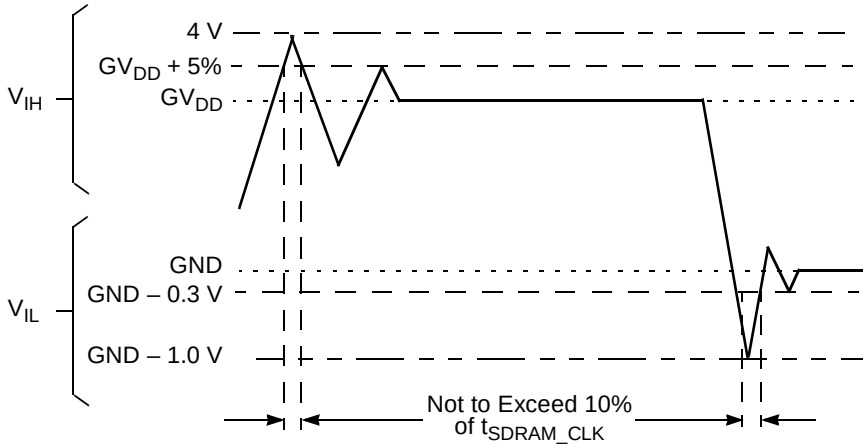



**Figure 3. Overshoot/Undershoot Voltage**

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the PCI interface for the 3.3- and 5-V signals, respectively.

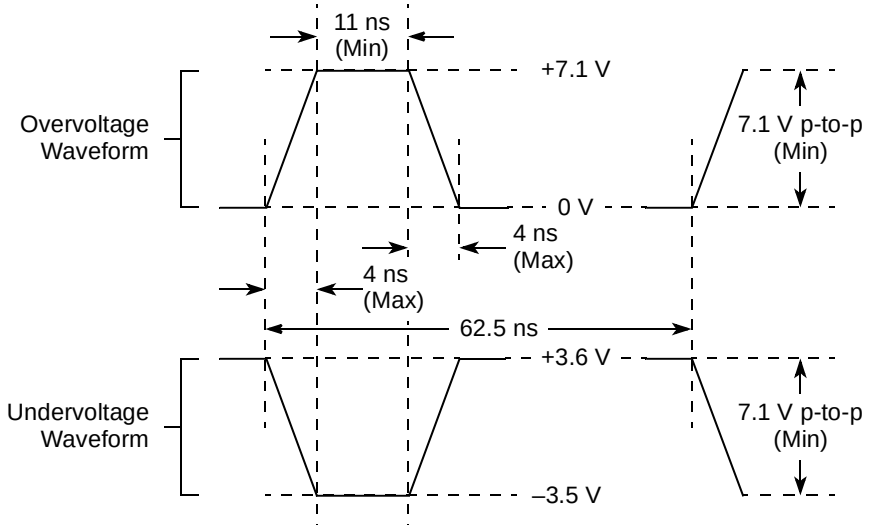



**Figure 4. Maximum AC Waveforms for 3.3-V Signaling**

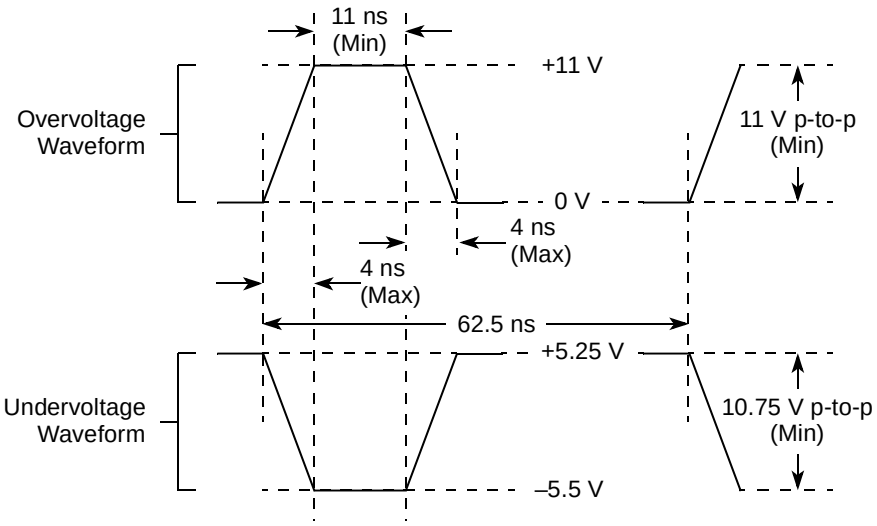



**Figure 5. Maximum AC Waveforms for 5-V Signaling**

## 4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8245 at recommended operating conditions.

**Table 3. DC Electrical Specifications**

At recommended operating conditions (see Table 2)

| Characteristic | Condition [3] | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage | PCI only, except PCI_SYNC_IN | $V_{IH}$ | $0.65 \times OV_{DD}$ | $LV_{DD}$ | V | 1 |
| Input low voltage | PCI only, except PCI_SYNC_IN | $V_{IL}$ | — | $0.3 \times OV_{DD}$ | V | |
| Input high voltage | All other pins, including PCI_SYNC_IN ($GV_{DD}$ = 3.3 V) | $V_{IH}$ | 2.0 | 3.3 | V | |
| Input low voltage | All inputs, including PCI_SYNC_IN | $V_{IL}$ | GND | 0.8 | V | |
| Input leakage current for pins using DRV_PCI driver | $0.5\ V \le V_{in} \le 2.7\ V$ @ $LV_{DD}$ = 4.75 V | $I_L$ | — | ±70 | μA | 4 |
| Input leakage current for all others | $LV_{DD}$ = 3.6 V $GV_{DD} \le 3.465$ V | $I_L$ | — | ±10 | μA | 4 |
| Output high voltage | $I_{OH}$ = driver-dependent ($GV_{DD}$ = 3.3 V) | $V_{OH}$ | 2.4 | — | V | 2 |
| Output low voltage | $I_{OL}$ = driver-dependent ($GV_{DD}$ = 3.3 V) | $V_{OL}$ | — | 0.4 | V | 2 |

## 4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8245. For details, see Section 7.8, "Thermal Management."

**Table 6. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection (Single-layer board—1s) | $R_{\theta JA}$ | 16.1 | °C/W | 1, 2 |
| Junction-to-ambient natural convection (Four-layer board—2s2p) | $R_{\theta JMA}$ | 12.0 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) (Single-layer board—1s) | $R_{\theta JMA}$ | 11.6 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) (Four layer board—2s2p) | $R_{\theta JMA}$ | 9.0 | °C/W | 1, 3 |
| Junction-to-board | $R_{\theta JB}$ | 4.8 | °C/W | 4 |
| Junction-to-case | $R_{\theta JC}$ | 1.8 | °C/W | 5 |
| Junction-to-package top (natural convection) | $\Psi_{JT}$ | 1.0 | °C/W | 6 |

**Notes:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate used for case temperature.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 9, "Ordering Information," for details on ordering parts.

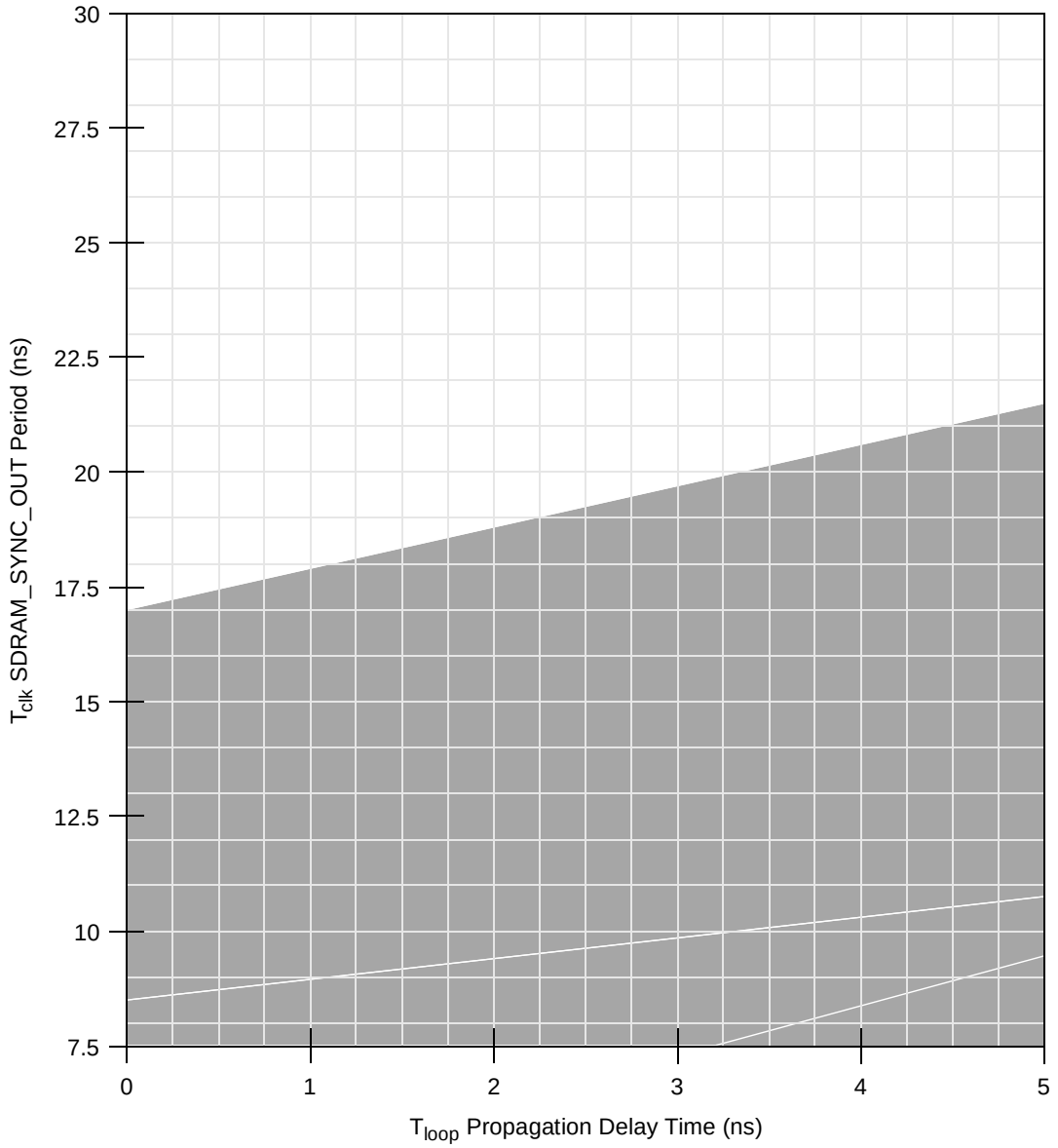



**Figure 9. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay**

Figure 13 shows the input timing diagram for mode select signals.

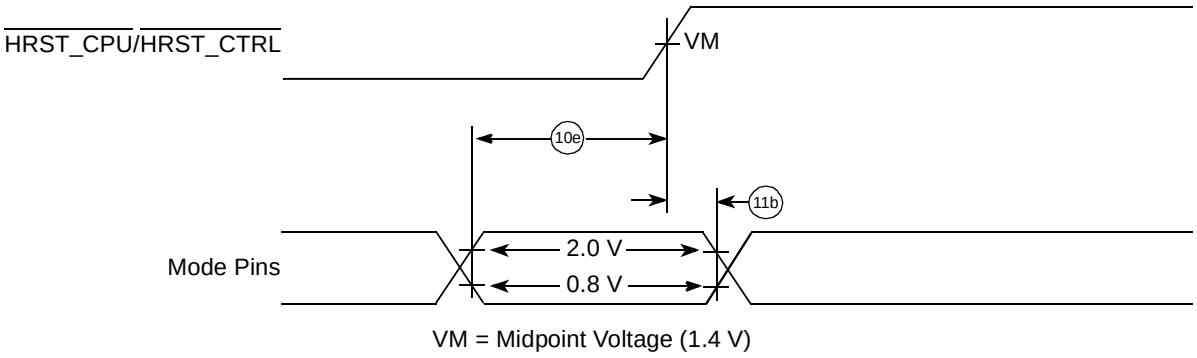



**Figure 13. Input Timing Diagram for Mode Select Signals**

## 4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with $LV_{DD}$ = 3.3 V ± 0.3 V. See Figure 11 for the input/output timing diagram referenced to *sys_logic_clk*. All output timings assume a purely resistive 50-Ω load (see Figure 14 for the AC test load for the MPC8245). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths indicated in Table 4.

**Table 11. Output AC Timing Specifications**

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 12a | PCI_SYNC_IN to output valid, see Figure 15 | | | | |
| 12a0 | Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default) | — | 6.0 | ns | 1, 3 |
| 12a1 | Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10 | — | 6.5 | | |
| 12a2 | Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI | — | 7.0 | | |
| 12a3 | Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00 | — | 7.5 | | |
| 12b | *sys_logic_clk* to output valid (memory control, address, and data signals) | — | 4.0 | ns | 2 |
| 12c | *sys_logic_clk* to output valid (for all others) | — | 7.0 | ns | 2 |
| 12d | *sys_logic_clk* to output valid (for $I^2C$) | — | 5.0 | ns | 2 |
| 12e | *sys_logic_clk* to output valid (ROM/Flash/PortX) | — | 6.0 | ns | 2 |
| 13a | Output hold (PCI), see Figure 15 | | | | |
| 13a0 | Tap 0, PCI_HOLD_DEL=00, [$\overline{\text{MCP}}$,CKE] = 11, 66-MHz PCI (default) | 2.0 | — | ns | 1, 3, 4 |
| 13a1 | Tap 1, PCI_HOLD_DEL=01, [$\overline{\text{MCP}}$,CKE] = 10 | 2.5 | — | | |
| 13a2 | Tap 2, PCI_HOLD_DEL=10, [$\overline{\text{MCP}}$,CKE] = 01, 33-MHz PCI | 3.0 | — | | |
| 13a3 | Tap 3, PCI_HOLD_DEL=11, [$\overline{\text{MCP}}$,CKE] = 00 | 3.5 | — | | |
| 13b | Output hold (all others) | 1.0 | — | ns | 2 |
| 14a | PCI_SYNC_IN to output high impedance (for PCI) | — | 14.0 | ns | 1, 3 |

**Table 11. Output AC Timing Specifications (continued)**

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 14b | *sys_logic_clk* to output high impedance (for all others) | — | 4.0 | ns | 2 |

**Notes:**

1. All PCI signals are measured from $GV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times OV_{DD}$ or $0.615 \times OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[3:0], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[31:0], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], IDSEL, and $\overline{\text{INTA}}$.
4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8245 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals; the values on these two signals are inverted and stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Since $\overline{\text{MCP}}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. Figure 15 shows the PCI_HOLD_DEL effect on output valid and hold times.

Figure 14 provides the AC test load for the MPC8245.

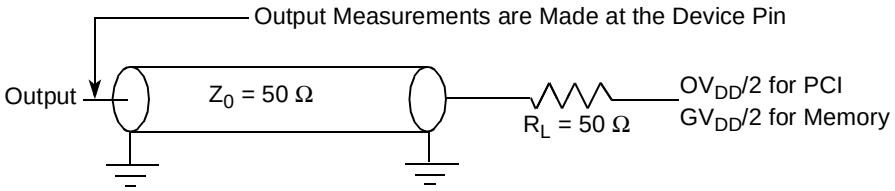



**Figure 14. AC Test Load for the MPC8245**

**Table 13. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 12).

| Parameter | Symbol [1] | Min | Max | Unit |
|---|---|---|---|---|
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8245 provides a delay time of at least 300 ns for the SDA signal (referred to as the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the MPC8245acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA is balanced, the MPC8245 does not cause the unintended generation of a Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8245 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved. It is assumed that the desired I²C SCL clock frequency is 400 KHz and the digital filter sampling rate register (DFFSR bits in I2CFDR) is programmed with its default setting of 0x10 (decimal 16):

   | | | |
   |---|---|---|
   | SDRAM Clock Frequency | 100 MHz | 133 MHz |
   | FDR Bit Setting | 0x00 | 0x2A |
   | Actual FDR Divider Selected | 384 | 896 |
   | Actual I²C SCL Frequency Generated | 260.4 KHz | 148.4 KHz |

   For details on I²C frequency calculation, refer to the application note AN2919 “Determining the I²C Frequency Divider Ratio for SCL”.
3. The maximum $t_{I2DXKL}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. Guaranteed by design.

Figure 16 provides the AC test load for the I²C.

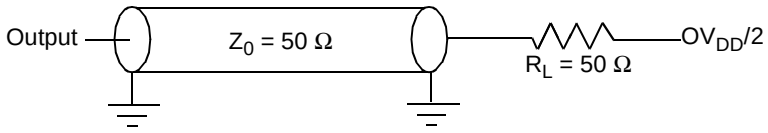
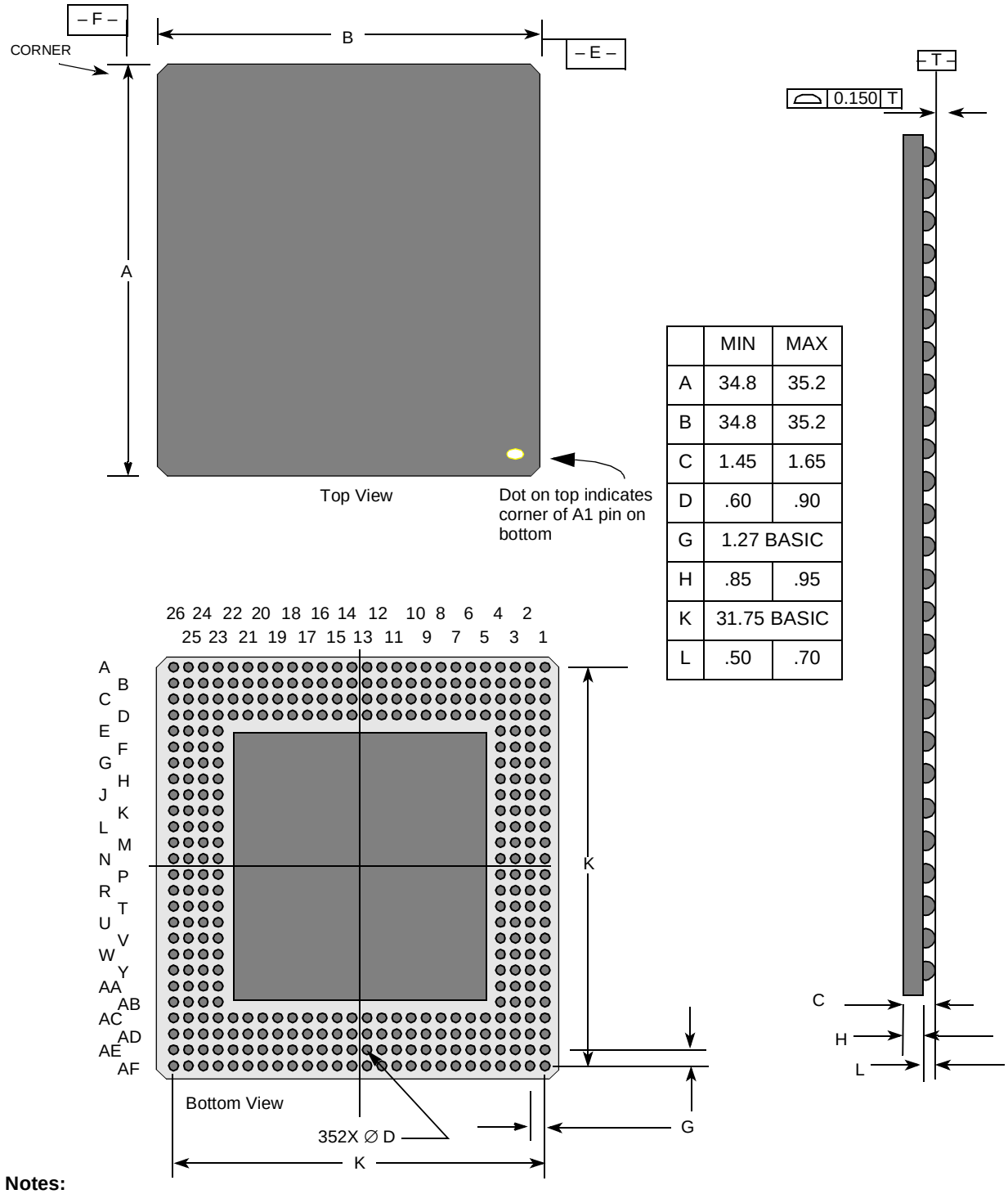



**Figure 16. I²C AC Test Load**

## 5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8245, 352 TBGA package.




| | MIN | MAX |
|---|---|---|
| A | 34.8 | 35.2 |
| B | 34.8 | 35.2 |
| C | 1.45 | 1.65 |
| D | .60 | .90 |
| G | 1.27 BASIC | |
| H | .85 | .95 |
| K | 31.75 BASIC | |
| L | .50 | .70 |

**Notes:**
1. Drawing not to scale.
2. All measurements are in millimeters (mm).

**Figure 24. MPC8245 Package Dimensions and Pinout Assignments**

**Table 16. MPC8245 Pinout Listing (continued)**

| Name | Pin Numbers | Type | Power Supply | Output Driver Type | Notes |
|---|---|---|---|---|---|
| **DUART Control Signals** | | | | | |
| SOUT1/PCI_CLK0 | AC25 | Output | $GV_{DD}$ | DRV_MEM_CTRL | 13, 14 |
| SIN1/PCI_CLK1 | AB25 | I/O | $GV_{DD}$ | DRV_MEM_CTRL | 13, 14, 26 |
| SOUT2/$\overline{\text{RTS1}}$/ PCI_CLK2 | AE26 | Output | $GV_{DD}$ | DRV_MEM_CTRL | 13, 14 |
| SIN2/$\overline{\text{CTS1}}$/ PCI_CLK3 | AF25 | I | $GV_{DD}$ | DRV_MEM_CTRL | 13, 14, 26 |
| **Clock-Out Signals** | | | | | |
| PCI_CLK0/SOUT1 | AC25 | Output | $GV_{DD}$ | DRV_PCI_CLK | 13, 14 |
| PCI_CLK1/SIN1 | AB25 | Output | $GV_{DD}$ | DRV_PCI_CLK | 13, 14, 26 |
| PCI_CLK2/$\overline{\text{RTS1}}$/ SOUT2 | AE26 | Output | $GV_{DD}$ | DRV_PCI_CLK | 13, 14 |
| PCI_CLK3/$\overline{\text{CTS1}}$/ SIN2 | AF25 | Output | $GV_{DD}$ | DRV_PCI_CLK | 13, 14, 26 |
| PCI_CLK4/DA3 | AF26 | Output | $GV_{DD}$ | DRV_PCI_CLK | 13, 14 |
| PCI_SYNC_OUT | AD25 | Output | $GV_{DD}$ | DRV_PCI_CLK | |
| PCI_SYNC_IN | AB23 | Input | $GV_{DD}$ | — | |
| SDRAM_CLK [0:3] | D1 G1 G2 E1 | Output | $GV_{DD}$ | DRV_MEM_CTRL or DRV_MEM_CLK | 6, 21 |
| SDRAM_SYNC_OUT | C1 | Output | $GV_{DD}$ | DRV_MEM_CTRL or DRV_MEM_CLK | 21 |
| SDRAM_SYNC_IN | H3 | Input | $GV_{DD}$ | — | |
| CKO/DA1 | B15 | Output | $OV_{DD}$ | DRV_STD_MEM | 14 |
| OSC_IN | AD21 | Input | $OV_{DD}$ | — | 19 |
| **Miscellaneous Signals** | | | | | |
| $\overline{\text{HRST\_CTRL}}$ | A20 | Input | $OV_{DD}$ | — | 27 |
| $\overline{\text{HRST\_CPU}}$ | A19 | Input | $OV_{DD}$ | — | 27 |
| $\overline{\text{MCP}}$ | A17 | Output | $OV_{DD}$ | DRV_STD_MEM | 3, 4, 17 |
| NMI | D16 | Input | $OV_{DD}$ | — | |
| $\overline{\text{SMI}}$ | A18 | Input | $OV_{DD}$ | — | 10 |
| $\overline{\text{SRESET}}$/SDMA12 | B16 | I/O | $GV_{DD}$ | DRV_MEM_CTRL | 10, 14 |
| TBEN/SDMA13 | B14 | I/O | $GV_{DD}$ | DRV_MEM_CTRL | 10, 14 |

**Table 16. MPC8245 Pinout Listing (continued)**

| Name | Pin Numbers | Type | Power Supply | Output Driver Type | Notes |
|---|---|---|---|---|---|
| $\overline{\text{QACK}}$/DA0 | F2 | Output | $OV_{DD}$ | DRV_STD_MEM | 4, 14, 25 |
| $\overline{\text{CHKSTOP\_IN}}$/ SDMA14 | D14 | I/O | $GV_{DD}$ | DRV_MEM_CTRL | 10, 14 |
| TRIG_IN/$\overline{\text{RCS2}}$ | AF20 | I/O | $OV_{DD}$ | — | 10, 14 |
| TRIG_OUT/$\overline{\text{RCS3}}$ | AC18 | Output | $GV_{DD}$ | DRV_MEM_CTRL | 14 |
| MAA[0:2] | AF2 AF1 AE1 | Output | $GV_{DD}$ | DRV_STD_MEM | 3, 4, 6 |
| $\overline{\text{MIV}}$ | A16 | Output | $OV_{DD}$ | — | 24 |
| PMAA[0:1] | AD18 AF18 | Output | $OV_{DD}$ | DRV_STD_MEM | 3, 4, 6, 15 |
| PMAA[2] | AE19 | Output | $OV_{DD}$ | DRV_STD_MEM | 4, 6, 15 |
| **Test/Configuration Signals** | | | | | |
| PLL_CFG[0:4]/ DA[10:6] | A22 B19 A21 B18 B17 | I/O | $OV_{DD}$ | DRV_STD_MEM | 6, 14, 20 |
| $\overline{\text{TEST0}}$ | AD22 | Input | $OV_{DD}$ | — | 1, 9 |
| RTC | Y2 | Input | $GV_{DD}$ | — | 11 |
| TCK | AF22 | Input | $OV_{DD}$ | — | 9, 12 |
| TDI | AF23 | Input | $OV_{DD}$ | — | 9, 12 |
| TDO | AC21 | Output | $OV_{DD}$ | — | 24 |
| TMS | AE22 | Input | $OV_{DD}$ | — | 9, 12 |
| $\overline{\text{TRST}}$ | AE23 | Input | $OV_{DD}$ | — | 9, 12 |
| **Power and Ground Signals** | | | | | |
| GND | AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3 | Ground | — | — | |
| $LV_{DD}$ | AC20 AC23 D20 D23 G23 P23 Y23 | Reference voltage 3.3 V, 5.0 V | $LV_{DD}$ | — | |
| $GV_{DD}$ | AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3 | Power for memory drivers 3.3 V | $GV_{DD}$ | — | |
| $OV_{DD}$ | AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24 | PCI/Stnd 3.3 V | $OV_{DD}$ | — | |

**Table 16. MPC8245 Pinout Listing (continued)**

| Name | Pin Numbers | Type | Power Supply | Output Driver Type | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4 | Power for core 1.8/2.0 V | $V_{DD}$ | — | 22 |
| No Connect | D17 | — | — | — | 23 |
| $AV_{DD}$ | C17 | Power for PLL (CPU core logic) 1.8/2.0 V | $AV_{DD}$ | — | 22 |
| $AV_{DD}2$ | AF24 | Power for PLL (peripheral logic) 1.8/2.0 V | $AV_{DD}2$ | — | 22 |
| **Debug/Manufacturing Pins** | | | | | |
| DA0/$\overline{\text{QACK}}$ | F2 | Output | $OV_{DD}$ | DRV_STD_MEM | 4, 10, 25 |
| DA1/CKO | B15 | Output | $OV_{DD}$ | DRV_STD_MEM | 14 |
| DA2 | C25 | Output | $OV_{DD}$ | DRV_PCI | 2 |
| DA3/PCI_CLK4 | AF26 | Output | $GV_{DD}$ | DRV_PCI_CLK | 14 |
| DA4/$\overline{\text{REQ4}}$ | Y26 | I/O | $OV_{DD}$ | — | 12, 14 |
| DA5/$\overline{\text{GNT4}}$ | W26 | Output | $OV_{DD}$ | DRV_PCI | 7, 15, 14 |
| DA[10:6]/ PLL_CFG[0:4] | A22 B19 A21 B18 B17 | I/O | $OV_{DD}$ | DRV_STD_MEM | 6, 14, 20 |
| DA[11] | AD26 | Output | $OV_{DD}$ | DRV_PCI | 2 |
| DA[12:13] | AF17 AF19 | Output | $OV_{DD}$ | DRV_STD_MEM | 2, 6 |

# 6 PLL Configurations

The internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

**Table 17. PLL Configurations (266- and 300-MHz Parts)**

| Ref. No. | PLL_CFG [0:4] [10,13] | 266-MHz Part [9] | | | 300-MHz Part [9] | | | Multipliers | |
|---|---|---|---|---|---|---|---|---|---|
| | | PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz) | Periph Logic/ MemBus Clock Range (MHz) | CPU Clock Range (MHz) | PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz) | Periph Logic/ MemBus Clock Range (MHz) | CPU Clock Range (MHz) | PCI-to-Mem (Mem VCO) | Mem-to-CPU (CPU VCO) |
| 0 | 00000[12] | 25–35[5] | 75–105 | 188–263 | 25–40[5,7] | 75–120 | 188–300 | 3 (2) | 2.5 (2) |
| 1 | 00001[12] | 25–29[5] | 75–88 | 225–264 | 25–33[5] | 75–99 | 225–297 | 3 (2) | 3 (2) |
| 2 | 00010[11] | 50[18]–59[5,7] | 50–59 | 225–266 | 50[18]–66[1] | 50–66 | 225–297 | 1 (4) | 4.5 (2) |
| 3 | 00011[11,14] | 50[17]–66[1] | 50–66 | 100–133 | 50[17]–66[1] | 50–66 | 100–133 | 1 (Bypass) | 2 (4) |
| 4 | 00100[12] | 25–46[4] | 50–92 | 100–184 | 25–46[4] | 50–92 | 100–184 | 2 (4) | 2 (4) |
| 6 | 00110[15] | Bypass | | | Bypass | | | Bypass | |
| 7 Rev B | 00111[14] | 60[6]–66[1] | 60–66 | 180–198 | 60[6]–66[1] | 60–66 | 180–198 | 1 (Bypass) | 3 (2) |
| 7 Rev D | 00111[14] | Not available | | | | | | | |
| 8 | 01000[12] | 60[6]–66[1] | 60–66 | 180–198 | 60[6]–66[1] | 60–66 | 180–198 | 1 (4) | 3 (2) |
| 9 | 01001[12] | 45[6]–66[1] | 90–132 | 180–264 | 45[6]–66[1] | 90–132 | 180–264 | 2 (2) | 2 (2) |
| A | 01010[12] | 25–29[5] | 50–58 | 225–261 | 25–33[5] | 50–66 | 225–297 | 2 (4) | 4.5 (2) |
| B | 01011[12] | 45[3]–59[5] | 68–88 | 204–264 | 45[3]–66[1] | 68–99 | 204–297 | 1.5 (2) | 3 (2) |
| C | 01100[12] | 36[6]–46[4] | 72–92 | 180–230 | 36[6]–46[4] | 72–92 | 180–230 | 2 (4) | 2.5 (2) |
| D | 01101[12] | 45[3]–50[5] | 68–75 | 238–263 | 45[3]–57[5] | 68–85 | 238–298 | 1.5 (2) | 3.5 (2) |
| E | 01110[12] | 30[6]–44[5] | 60–88 | 180–264 | 30[6]–46[4] | 60–92 | 180–276 | 2 (4) | 3 (2) |
| F | 01111[12] | 25[5] | 75 | 263 | 25–28[5] | 75–85 | 263–298 | 3 (2) | 3.5 (2) |
| 10 | 10000[12] | 30[6]–44[2,5] | 90–132 | 180–264 | 30[6]–44[2] | 90–132 | 180–264 | 3 (2) | 2 (2) |
| 11 | 10001[12] | 25–26[5,7] | 100–106 | 250–266 | 25–29[2] | 100–116 | 250–290 | 4 (2) | 2.5 (2) |
| 12 | 10010[12] | 60[6]–66[1] | 90–99 | 180–198 | 60[6]–66[1] | 90–99 | 180–198 | 1.5 (2) | 2 (2) |

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic 0 level is read into the configuration bits during reset if the default logic 1 level is not desired.

Any other unused active low input pins should be tied to a logic-one level through weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND through weak pull-down resistors (2–10 kΩ).

## 7.5 PCI Reference Voltage—$LV_{DD}$

The MPC8245 PCI reference voltage ($LV_{DD}$) pins should be connected to a 3.3 ± 0.3 V power supply if interfacing the MPC8245 into a 3.3-V PCI bus system. Similarly, the $LV_{DD}$ pins should be connected to a 5.0 V ± 5% power supply if interfacing the MPC8245 into a 5-V PCI bus system. For either reference voltage, the MPC8245 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8245 tolerates 5-V signals when interfaced into a 5-V PCI bus system.

## 7.6 MPC8245 Compatibility with MPC8240

The MPC8245 AC timing specifications are backward-compatible with those of the MPC8240, except for the requirements of item 11 in Table 10. Timing adjustments are needed as specified for $T_{os}$ (SDRAM_SYNC_IN to *sys_logic_clk* offset) time requirements.

The MPC8245 does not support the SDRAM flow-through memory interface.

The nominal core $V_{DD}$ power supply changes from 2.5 V on the MPC8240 to 1.8/2.0 V on the MPC8245. See Table 2.

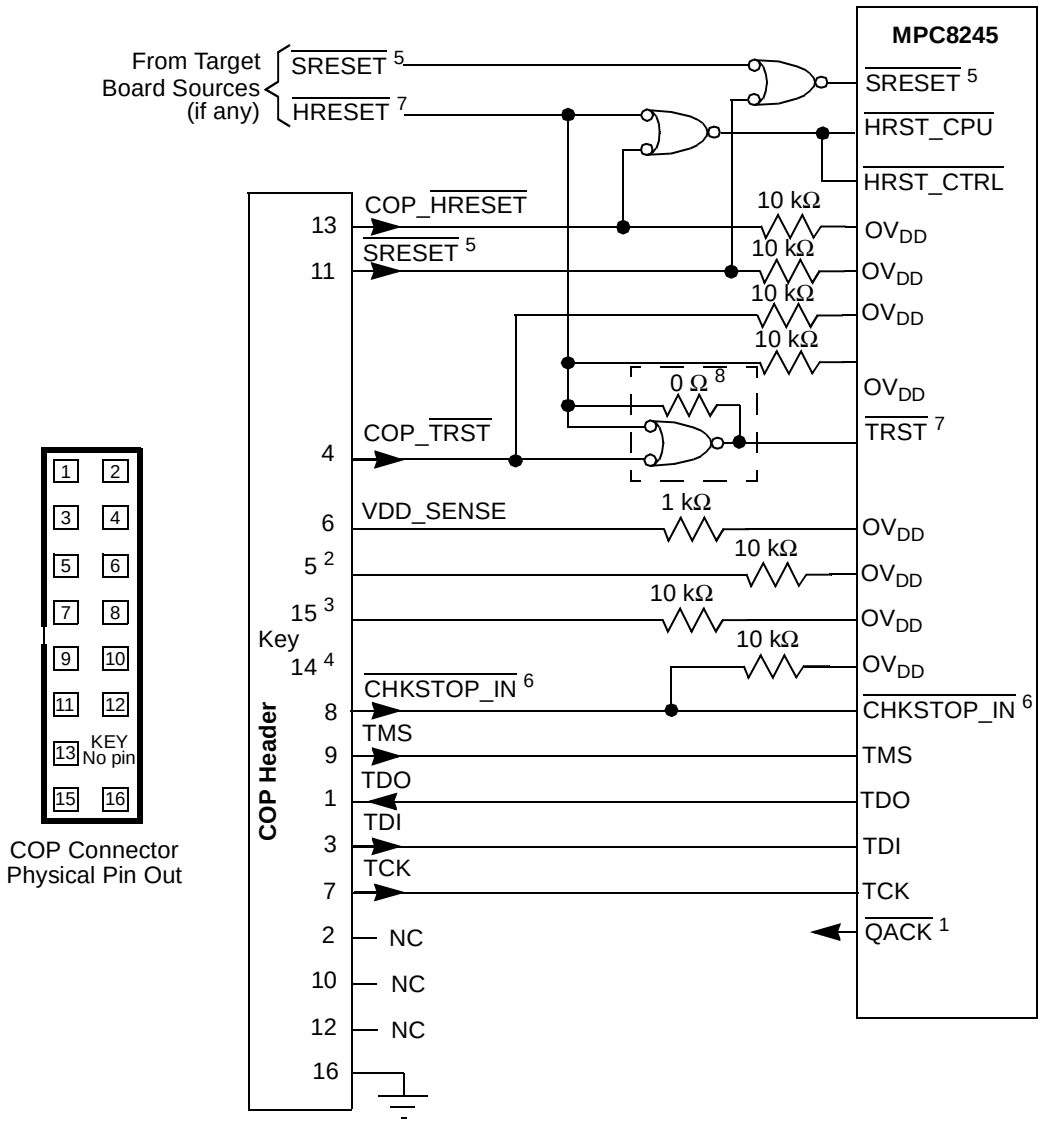
For example, the MPC8245 PLL_CFG[0:4] setting 0x02 (0b00010) has a different PCI-to-Mem and Mem-to-CPU multiplier ratio than the same setting on the MPC8240, so it is not backward-compatible. See Table 17.

Most of the MPC8240 PLL_CFG[0:4] settings are subsets of the PCI_SYNC_IN input frequency range accepted by the MPC8245. However, the parts are not fully backward-compatible since the ranges of the two parts do not always match. Modes 0x8 and 0x18 of the MPC8245 are not compatible with settings 0x8 and 0x18 on the MPC8240. See Table 17 and Table 18.

Two reset configuration signals on the MPC8245 are not used as reset configuration signals on the MPC8240: SDMA0 and SDMA1.

The SDMA0 reset configuration pin selects between the MPC8245 DUART and the MPC8240 backward-compatible mode PCI_CLK[0:4] functionality on these multiplexed signals. The default state (logic 1) of SDMA0 selects the MPC8240 backward-compatible mode of PCI_CLK[0:4] functionality while a logic 0 state on the SDMA0 signal selects DUART functionality. In DUART mode, four of the five PCI clocks, PCI_CLK[0:3], are not available.

The SDMA1 reset configuration pin selects between MPC8245 extended ROM functionality and MPC8240 backward-compatible functionality on the multiplexed signals: TBEN, $\overline{\text{CHKSTOP\_IN}}$,




**Note:**

1. $\overline{\text{QACK}}$ is an output and is not required at the COP header for emulation.
2. RUN/$\overline{\text{STOP}}$ normally found on pin 5 of the COP header is not implemented on the MPC8245. Connect pin 5 of the COP header to $OV_{DD}$ with a 1-kΩ pull-up resistor.
3. $\overline{\text{CKSTP\_OUT}}$ normally on pin 15 of the COP header is not implemented on the MPC8245. Connect pin 15 of the COP header to $OV_{DD}$ with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. $\overline{\text{SRESET}}$ functions as output SDMA12 in extended ROM mode.
6. $\overline{\text{CHKSTOP\_IN}}$ functions as output SDMA14 in extended ROM mode.
7. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to control the processor as shown.
8. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header through an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.

**Figure 26. COP Connector Diagram**

# 8 Document Revision History

Table 19 provides a revision history for this hardware specification.

**Table 19. Revision History Table**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 10 | 8/07 | Section 3, Table 3, and Table 7—Changed format of recommended voltage supply values so that delta to the chosen nominal does not exceed ± 100 mV.<br>Completely replaced Section 4.6 with compliant $I^2C$ specifications as with other related integrated processor devices. |
| 9 | 12/27/05 | Document—Added Power Architecture information.<br>Section 4.1—Changed increased absolute maximum range for $V_{DD}$ in Table 1. Updated format of nominal voltage listings in Table 2.<br>Section 9.2—Removed Note 3 from Table 21.<br>Updated back page information. |
| 8 | 11/15/2005 | Document—Imported new template and made minor editorial changes.<br>Removed references to a 466 MHz part since it is not available for new orders.<br>Section 4.3.2—Added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3.<br>Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2.<br>Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated the section to reflect what we offer for new orders.<br>Section 9.3—Added new section, “Part Marking.” Updated Figure 33 to match with current part marking format. |
| 7 | 10/07/2004 | Section 4.1.2—Table 2: Corrected range of $AV_{DD}$ and $AVDD_2$.<br>Section 9.1—Table 21: Corrected voltage range under Process Descriptor column. Minor reformatting. |
| 6.1 | 05/24/2004 | Section 4.5.3—Table 11: Spec 12b was improved from 4.5 ns to 4.0 ns. This improvement is guaranteed on devices marked after work week (WW) 28 of 2004. A device's work week may be determined from the “YYWW” portion of the devices trace ability code which is marked on the top of the device. So for WW28 in 2004, the device’s YYWW is marked as 0428. For more information refer to Figure 33 |
| 6 | 05/11/2004 | Section 4.1.2—Table 2: Corrected range of $GV_{DD}$ to 3.3 ± 5%.<br>Section 4.2.1—Table 4: Changed the default for drive strength of DRV_STD_MEM.<br>Section 4.5.1—Table 8: Changed the wording description for item 15.<br>Section 4.5.2—Table 10: Changed $T_{os}$ range and wording in note; Figure 11:changed wording for SDRAM_SYNC_IN description relative to $T_{OS}$.<br>Section 4.5.3—Table 11: Changed timing specification for *sys_logic_clk* to output valid (memory control, address, and data signals). |
| 5.1 | — | Section 4.3.1—Table 9: Corrected last row to state the correct description for the bit setting. Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay” |

**Table 19. Revision History Table (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 5 | — | Section 4.1.2 — Added note 6 and related label for latching of the PLL_CFG signals.<br>Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN.<br>Section 4.3 — Table 7, updated specifications for the voltage range of $V_{DD}$ for specific CPU frequencies.<br>Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs.<br>Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2.<br>Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2.<br>Section 5.3 — Table 17: Removed extra listing of DRDY in Test/Configuration signal list and updated relevant notes for signal in Memory Interface signal listing. Updated note #20. Added note 26 for the signals of the UART interface.<br>Section 7.6 — Added reference to AN2128 application note that highlights the differences between the MPC8240 and the MPC8245.<br>Section 7.7 — Added relevant notes to this section and updated Figure 29. |
| 4 | — | Section 1.4.1.2—Updated notes for $GV_{DD}$, $AV_{DD}$, $AV_{DD2}$.<br>Section 1.5.1—Updated solder ball information to include lead-free (V V) balls.<br>Section 1.5.3—Updated Note 25 for $\overline{\text{QACK}}$/DA0 signal. Added a sentence to Note 3.<br>Section 1.6 —Incorporated Note 19 into Note 12 and modified Tables 18 and 19 accordingly.<br>Section 1.9—Updated part marking nomenclature where appropriate to include the lead-free offering.<br>Replaced reference to PNS document MPC8245RZUPNS with MPC8245ARZUPNS. |
| 3 | — | Section 1.4.1.2—Figure 2: Updated Note 2 and removed ‘voltage regulator delay’ label since Section 1.7.2 is being deleted this revision. Added Figures 4 and 5 to show voltage overshoot and undershoot of the PCI interface on the MPC8245.<br>Section 1.4.1.3—Table 3: Updated the maximum input capacitance from 7 to 16 pF based on characterization data.<br>Section 1.4.3.1—Updated PCI_SYNC_IN jitter specifications to 200 ps.<br>Section 1.4.3.3—Table 11, item 12b: added the word ‘address’ to help clarify which signals the spec applies to. Figure 15: edited timing for items 12a0 and 12a2 to correspond with Table 11.<br>Section 1.5.3—Updated notes for the $\overline{\text{QACK}}$/DA0 signal because this signal has been found to have no internal pull resistor.<br>Section 1.6—Corrected note numbers for reference numbers 3,10,1B, and 1C of the PLL tables. Updated PLL specifications for modes 7 and 1E.<br>Section 1.7.2—Removed this section since the information already exists in Section 1.4.1.5.<br>Section 1.7.4—Added the words ‘the clamping voltage’ to describe $LV_{DD}$ in the sixth paragraph. Changed the $\overline{\text{QACK}}$/DA0 signal from the list of signals having an internal pull-up resistor to the list of signals needing a weak pull-up resistor to $OV_{DD}$.<br>Section 1.9.1—Tables 21 thru 23: Added processor version register value. |

**Table 19. Revision History Table (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 2 | — | Globally changed EPIC to PIC.<br>Section 1.4.1.4—Note 5: Changed register reference from 0x72 to 0x73.<br>Section 1.4.1.5—Table 5: Updated power dissipation numbers based on latest characterization data.<br>Section 1.4.2—Table 6: Updated table to show more thermal specifications.<br>Section 1.4.3—Table 7: Updated minimum memory bus value to 50 MHz.<br>Section 1.4.3.1—Changed equations for DLL locking range based on characterization data. Added updates and reference to AN2164 for note 6. Added table defining Tdp parameters. Labeled N value in Figures 5 through 8.<br>Section 1.4.3.2—Table 10: Changed bit definitions for tap points. Updated note on Tos and added reference to AN2164 for note 7. Updated Figure 9 to show significance of Tos.<br>Section 1.4.3.4—Added column for SDRAM_CLK @ 133 MHz<br>Sections 1.5.1 and 1.5.2—Corrected packaging information to state TBGA packaging.<br>Section 1.5.3—Corrected some signals in Table 16 which were missing overbars in the Rev 1.0 release of the document.<br>Section 1.6—Updated Note 10 of Tables 18 and 19.<br>Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors.<br>Section 1.9—Updated format of tables in Ordering Information section. |
| 1 | — | Updated document template.<br>Section 1.4.1.4—Changed the driver type names in Table 6 to match with the names used in the MPC8245 Reference Manual.<br>Section 1.5.3—Updated driver type names for signals in Table 16 to match with names used in the MPC8245 Integrated Processor Reference Manual.<br>Section 1.4.1.2—Updated Table 7 to refer to new PLL Tables for VCO limits.<br>Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid timing.<br>Section 1.5.1—Updated solder balls information to 62Sn/36PB/2Ag.<br>Section 1.6—Updated PLL Tables 17 and 18 and appropriate notes to reflect changes of VCO ranges for memory and CPU frequencies.<br>Section 1.7—Updated voltage sequencing requirements in Table 2 and removed Section 1.7.2.<br>Section 1.7.8—Updated TRST information and Figure 26.<br>New Section 1.7.2—Updated the range of I/O power consumption numbers for $OV_{DD}$ and $GV_{DD}$ to correct values as in Table 5. Updated fastest frequency combination to 66:100:350 MHz.<br>Section 1.7.9—Updated list for heat sink and thermal interface vendors.<br>Section 1.9—Changed format of Ordering Information section. Added tables to reflect part number specifications also available.<br>Added Sections 1.9.2 and 1.9.3. |
| 0.5 | — | Corrected labels for Figures 5 through 8. |

**Table 19. Revision History Table (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 0.1 | — | Made $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V ± 100 mV information for 133-MHz memory interface operation to Section 1.3, Table 2, Table 5, Table 9, Table 17, and Section 1.7.2.<br>Pin D17, formerly $LAV_{DD}$ (supply voltage for DLL), is a NC on the MPC8245 since the DLL voltage is supplied internally. Eliminated all references to $LAV_{DD}$; updated Section 1.7.1.<br>Previous Note 4 of Table 2 did not apply to the MPC8245 (MPC8240 document legacy). New Note 4 added in reference to maximum CPU speed at reduced $V_{DD}$ voltage.<br>Updated the Programmable Output Impedance of DEV_MEM_ADDR in Table 4 to 6 Ω to reflect characterization data.<br>Updated Table 5 to reflect reduced power consumption when operating $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V ± 100 mV. Changed Notes 2, 3, and 4 to reflect $V_{DD}$ at 1.9 V. Changed Note 5 to represent $V_{DD} = AV_{DD}$ = 1.8 V.<br>Updated Table 7 to reflect $V_{DD}/AV_{DD}/AV_{DD}2$ voltage level operating frequency dependencies; changed 250 MHz device column to 266 MHz; modified Note 1 eliminating VCO references; added Note 2. Changed 250 MHz processor frequency offering to 266 MHz.<br>Changed Spec 12b for memory output valid time in Table 11 from 5.5 ns to 4.5 ns; this is a key specification change to enable 133-MHz memory interface designs.<br>Updated Pinout Table 16 with the following changes:<br>• Pin types for $\overline{\text{RCS0}}$, $\overline{\text{RCS3}}$/TRIG_OUT and DA[11:15] were erroneously listed as I/O, changed Pin Types to Output.<br>• Pin types for $\overline{\text{REQ}}$4/DA4, $\overline{\text{RCS2}}$/TRIG_IN, and PLL_CFG[0:4]/DA[10:6] were erroneously listed as Input, changed Pin Types to I/O.<br>• Changed Pin D17 from $LAV_{DD}$ to No Connect; deleted Note 21 and references.<br>• Notes 3, 5, and 7 contained references to the MPC8240 (MPC8240 document legacy); changed these references to MPC8245.<br>• Previous Notes 13 and 14 did not apply to the MPC8245 (MPC8240 document legacy), these notes were deleted; moved Note 19 to become new Note 13; moved Note 20 to become new Note 14; updated associated references.<br>• Added Note 3 to SDMA[1:0] signals about internal pull-up resistors during reset state.<br>• Reversed vector ordering for the PCI Interface Signals: $\overline{\text{C/BE}}$[0:3] changed to $\overline{\text{C/BE}}$[3:0], AD[0:31] changed to AD[31:0], $\overline{\text{GNT}}$[0:3] changed to $\overline{\text{GNT}}$[3:0], and $\overline{\text{REQ}}$[0:3] changed to $\overline{\text{REQ}}$[3:0]. The package pin number orderings were also reversed meaning that pin functionality did NOT change. For example, AD0 is still on signal C22, AD1 is still on signal D22,..., AD31 is still on signal V25. This change was made to make the vectored PCI signals in this hardware specification consistent with the *PCI Local Bus Specification* and the *MPC8245 Integrated Processor Reference Manual* vector ordering.<br>• Changed $\overline{\text{TEST1}}/\overline{\text{DRDY}}$ signal on pin B20 to $\overline{\text{DRDY}}$.<br>• Changed $\overline{\text{TEST2}}$ signal on pin Y2 to RTC for performance monitor use.<br>Updated PLL Table 17 with the following changes for 133-MHz memory interface operation:<br>• Added Ref. 9 (01001) and Ref. 17 (10111) details; removed these settings from Note 10 (reserved settings list).<br>• Enhanced range of Ref. 10 (10000).<br>• Updated Note 13, changed bits 16–20 erroneous information to correct bits 23–19.<br>• Added Notes 16 and 17.<br>Added information to Section 1.7.8 in reference to $\overline{\text{CHKSTOP\_IN}}$ and $\overline{\text{SRESET}}$ being unavailable in extended ROM mode. |
| 0.0 | — | Initial release. |

# 9 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 9.1, “Part Numbers Fully Addressed by This Document.” Section 9.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

## 9.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC8245. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number. The revision level can be determined by reading the Revision ID register at address offset 0x08.

**Table 20. Part Numbering Nomenclature**

| MPC | *nnnn* | L | *xx* | *nnn* | *x* |
|---|---|---|---|---|---|

| Product Code | Part Identifier | Process Descriptor | Package [1] | Processor Frequency [2] (MHz) | Revision Level | Processor Version Register Value |
|---|---|---|---|---|---|---|
| MPC | 8245 | L: 0° to 105°C | ZU = TBGA<br>V V = Lead-free TBGA | 266, 300<br>1.7 V to 2.1 V | D:1.4 Rev ID:0x14 | 0x80811014 |
| | | L: 0° to 105°C | ZU = TBGA<br>V V = Lead-free TBGA | 333, 350<br>1.9 V to 2.2 V | | |

**Notes:**

1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.