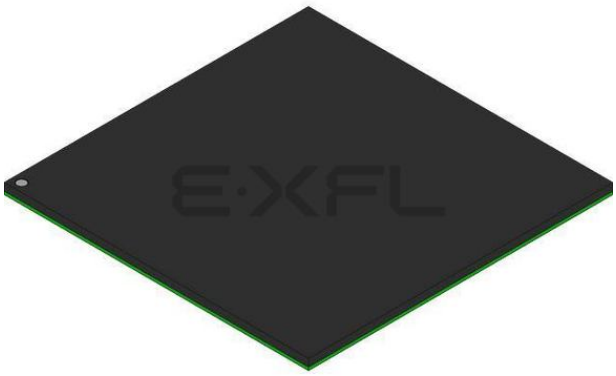

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The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, a 16-Kbyte instruction cache, a 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade off performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8245 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8245 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8245 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—Entire cache or on a per-way basis up to three of four ways
  - Dynamic power management: 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing supporting SDRAM
    - One to eight banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

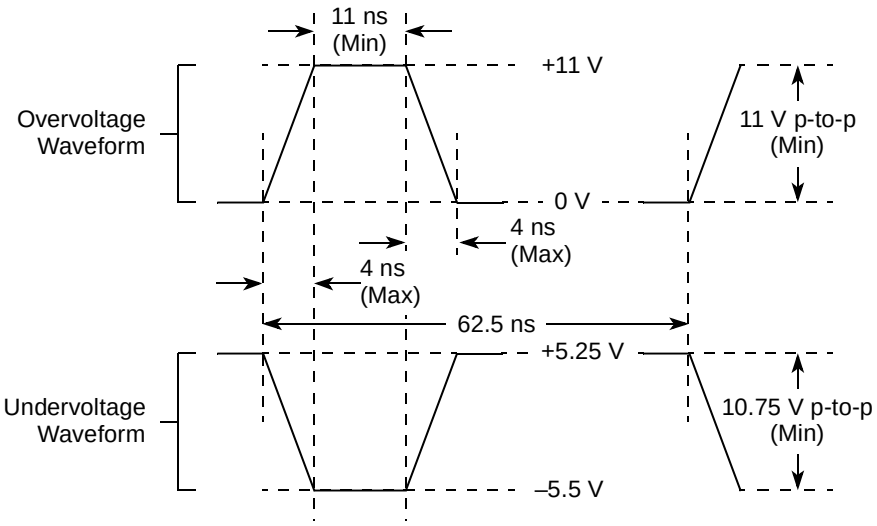

Figure 5. Maximum AC Waveforms for 5-V Signaling

4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8245 at recommended operating conditions.

Table 3. DC Electrical Specifications

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only, except PCI_SYNC_IN	V_{IH}	$0.65 \times OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only, except PCI_SYNC_IN	V_{IL}	—	$0.3 \times OV_{DD}$	V	
Input high voltage	All other pins, including PCI_SYNC_IN (GV_{DD} = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs, including PCI_SYNC_IN	V_{IL}	GND	0.8	V	
Input leakage current for pins using DRV_PCI driver	$0.5\ V \le V_{in} \le 2.7\ V$ @ LV_{DD} = 4.75 V	I_L	—	±70	μA	4
Input leakage current for all others	LV_{DD} = 3.6 V $GV_{DD} \le 3.465$ V	I_L	—	±10	μA	4
Output high voltage	I_{OH} = driver-dependent (GV_{DD} = 3.3 V)	V_{OH}	2.4	—	V	2
Output low voltage	I_{OL} = driver-dependent (GV_{DD} = 3.3 V)	V_{OL}	—	0.4	V	2

4.3 Power Characteristics

Table 5 provides power consumption data for the MPC8245.

Table 5. Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock/CPU Clock Frequency (MHz)							Unit	Notes
	66/66/266	66/133/266	66/66/300	66/100/300	33/83/333	66/133/333	66/100/350		
Typical	1.7 (1.5)	2.0 (1.8)	1.8 (1.7)	2.0 (1.8)	2.0	2.3	2.2	W	1, 5
Max—FP	2.2 (1.9)	2.4 (2.1)	2.3 (2.0)	2.5 (2.2)	2.6	2.8	2.8	W	1, 2
Max—INT	1.8 (1.6)	2.1 (1.8)	2.0 (1.8)	2.1 (1.8)	2.2	2.4	2.4	W	1, 3
Doze	1.1 (1.0)	1.4 (1.3)	1.2 (1.1)	1.4 (1.3)	1.4	1.6	1.5	W	1, 4, 6
Nap	0.4 (0.4)	0.7 (0.7)	0.4 (0.4)	0.6 (0.6)	0.5	0.7	0.6	W	1, 4, 6
Sleep	0.2 (0.2)	0.4 (0.4)	0.2 (0.4)	0.3 (0.3)	0.3	0.4	0.3	W	1, 4, 6

I/O Power Supplies [10]				
Mode	**Min**	**Max**	**Unit**	**Notes**
Typ—OV_{DD}	134 (121)	334 (301)	mW	7, 8
Typ—GV_{DD}	324 (292)	800 (720)	mW	7, 9

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power. Information on OV_{DD} and GV_{DD} supply power is captured in the I/O power supplies section of this table. Values shown in parenthesis ( ) indicate power consumption at $V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 V.
2. Maximum—FP power is measured at V_{DD} = 2.1 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 2.1 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 2.1 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at $V_{DD} = AV_{DD}$ = 2.0 V, OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. The typical minimum I/O power values were results of the MPC8245 performing cache resident integer operations at the slowest frequency combination of 33:66:200 (PCI:Mem:CPU) MHz.
8. The typical maximum OV_{DD} value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory.
9. The typical maximum GV_{DD} value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.
10. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW. Guaranteed by design and not tested.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for details on MPC8245 memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

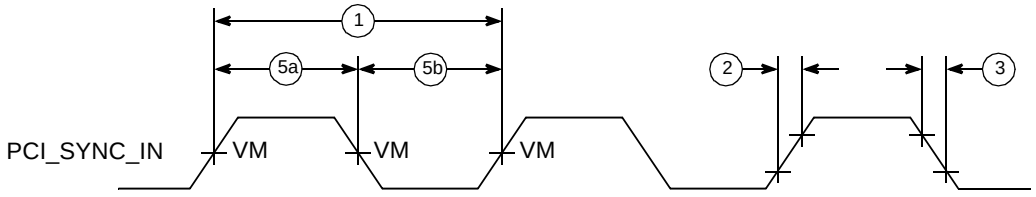

Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The gray areas show where the DLL locks.

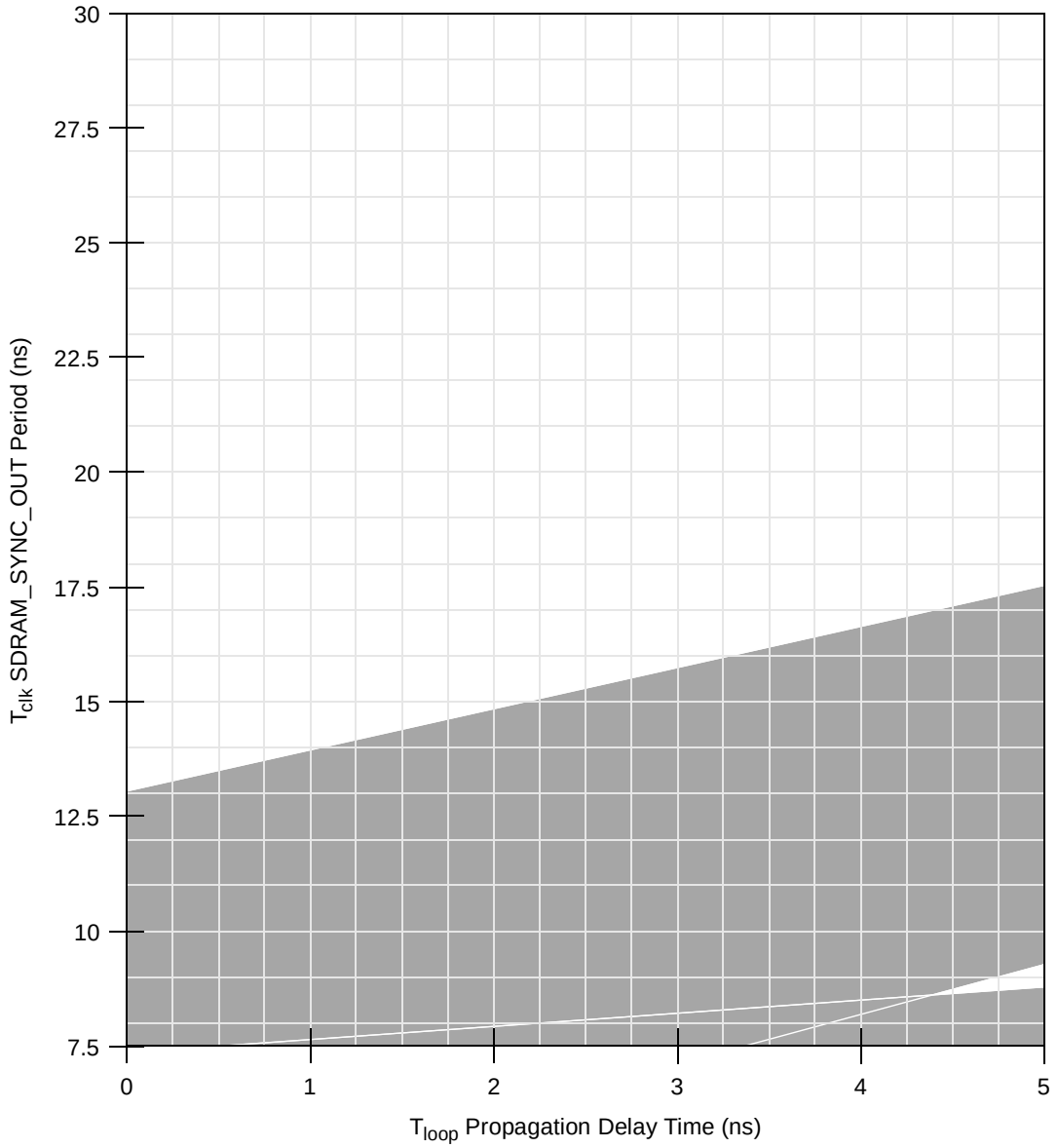

Figure 7. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=0 and Normal Tap Delay

Table 10. Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to *sys_logic_clk* (input setup)				
10b0	Tap 0, register offset <0x77>, bits 5–4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5–4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5–4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5–4 = 0b11	0.5	—		
10c	PIC, misc. debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^2C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5–4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5–4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5–4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5–4 = 0b11	2.1	—		
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to Inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5–4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. To maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*, the feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range. The feedback trace length is relative to the SDRAM clock output trace lengths. We recommend that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the problem of T_{os}, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.

Figure 17 shows the AC timing diagram for the I^2C bus.

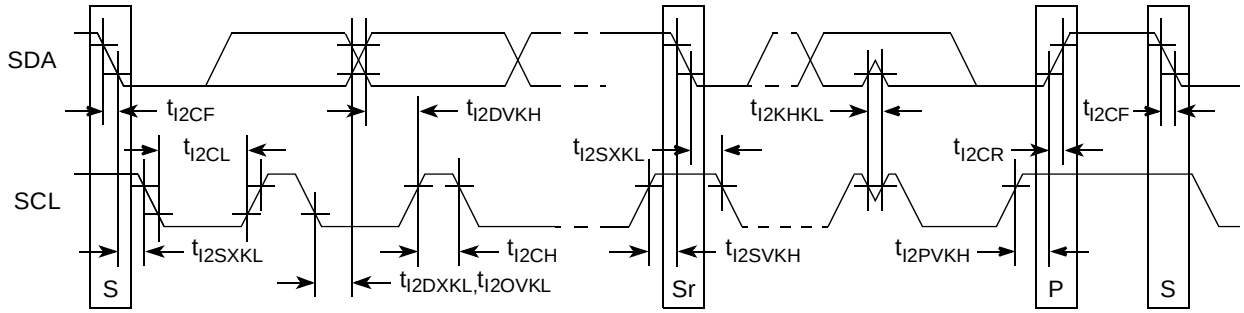

Figure 17. I^2C Bus AC Timing Diagram

4.7 PIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the PIC serial interrupt mode AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with GV_{DD} = 3.3 V ± 5% and LV_{DD} = 3.3 V ± 0.3 V.

Table 14. PIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	—
3	S_CLK output valid time	—	6	ns	—
4	Output hold time	0	—	ns	—
5	$\overline{\text{S\_FRAME}}$, S_RST output valid time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT input setup time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:

1. See the *MPC8245 Integrated Processor Reference Manual* for a description of the PIC interrupt control register (ICR) and S_CLK frequency programming.
2. S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 18 and Figure 19, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. The *MPC8245 Integrated Processor Reference Manual* describes the functional relationships between these signals.
3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor Reference Manual* for a complete clocking description.

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN) (continued)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams.

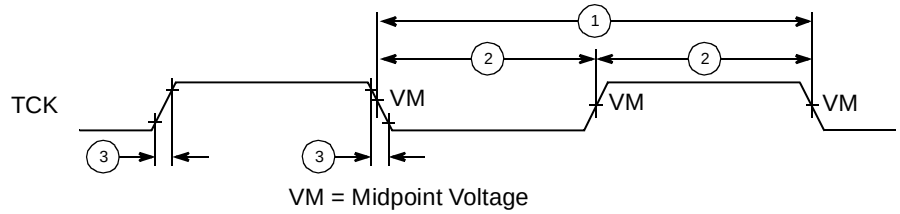

Figure 20. JTAG Clock Input Timing Diagram

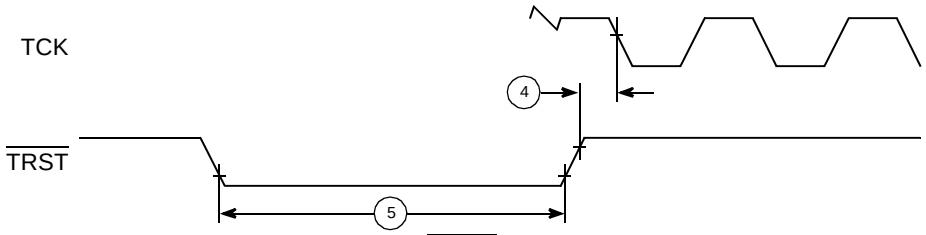

Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

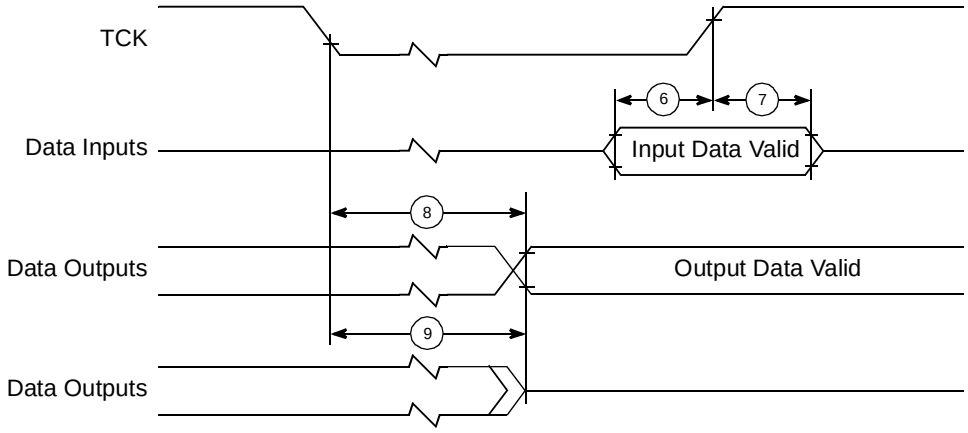

Figure 22. JTAG Boundary Scan Timing Diagram

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DQM[0:7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{CS}$[0:7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{FOE}$	H1	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS0}$	N4	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS1}$	N2	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{RCS2}$/TRIG_IN	AF20	I/O	OV_{DD}	6 ohms	10, 14
$\overline{RCS3}$/TRIG_OUT	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
SDMA[1:0]	W1 W2	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4, 6
SDMA[11:2]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{DRDY}$	B20	Input	OV_{DD}	—	9, 10
SDMA12/$\overline{SRESET}$	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA13/TBEN	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA14/ $\overline{CHKSTOP\_IN}$	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDBA1	P1	Output	GV_{DD}	DRV_MEM_CTRL	
SDBA0	P2	Output	GV_{DD}	DRV_MEM_CTRL	
PAR[0:7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GV_{DD}	DRV_STD_MEM	6
$\overline{SDRAS}$	AD1	Output	GV_{DD}	DRV_MEM_CTRL	3
$\overline{SDCAS}$	AD2	Output	GV_{DD}	DRV_MEM_CTRL	3
CKE	H2	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{WE}$	AA1	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{AS}$	Y1	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
PIC Control Signals					
IRQ0/S_INT	C19	Input	OV_{DD}	—	
IRQ1/S_CLK	B21	I/O	OV_{DD}	DRV_PCI	
IRQ2/S_RST	AC22	I/O	OV_{DD}	DRV_PCI	
IRQ3/$\overline{S\_FRAME}$	AE24	I/O	OV_{DD}	DRV_PCI	
IRQ4/$\overline{L\_INT}$	A23	I/O	OV_{DD}	DRV_PCI	
I^2C Control Signals					
SDA	AE20	I/O	OV_{DD}	DRV_STD_MEM	10, 16
SCL	AF21	I/O	OV_{DD}	DRV_STD_MEM	10, 16

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DUART Control Signals					
SOUT1/PCI_CLK0	AC25	Output	GV_{DD}	DRV_MEM_CTRL	13, 14
SIN1/PCI_CLK1	AB25	I/O	GV_{DD}	DRV_MEM_CTRL	13, 14, 26
SOUT2/$\overline{\text{RTS1}}$/ PCI_CLK2	AE26	Output	GV_{DD}	DRV_MEM_CTRL	13, 14
SIN2/$\overline{\text{CTS1}}$/ PCI_CLK3	AF25	I	GV_{DD}	DRV_MEM_CTRL	13, 14, 26
Clock-Out Signals					
PCI_CLK0/SOUT1	AC25	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_CLK1/SIN1	AB25	Output	GV_{DD}	DRV_PCI_CLK	13, 14, 26
PCI_CLK2/$\overline{\text{RTS1}}$/ SOUT2	AE26	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_CLK3/$\overline{\text{CTS1}}$/ SIN2	AF25	Output	GV_{DD}	DRV_PCI_CLK	13, 14, 26
PCI_CLK4/DA3	AF26	Output	GV_{DD}	DRV_PCI_CLK	13, 14
PCI_SYNC_OUT	AD25	Output	GV_{DD}	DRV_PCI_CLK	
PCI_SYNC_IN	AB23	Input	GV_{DD}	—	
SDRAM_CLK [0:3]	D1 G1 G2 E1	Output	GV_{DD}	DRV_MEM_CTRL or DRV_MEM_CLK	6, 21
SDRAM_SYNC_OUT	C1	Output	GV_{DD}	DRV_MEM_CTRL or DRV_MEM_CLK	21
SDRAM_SYNC_IN	H3	Input	GV_{DD}	—	
CKO/DA1	B15	Output	OV_{DD}	DRV_STD_MEM	14
OSC_IN	AD21	Input	OV_{DD}	—	19
Miscellaneous Signals					
$\overline{\text{HRST\_CTRL}}$	A20	Input	OV_{DD}	—	27
$\overline{\text{HRST\_CPU}}$	A19	Input	OV_{DD}	—	27
$\overline{\text{MCP}}$	A17	Output	OV_{DD}	DRV_STD_MEM	3, 4, 17
NMI	D16	Input	OV_{DD}	—	
$\overline{\text{SMI}}$	A18	Input	OV_{DD}	—	10
$\overline{\text{SRESET}}$/SDMA12	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TBEN/SDMA13	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
$\overline{\text{QACK}}$/DA0	F2	Output	OV_{DD}	DRV_STD_MEM	4, 14, 25
$\overline{\text{CHKSTOP\_IN}}$/ SDMA14	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TRIG_IN/$\overline{\text{RCS2}}$	AF20	I/O	OV_{DD}	—	10, 14
TRIG_OUT/$\overline{\text{RCS3}}$	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
MAA[0:2]	AF2 AF1 AE1	Output	GV_{DD}	DRV_STD_MEM	3, 4, 6
$\overline{\text{MIV}}$	A16	Output	OV_{DD}	—	24
PMAA[0:1]	AD18 AF18	Output	OV_{DD}	DRV_STD_MEM	3, 4, 6, 15
PMAA[2]	AE19	Output	OV_{DD}	DRV_STD_MEM	4, 6, 15
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
$\overline{\text{TEST0}}$	AD22	Input	OV_{DD}	—	1, 9
RTC	Y2	Input	GV_{DD}	—	11
TCK	AF22	Input	OV_{DD}	—	9, 12
TDI	AF23	Input	OV_{DD}	—	9, 12
TDO	AC21	Output	OV_{DD}	—	24
TMS	AE22	Input	OV_{DD}	—	9, 12
$\overline{\text{TRST}}$	AE23	Input	OV_{DD}	—	9, 12
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground	—	—	
LV_{DD}	AC20 AC23 D20 D23 G23 P23 Y23	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	
GV_{DD}	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for memory drivers 3.3 V	GV_{DD}	—	
OV_{DD}	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3 V	OV_{DD}	—	

6 PLL Configurations

The internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (266- and 300-MHz Parts)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–35[5]	75–105	188–263	25–40[5,7]	75–120	188–300	3 (2)	2.5 (2)
1	00001[12]	25–29[5]	75–88	225–264	25–33[5]	75–99	225–297	3 (2)	3 (2)
2	00010[11]	50[18]–59[5,7]	50–59	225–266	50[18]–66[1]	50–66	225–297	1 (4)	4.5 (2)
3	00011[11,14]	50[17]–66[1]	50–66	100–133	50[17]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100[12]	25–46[4]	50–92	100–184	25–46[4]	50–92	100–184	2 (4)	2 (4)
6	00110[15]	Bypass			Bypass			Bypass	
7 Rev B	00111[14]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (Bypass)	3 (2)
7 Rev D	00111[14]	Not available							
8	01000[12]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (4)	3 (2)
9	01001[12]	45[6]–66[1]	90–132	180–264	45[6]–66[1]	90–132	180–264	2 (2)	2 (2)
A	01010[12]	25–29[5]	50–58	225–261	25–33[5]	50–66	225–297	2 (4)	4.5 (2)
B	01011[12]	45[3]–59[5]	68–88	204–264	45[3]–66[1]	68–99	204–297	1.5 (2)	3 (2)
C	01100[12]	36[6]–46[4]	72–92	180–230	36[6]–46[4]	72–92	180–230	2 (4)	2.5 (2)
D	01101[12]	45[3]–50[5]	68–75	238–263	45[3]–57[5]	68–85	238–298	1.5 (2)	3.5 (2)
E	01110[12]	30[6]–44[5]	60–88	180–264	30[6]–46[4]	60–92	180–276	2 (4)	3 (2)
F	01111[12]	25[5]	75	263	25–28[5]	75–85	263–298	3 (2)	3.5 (2)
10	10000[12]	30[6]–44[2,5]	90–132	180–264	30[6]–44[2]	90–132	180–264	3 (2)	2 (2)
11	10001[12]	25–26[5,7]	100–106	250–266	25–29[2]	100–116	250–290	4 (2)	2.5 (2)
12	10010[12]	60[6]–66[1]	90–99	180–198	60[6]–66[1]	90–99	180–198	1.5 (2)	2 (2)

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Not usable			Off	Off

Notes:

1. Limited by the maximum PCI input frequency (66 MHz).
2 Limited by the maximum system memory interface operating frequency (100 MHz @ 300 MHz CPU).
3. Limited by the minimum memory VCO frequency (133 MHz).
4. Limited due to the maximum memory VCO frequency (372 MHz).
5. Limited by the maximum CPU operating frequency.
6. Limited by the minimum CPU VCO frequency (360 MHz).
7. Limited by the maximum CPU VCO frequency (maximum marked CPU speed X 2).
8. In clock-off mode, no clocking occurs inside the MPC8245, regardless of the PCI_SYNC_IN input.
9. Range values are rounded down to the nearest whole number (decimal place accuracy removed).
10. PLL_CFG[0:4] settings not listed are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting differ from the MPC8240 and are not backward-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting differs from or does not exist on the MPC8240 and may not be fully backward-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
16. Limited by the maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).
17. Limited by the minimum CPU operating frequency (100 MHz).
18. Limited by the minimum memory bus frequency (50 MHz).

Table 18. PLL Configurations (333- and 350-MHz Parts)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–44[16]	75–132	188–330	25–44[16]	75–132	188–330	3 (2)	2.5 (2)
1	00001[12]	25–37[5,7]	75–111	225–333	25–38[5]	75–114	225–342	3 (2)	3 (2)

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

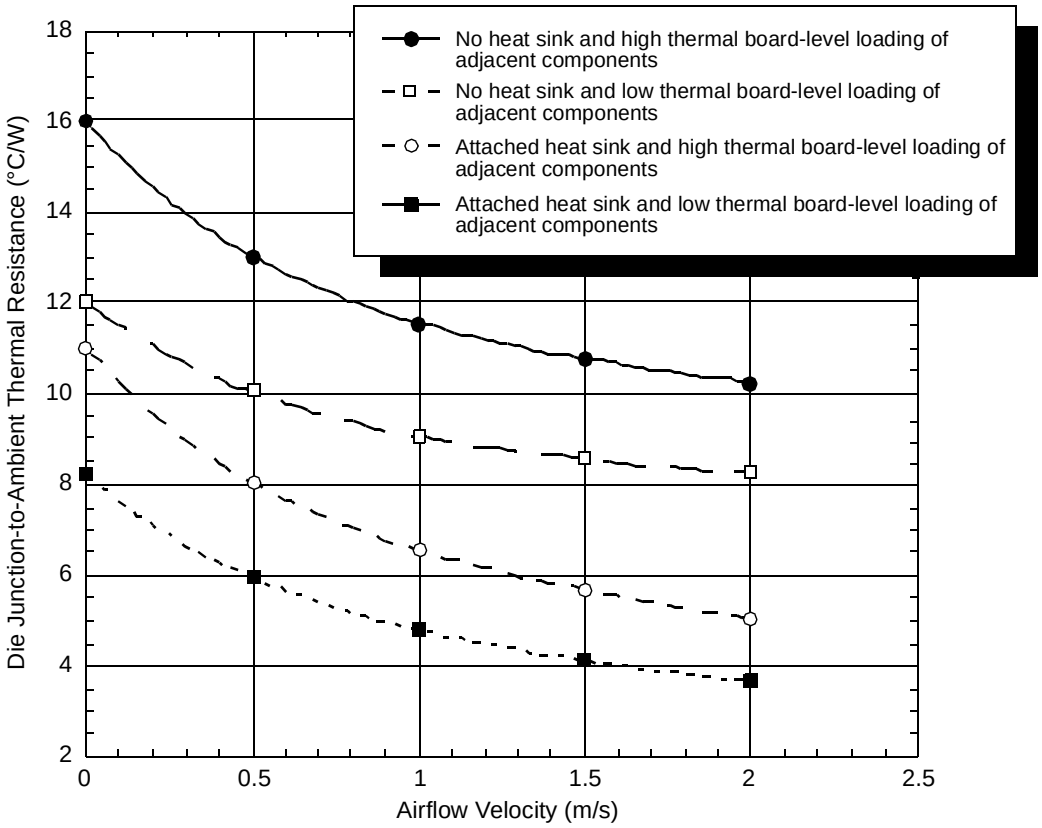

Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances and may or may not need airflow.

7.8.1 Internal Package Conduction Resistance

The intrinsic conduction thermal resistance paths for the TBGA cavity-down packaging technology shown in Figure 29 are as follows:

- Die junction-to-case thermal resistance
- Die junction-to-ball thermal resistance

Figure 29 depicts the primary heat transfer path for a package with an attached heat sink mounted on a printed-circuit board.

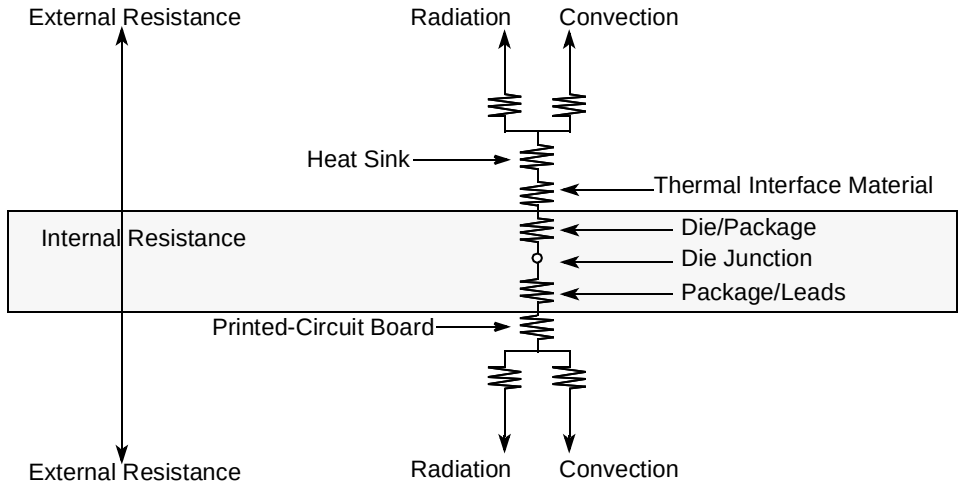

Figure 29. TBGA Package with Heat Sink Mounted to a Printed-Circuit Board

In a TBGA package, the active side of the die faces the printed-circuit board. Most of the heat travels through the die, across the die attach layer, and into the copper spreader. Some of the heat is removed from the top surface of the spreader through convection and radiation. Another percentage of the heat enters the printed-circuit board through the solder balls. The heat is then removed from the exposed surfaces of the board through convection and radiation. If a heat sink is used, a larger percentage of heat leaves through the top side of the spreader.

7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material placed between the top of the package and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 30 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 30). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

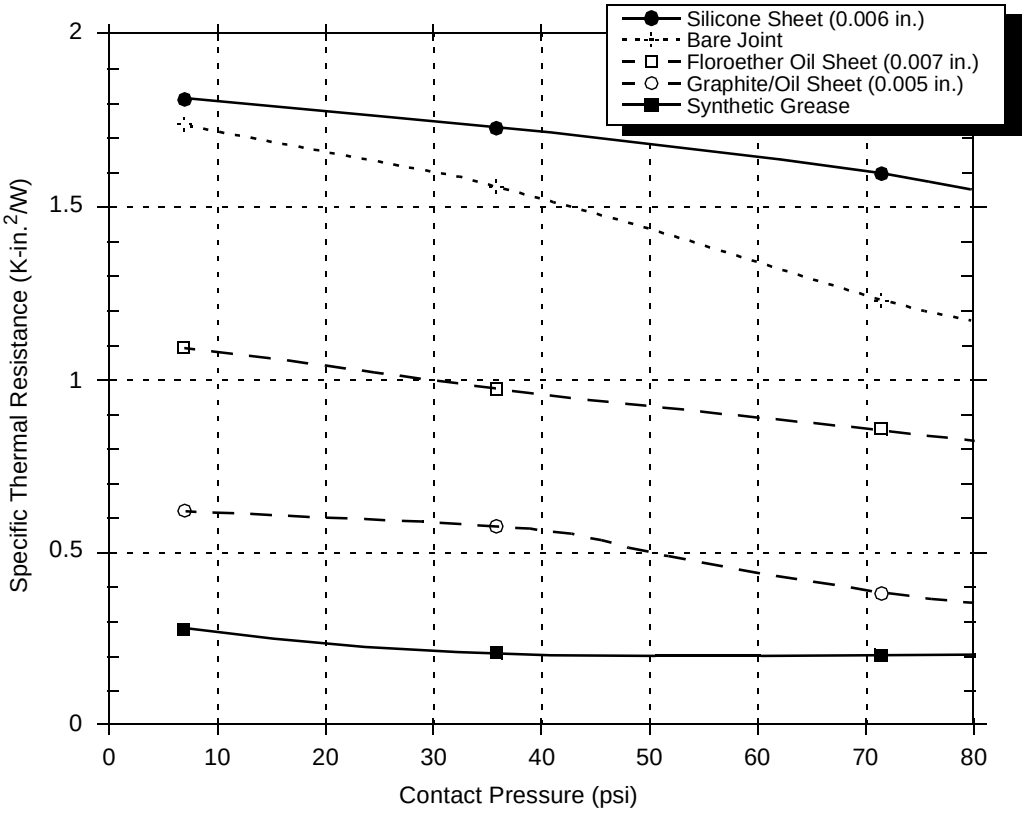

Figure 30. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application without a heat sink, the thermal characterization parameter (Ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.9 References

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
2	—	Globally changed EPIC to PIC. Section 1.4.1.4—Note 5: Changed register reference from 0x72 to 0x73. Section 1.4.1.5—Table 5: Updated power dissipation numbers based on latest characterization data. Section 1.4.2—Table 6: Updated table to show more thermal specifications. Section 1.4.3—Table 7: Updated minimum memory bus value to 50 MHz. Section 1.4.3.1—Changed equations for DLL locking range based on characterization data. Added updates and reference to AN2164 for note 6. Added table defining Tdp parameters. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Table 10: Changed bit definitions for tap points. Updated note on Tos and added reference to AN2164 for note 7. Updated Figure 9 to show significance of Tos. Section 1.4.3.4—Added column for SDRAM_CLK @ 133 MHz Sections 1.5.1 and 1.5.2—Corrected packaging information to state TBGA packaging. Section 1.5.3—Corrected some signals in Table 16 which were missing overbars in the Rev 1.0 release of the document. Section 1.6—Updated Note 10 of Tables 18 and 19. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.9—Updated format of tables in Ordering Information section.
1	—	Updated document template. Section 1.4.1.4—Changed the driver type names in Table 6 to match with the names used in the MPC8245 Reference Manual. Section 1.5.3—Updated driver type names for signals in Table 16 to match with names used in the MPC8245 Integrated Processor Reference Manual. Section 1.4.1.2—Updated Table 7 to refer to new PLL Tables for VCO limits. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid timing. Section 1.5.1—Updated solder balls information to 62Sn/36PB/2Ag. Section 1.6—Updated PLL Tables 17 and 18 and appropriate notes to reflect changes of VCO ranges for memory and CPU frequencies. Section 1.7—Updated voltage sequencing requirements in Table 2 and removed Section 1.7.2. Section 1.7.8—Updated TRST information and Figure 26. New Section 1.7.2—Updated the range of I/O power consumption numbers for OV_{DD} and GV_{DD} to correct values as in Table 5. Updated fastest frequency combination to 66:100:350 MHz. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of Ordering Information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.
0.5	—	Corrected labels for Figures 5 through 8.

9.3 Part Marking

Parts are marked as the example shown in Figure 31.

Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is test traceability code.
YWWLAZ is the assembly traceability code.
CCCCC is the country code.

Figure 31. Part Marking for TBGA Device