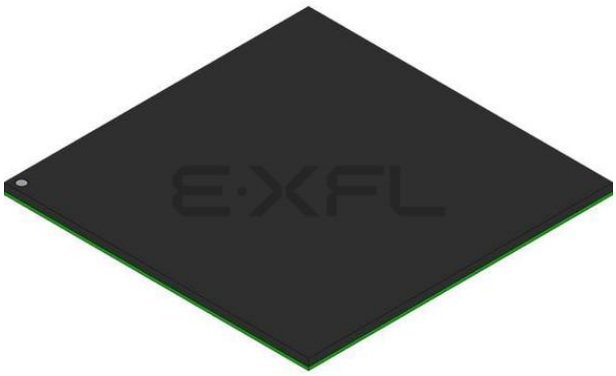


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8245lzu350d

4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC8245 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.25	V
Supply voltage—memory bus drivers	GV_{DD}	–0.3 to 3.6	V
Supply voltage—PCI and standard I/O buffers	OV_{DD}	–0.3 to 3.6	V
Supply voltage—PLLs	AV_{DD}/AV_{DD} 2	–0.3 to 2.25	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105[3]	°C
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.
3. Note that this temperature range does not apply to the 400 MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8245. Some voltage values do not apply to the 400-MHz parts. For details, refer to the hardware specifications addendum MPC8245ECSO2AD.

Table 2. Recommended Operating Conditions[1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply voltage	V_{DD}	1.8/1.9/2.0 V ± 100 mV	V	4, 7
		2.0/2.1 V ± 100 mV	V	5, 7
I/O buffer supply for PCI and standard	OV_{DD}	3.3 ± 0.3	V	7
Supply voltages for memory bus drivers	GV_{DD}	3.3 ± 5%	V	9
CPU PLL supply voltage	AV_{DD}	1.8/1.9/2.0 V ±	V	4, 7, 12
		2.0/2.1 V ±	V	5, 7, 12

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8245. For details, see Section 7.8, "Thermal Management."

Table 6. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection (Single-layer board—1s)	$R_{\theta JA}$	16.1	°C/W	1, 2
Junction-to-ambient natural convection (Four-layer board—2s2p)	$R_{\theta JMA}$	12.0	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Single-layer board—1s)	$R_{\theta JMA}$	11.6	°C/W	1, 3
Junction-to-ambient (@200 ft/min) (Four layer board—2s2p)	$R_{\theta JMA}$	9.0	°C/W	1, 3
Junction-to-board	$R_{\theta JB}$	4.8	°C/W	4
Junction-to-case	$R_{\theta JC}$	1.8	°C/W	5
Junction-to-package top (natural convection)	Ψ_{JT}	1.0	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate used for case temperature.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 9, "Ordering Information," for details on ordering parts.

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*, for details on MPC8245 memory clock design.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

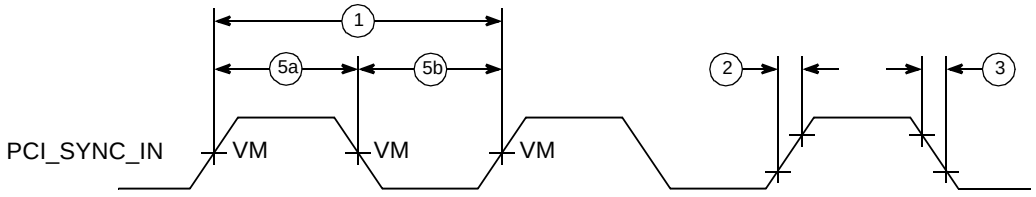


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Figure 7 through Figure 10 show the DLL locking range loop delay vs. frequency of operation. These graphs define the areas of DLL locking for various modes. The gray areas show where the DLL locks.

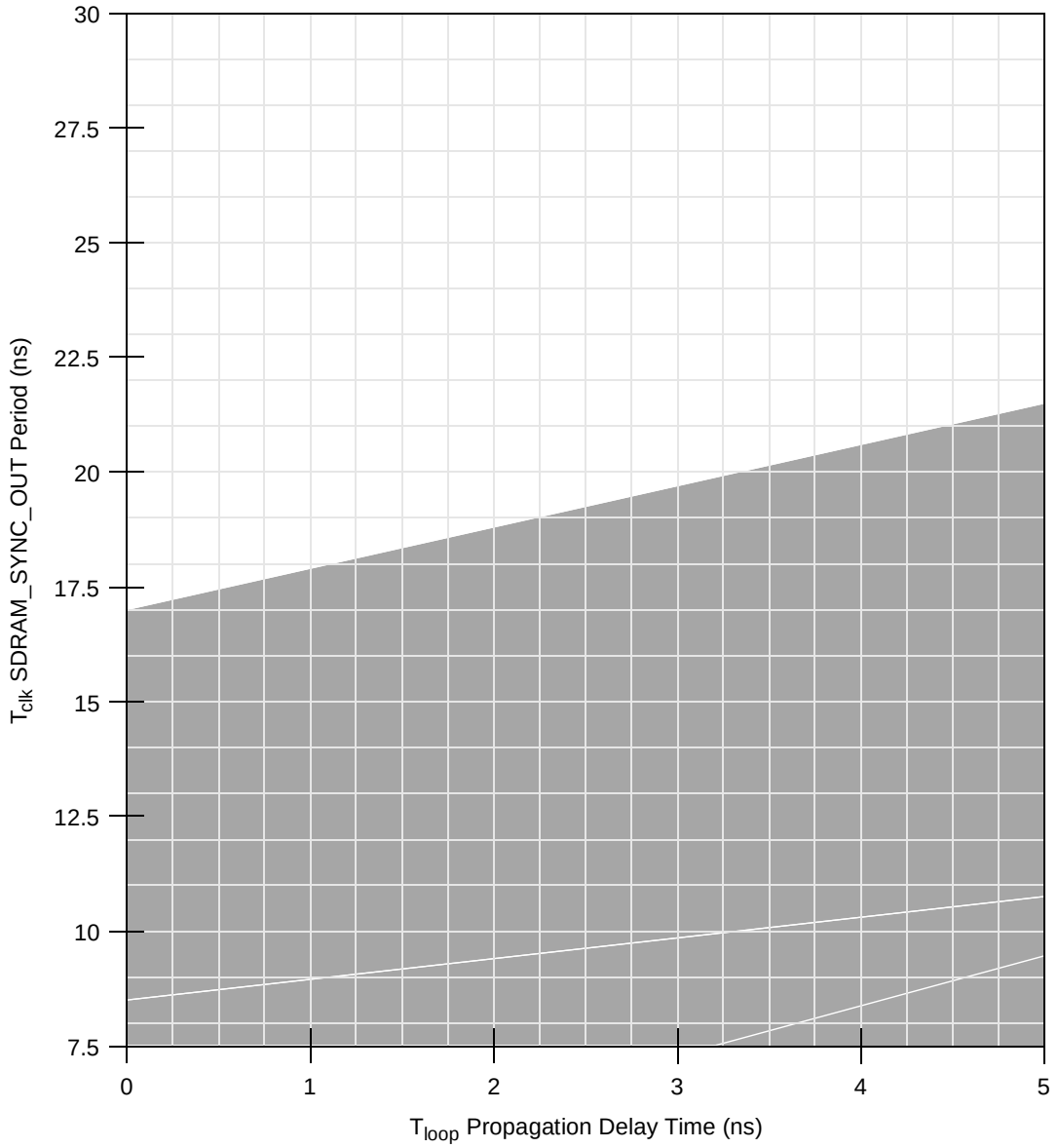


Figure 9. DLL Locking Range Loop Delay Versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay

Table 10. Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to *sys_logic_clk* (input setup)				
10b0	Tap 0, register offset <0x77>, bits 5–4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5–4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5–4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5–4 = 0b11	0.5	—		
10c	PIC, misc. debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^2C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5–4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5–4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5–4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5–4 = 0b11	2.1	—		
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to Inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5–4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. To maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*, the feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range. The feedback trace length is relative to the SDRAM clock output trace lengths. We recommend that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the problem of T_{os}, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.

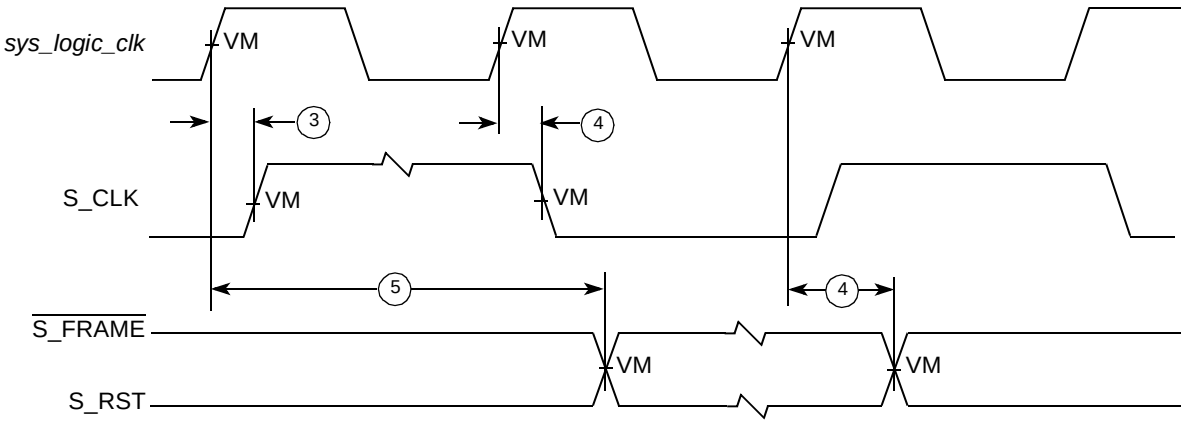


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

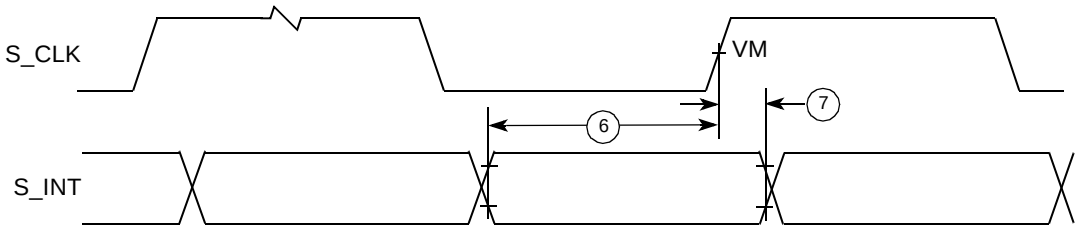


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.8 IEEE 1149.1 (JTAG) AC Timing Specifications

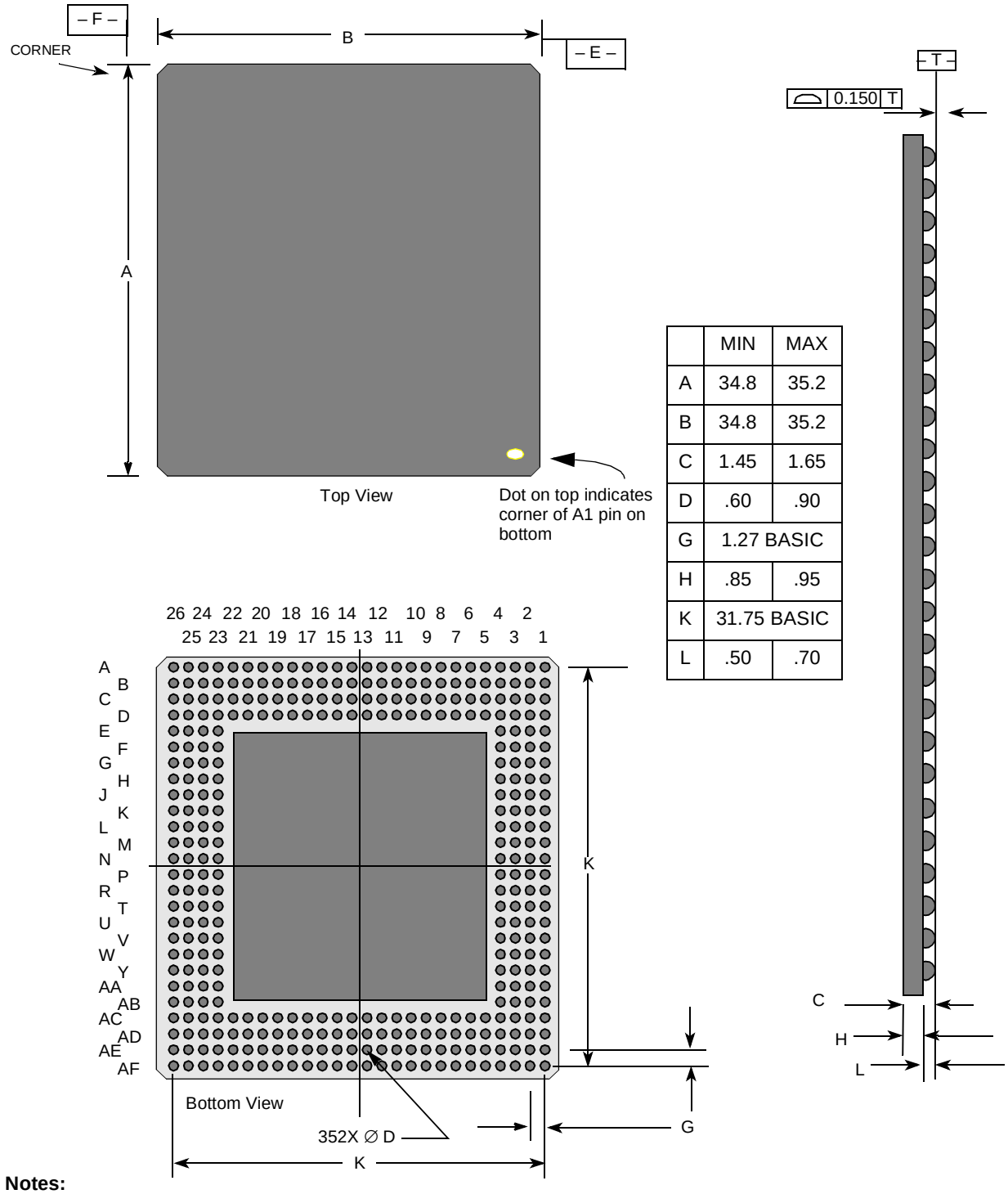
Table 15 provides the JTAG AC timing specifications for the MPC8245 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.5 V	20	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	

5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8245, 352 TBGA package.



	MIN	MAX
A	34.8	35.2
B	34.8	35.2
C	1.45	1.65
D	.60	.90
G	1.27 BASIC	
H	.85	.95
K	31.75 BASIC	
L	.50	.70

Notes:
1. Drawing not to scale.
2. All measurements are in millimeters (mm).

Figure 24. MPC8245 Package Dimensions and Pinout Assignments

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
DQM[0:7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{CS}$[0:7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{FOE}$	H1	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS0}$	N4	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{RCS1}$	N2	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{RCS2}$/TRIG_IN	AF20	I/O	OV_{DD}	6 ohms	10, 14
$\overline{RCS3}$/TRIG_OUT	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
SDMA[1:0]	W1 W2	I/O	GV_{DD}	DRV_MEM_CTRL	3, 4, 6
SDMA[11:2]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3	Output	GV_{DD}	DRV_MEM_CTRL	6
$\overline{DRDY}$	B20	Input	OV_{DD}	—	9, 10
SDMA12/$\overline{SRESET}$	B16	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA13/TBEN	B14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDMA14/ $\overline{CHKSTOP\_IN}$	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
SDBA1	P1	Output	GV_{DD}	DRV_MEM_CTRL	
SDBA0	P2	Output	GV_{DD}	DRV_MEM_CTRL	
PAR[0:7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GV_{DD}	DRV_STD_MEM	6
$\overline{SDRAS}$	AD1	Output	GV_{DD}	DRV_MEM_CTRL	3
$\overline{SDCAS}$	AD2	Output	GV_{DD}	DRV_MEM_CTRL	3
CKE	H2	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
$\overline{WE}$	AA1	Output	GV_{DD}	DRV_MEM_CTRL	
$\overline{AS}$	Y1	Output	GV_{DD}	DRV_MEM_CTRL	3, 4
PIC Control Signals					
IRQ0/S_INT	C19	Input	OV_{DD}	—	
IRQ1/S_CLK	B21	I/O	OV_{DD}	DRV_PCI	
IRQ2/S_RST	AC22	I/O	OV_{DD}	DRV_PCI	
IRQ3/$\overline{S\_FRAME}$	AE24	I/O	OV_{DD}	DRV_PCI	
IRQ4/$\overline{L\_INT}$	A23	I/O	OV_{DD}	DRV_PCI	
I^2C Control Signals					
SDA	AE20	I/O	OV_{DD}	DRV_STD_MEM	10, 16
SCL	AF21	I/O	OV_{DD}	DRV_STD_MEM	10, 16

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Numbers	Type	Power Supply	Output Driver Type	Notes
$\overline{\text{QACK}}$/DA0	F2	Output	OV_{DD}	DRV_STD_MEM	4, 14, 25
$\overline{\text{CHKSTOP\_IN}}$/ SDMA14	D14	I/O	GV_{DD}	DRV_MEM_CTRL	10, 14
TRIG_IN/$\overline{\text{RCS2}}$	AF20	I/O	OV_{DD}	—	10, 14
TRIG_OUT/$\overline{\text{RCS3}}$	AC18	Output	GV_{DD}	DRV_MEM_CTRL	14
MAA[0:2]	AF2 AF1 AE1	Output	GV_{DD}	DRV_STD_MEM	3, 4, 6
$\overline{\text{MIV}}$	A16	Output	OV_{DD}	—	24
PMAA[0:1]	AD18 AF18	Output	OV_{DD}	DRV_STD_MEM	3, 4, 6, 15
PMAA[2]	AE19	Output	OV_{DD}	DRV_STD_MEM	4, 6, 15
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	A22 B19 A21 B18 B17	I/O	OV_{DD}	DRV_STD_MEM	6, 14, 20
$\overline{\text{TEST0}}$	AD22	Input	OV_{DD}	—	1, 9
RTC	Y2	Input	GV_{DD}	—	11
TCK	AF22	Input	OV_{DD}	—	9, 12
TDI	AF23	Input	OV_{DD}	—	9, 12
TDO	AC21	Output	OV_{DD}	—	24
TMS	AE22	Input	OV_{DD}	—	9, 12
$\overline{\text{TRST}}$	AE23	Input	OV_{DD}	—	9, 12
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground	—	—	
LV_{DD}	AC20 AC23 D20 D23 G23 P23 Y23	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	
GV_{DD}	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for memory drivers 3.3 V	GV_{DD}	—	
OV_{DD}	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3 V	OV_{DD}	—	

6 PLL Configurations

The internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (266- and 300-MHz Parts)

Ref. No.	PLL_CFG [0:4] [10,13]	266-MHz Part [9]			300-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ MemBus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000[12]	25–35[5]	75–105	188–263	25–40[5,7]	75–120	188–300	3 (2)	2.5 (2)
1	00001[12]	25–29[5]	75–88	225–264	25–33[5]	75–99	225–297	3 (2)	3 (2)
2	00010[11]	50[18]–59[5,7]	50–59	225–266	50[18]–66[1]	50–66	225–297	1 (4)	4.5 (2)
3	00011[11,14]	50[17]–66[1]	50–66	100–133	50[17]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100[12]	25–46[4]	50–92	100–184	25–46[4]	50–92	100–184	2 (4)	2 (4)
6	00110[15]	Bypass			Bypass			Bypass	
7 Rev B	00111[14]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (Bypass)	3 (2)
7 Rev D	00111[14]	Not available							
8	01000[12]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (4)	3 (2)
9	01001[12]	45[6]–66[1]	90–132	180–264	45[6]–66[1]	90–132	180–264	2 (2)	2 (2)
A	01010[12]	25–29[5]	50–58	225–261	25–33[5]	50–66	225–297	2 (4)	4.5 (2)
B	01011[12]	45[3]–59[5]	68–88	204–264	45[3]–66[1]	68–99	204–297	1.5 (2)	3 (2)
C	01100[12]	36[6]–46[4]	72–92	180–230	36[6]–46[4]	72–92	180–230	2 (4)	2.5 (2)
D	01101[12]	45[3]–50[5]	68–75	238–263	45[3]–57[5]	68–85	238–298	1.5 (2)	3.5 (2)
E	01110[12]	30[6]–44[5]	60–88	180–264	30[6]–46[4]	60–92	180–276	2 (4)	3 (2)
F	01111[12]	25[5]	75	263	25–28[5]	75–85	263–298	3 (2)	3.5 (2)
10	10000[12]	30[6]–44[2,5]	90–132	180–264	30[6]–44[2]	90–132	180–264	3 (2)	2 (2)
11	10001[12]	25–26[5,7]	100–106	250–266	25–29[2]	100–116	250–290	4 (2)	2.5 (2)
12	10010[12]	60[6]–66[1]	90–99	180–198	60[6]–66[1]	90–99	180–198	1.5 (2)	2 (2)

Table 18. PLL Configurations (333- and 350-MHz Parts) (continued)

Ref	PLL_CFG[0:4] [10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
2	00010[11]	50[18]–66[1]	50–66	225–297	50[18]–66[1]	50–66	225–297	1 (4)	4.5 (2)
3	00011[11,14]	50[17]–66[1]	50–66	100–133	50[17]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100[12]	25–46[4]	50–92	100–184	25–46[4]	50–92	100–184	2 (4)	2 (4)
6	00110[15]	Bypass			Bypass			Bypass	
7 Rev B	00111[14]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (Bypass)	3 (2)
7 Rev D	00111[14]	Not available			25	100	350	4(2)	3.5(2)
8	01000[12]	60[6]–66[1]	60–66	180–198	60[6]–66[1]	60–66	180–198	1 (4)	3 (2)
9	01001[12]	45[6]–66[1]	90–132	180–264	45[6]–66[1]	90–132	180–264	2 (2)	2 (2)
A	01010[12]	25–37[5,7]	50–74	225–333	25–38[5]	50–76	225–342	2 (4)	4.5 (2)
B	01011[12]	45[3]–66[1]	68–99	204–297	45[3]–66[1]	68–99	204–297	1.5 (2)	3 (2)
C	01100[12]	36[6]–46[4]	72–92	180–230	36[6]–46[4]	72–92	180–230	2 (4)	2.5 (2)
D	01101[12]	45[3]–63[5,7]	68–95	238–333	45[3]–66[1]	68–99	238–347	1.5 (2)	3.5 (2)
E	01110[12]	30[6]–46[4]	60–92	180–276	30[6]–46[4]	60–92	180–276	2 (4)	3 (2)
F	01111[12]	25–31[5]	75–93	263–326	25–33[5]	75–99	263–347	3 (2)	3.5 (2)
10	10000[12]	30[6]–44[2]	90–132	180–264	30[6]–44[2]	90–132	180–264	3 (2)	2 (2)
11	10001[12]	25–33[2,16]	100–132	250–330	25–33[2,16]	100–132	250–330	4 (2)	2.5 (2)
12	10010[12]	60[6]–66[1]	90–99	180–198	60[6]–66[1]	90–99	180–198	1.5 (2)	2 (2)
13	10011[12]	25–27[5]	100–108	300–324	25–29[5]	100–116	300–348	4 (2)	3 (2)
14	10100[12]	26[6]–47[4]	52–94	182–329	26[6]–47[4]	52–94	182–329	2 (4)	3.5 (2)
15	10101[12]	27[3]–33[5]	68–83	272–332	27[3]–34[5]	68–85	272–340	2.5 (2)	4 (2)
16	10110[12]	25–41[5]	50–82	200–328	25–43[5]	50–86	200–344	2 (4)	4 (2)
17	10111[12]	25–33[2]	100–132	200–264	25–33[2]	100–132	200–264	4 (2)	2 (2)
18	11000[12]	27[3]–44[5]	68–110	204–330	27[3]–46[5]	68–115	204–345	2.5 (2)	3 (2)
19	11001[12]	36[6]–66[1]	72–132	180–330	36[6]–66[1]	72–132	180–330	2 (2)	2.5 (2)
1A	11010[12]	50[18]–66[1]	50–66	200–264	50[18]–66[1]	50–66	200–264	1 (4)	4 (2)
1B	11011[12]	34[3]–55[5]	68–110	204–330	34[3]–58[5]	68–116	204–348	2 (2)	3 (2)
1C	11100[12]	44[3]–66[1]	66–99	198–297	44[3]–66[1]	66–99	198–297	1.5 (2)	3 (2)
1D	11101[12]	48[6]–66[1]	72–99	180–248	48[6]–66[1]	72–99	180–248	1.5 (2)	2.5(2)

7 System Design

This section provides electrical and thermal design recommendations for successful application of the MPC8245.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8245 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500-kHz to 10-MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 25 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), using multiple small capacitors of equal value is recommended over using multiple values.

Place the circuits as closely as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing from the capacitors to the input signal pins should be as direct as possible with minimal inductance of vias.

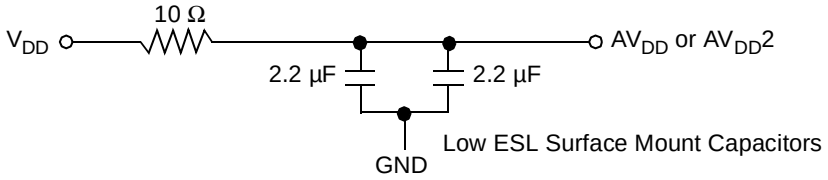


Figure 25. PLL Power Supply Filter Circuit

7.2 Decoupling Recommendations

Due to its dynamic power management feature, large address and data buses, and high operating frequencies, the MPC8245 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8245 system, and the MPC8245 itself requires a clean, tightly regulated source of power. Therefore, place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin. These decoupling capacitors should receive their power from dedicated power planes in the PCB, with short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic 0 level is read into the configuration bits during reset if the default logic 1 level is not desired.

Any other unused active low input pins should be tied to a logic-one level through weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND through weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8245 PCI reference voltage (LV_{DD}) pins should be connected to a 3.3 ± 0.3 V power supply if interfacing the MPC8245 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to a 5.0 V ± 5% power supply if interfacing the MPC8245 into a 5-V PCI bus system. For either reference voltage, the MPC8245 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8245 tolerates 5-V signals when interfaced into a 5-V PCI bus system.

7.6 MPC8245 Compatibility with MPC8240

The MPC8245 AC timing specifications are backward-compatible with those of the MPC8240, except for the requirements of item 11 in Table 10. Timing adjustments are needed as specified for T_{os} (SDRAM_SYNC_IN to *sys_logic_clk* offset) time requirements.

The MPC8245 does not support the SDRAM flow-through memory interface.

The nominal core V_{DD} power supply changes from 2.5 V on the MPC8240 to 1.8/2.0 V on the MPC8245. See Table 2.

For example, the MPC8245 PLL_CFG[0:4] setting 0x02 (0b00010) has a different PCI-to-Mem and Mem-to-CPU multiplier ratio than the same setting on the MPC8240, so it is not backward-compatible. See Table 17.

Most of the MPC8240 PLL_CFG[0:4] settings are subsets of the PCI_SYNC_IN input frequency range accepted by the MPC8245. However, the parts are not fully backward-compatible since the ranges of the two parts do not always match. Modes 0x8 and 0x18 of the MPC8245 are not compatible with settings 0x8 and 0x18 on the MPC8240. See Table 17 and Table 18.

Two reset configuration signals on the MPC8245 are not used as reset configuration signals on the MPC8240: SDMA0 and SDMA1.

The SDMA0 reset configuration pin selects between the MPC8245 DUART and the MPC8240 backward-compatible mode PCI_CLK[0:4] functionality on these multiplexed signals. The default state (logic 1) of SDMA0 selects the MPC8240 backward-compatible mode of PCI_CLK[0:4] functionality while a logic 0 state on the SDMA0 signal selects DUART functionality. In DUART mode, four of the five PCI clocks, PCI_CLK[0:3], are not available.

The SDMA1 reset configuration pin selects between MPC8245 extended ROM functionality and MPC8240 backward-compatible functionality on the multiplexed signals: TBEN, $\overline{\text{CHKSTOP\_IN}}$,

$\overline{\text{SRESET}}$, TRIG_IN, and TRIG_OUT. The default state (logic 1) of SDMA1 selects the MPC8240 backward-compatible mode functionality, while a logic 0 state on the SDMA1 signal selects extended ROM functionality. In extended ROM mode, the TBEN, $\overline{\text{CHKSTOP\_IN}}$, $\overline{\text{SRESET}}$, TRIG_IN, and TRIG_OUT functionalities are not available.

The driver names and pin capability of the MPC8245 and the MPC8240 differ slightly. Refer to the drive capability table (for the ODCR register at 0x73) in the *MPC8240 Integrated Processor Hardware Specifications* and Table 4.

The programmable PCI output valid and output hold feature controlled by bits in the power management configuration register 2 (PMCR2) <0x72> differs slightly in the MPC8245. For the MPC8240, three bits, PMCR2[6:4] = PCI_HOLD_DEL, are used to select 1 of 8 possible PCI output timing configurations. PMCR2[6:5] are software-controllable but are initially set by the reset configuration state of the $\overline{\text{MCP}}$ and CKE signals, respectively. Software can change PMCR2[4]. The default configuration for PMCR2[6:4] = 0b110 since the $\overline{\text{MCP}}$ and CKE signals have internal pull-up resistors, but this default configuration does not select 33- or 66-MHz PCI operation output timing parameters for the MPC8240. Software makes this selection. For the MPC8245, only two bits in the power management configuration register 2 (PMCR2), PMCR2[5:4] = PCI_HOLD_DEL, control the variable PCI output timing. PMCR2[5:4] are software controllable but are initially set by the inverted reset configuration state of the $\overline{\text{MCP}}$ and CKE signals, respectively. The default configuration for PMCR2[5:4] = 0b00 since the $\overline{\text{MCP}}$ and CKE signals have internal pull-up resistors and the values from these signals are inverted; this default configuration selects 66-MHz PCI operation output timing parameters. There are four programmable PCI output timing configurations on the MPC8245. See Table 11.

Voltage sequencing requirements for the MPC8245 are similar to those for the MPC8240, with two exceptions in the MPC8245. In the MPC8245, the non-PCI input voltages (V_{in}) must not be greater than GV_{DD} or OV_{DD} by more than 0.6 V at all times, including during power-on reset (see Caution 5 in Table 2). Second, LV_{DD} must not exceed OV_{DD} by more than 3.0 V at any time, including during power-on reset (see Caution 10 in Table 2); the allowable separation between LV_{DD} and OV_{DD} is 3.6 V for the MPC8240.

There is no LAV_{DD} input voltage supply signal on the MPC8245 since the SDRAM clock delay-locked loop (DLL) has power supplied internally. Signal D17 should be treated as a NC for the MPC8245. Application note AN2128 highlights the differences between the MPC8240 and the MPC8245.

7.7 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the Power Architecture technology. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, more reliable power-on reset performance can be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG, with additional status monitoring signals. The COP port must independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to control the processor. If the target system has independent

reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

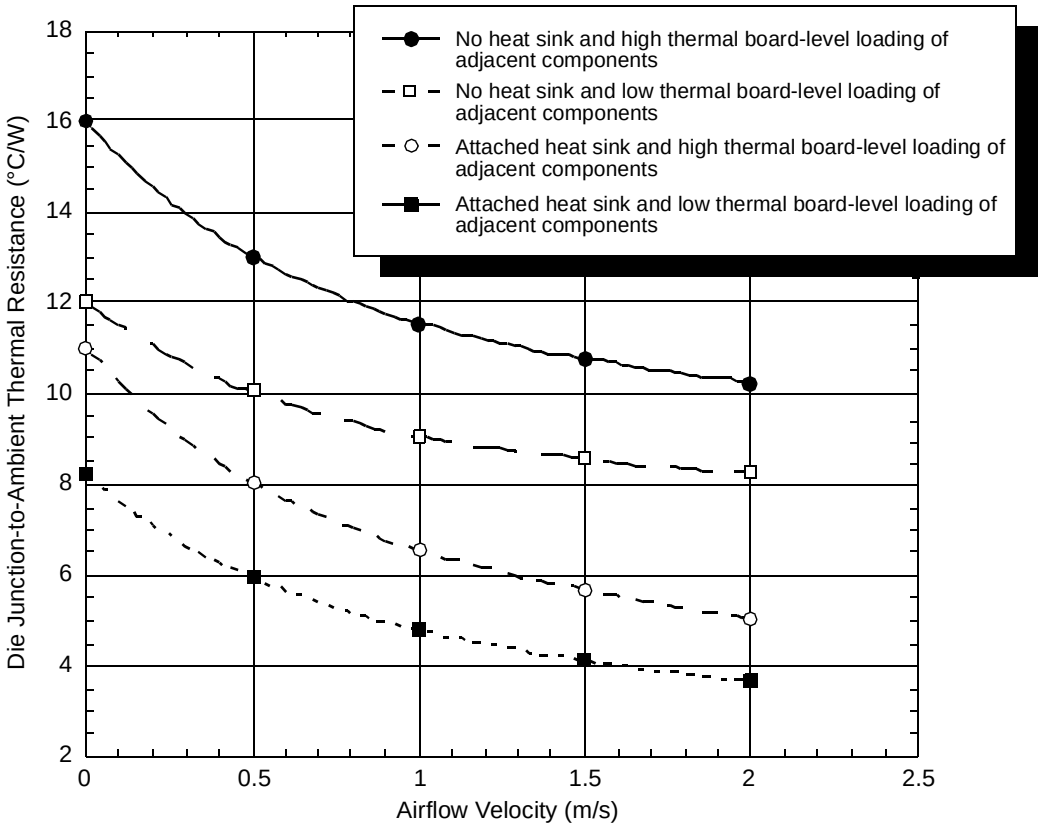


Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. Several commercially-available heat sinks for the MPC8245 are provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
2	—	Globally changed EPIC to PIC. Section 1.4.1.4—Note 5: Changed register reference from 0x72 to 0x73. Section 1.4.1.5—Table 5: Updated power dissipation numbers based on latest characterization data. Section 1.4.2—Table 6: Updated table to show more thermal specifications. Section 1.4.3—Table 7: Updated minimum memory bus value to 50 MHz. Section 1.4.3.1—Changed equations for DLL locking range based on characterization data. Added updates and reference to AN2164 for note 6. Added table defining Tdp parameters. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Table 10: Changed bit definitions for tap points. Updated note on Tos and added reference to AN2164 for note 7. Updated Figure 9 to show significance of Tos. Section 1.4.3.4—Added column for SDRAM_CLK @ 133 MHz Sections 1.5.1 and 1.5.2—Corrected packaging information to state TBGA packaging. Section 1.5.3—Corrected some signals in Table 16 which were missing overbars in the Rev 1.0 release of the document. Section 1.6—Updated Note 10 of Tables 18 and 19. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.9—Updated format of tables in Ordering Information section.
1	—	Updated document template. Section 1.4.1.4—Changed the driver type names in Table 6 to match with the names used in the MPC8245 Reference Manual. Section 1.5.3—Updated driver type names for signals in Table 16 to match with names used in the MPC8245 Integrated Processor Reference Manual. Section 1.4.1.2—Updated Table 7 to refer to new PLL Tables for VCO limits. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid timing. Section 1.5.1—Updated solder balls information to 62Sn/36PB/2Ag. Section 1.6—Updated PLL Tables 17 and 18 and appropriate notes to reflect changes of VCO ranges for memory and CPU frequencies. Section 1.7—Updated voltage sequencing requirements in Table 2 and removed Section 1.7.2. Section 1.7.8—Updated TRST information and Figure 26. New Section 1.7.2—Updated the range of I/O power consumption numbers for OV_{DD} and GV_{DD} to correct values as in Table 5. Updated fastest frequency combination to 66:100:350 MHz. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of Ordering Information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.
0.5	—	Corrected labels for Figures 5 through 8.

Table 19. Revision History Table (continued)

Revision	Date	Substantive Change(s)
0.2	—	Changed core supply voltage to 2.0 ± 100 mV in Section 1.3. (Supply voltage of 1.8 ± 100 mV is no longer recommended.) Changed rows 2, 5, and 6 of Table 2 to 2.0 ± 100 mV in the “Recommended Value” column. Changed the power consumption numbers in Table 5 to reflect the power values for V_{DD} = 2.0 V. (Notes 2, 3, 4, and 5 of the table were also updated to reflect the new value of V_{DD}.) Updated Table 9 for $V_{DD}/AV_{DD}/AV_{DD}2$ to 2.0 ± 100 mV. Table 8: $V_{DD}/AV_{DD}/AV_{DD}2$ was changed to 2.0 V for both CPU frequency offerings. Note 2 was updated by removing the “at reduced voltage...” statement. Table 10: Update maximum time of the rows 12a0 through 12a3. Table 16: Fixed overbars for the active-low signals. Changed pin type information for V_{DD}, AV_{DD}, and $AV_{DD}2$ to 2.0 V. Changed Note 16 of Table 17 to a value of 2.0 V for $V_{DD}/AV_{DD}/AV_{DD}2$. Removed second sentence of the second paragraph in Section 1.7.2 because it referenced information about a 1.8-V design. Removed reference to 1.8 V in third sentence of Section 1.7.7.

9 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 9.1, “Part Numbers Fully Addressed by This Document.” Section 9.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

9.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC8245. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number. The revision level can be determined by reading the Revision ID register at address offset 0x08.

Table 20. Part Numbering Nomenclature

MPC	*nnnn*	L	*xx*	*nnn*	*x*

Product Code	Part Identifier	Process Descriptor	Package [1]	Processor Frequency [2] (MHz)	Revision Level	Processor Version Register Value
MPC	8245	L: 0° to 105°C	ZU = TBGA V V = Lead-free TBGA	266, 300 1.7 V to 2.1 V	D:1.4 Rev ID:0x14	0x80811014
		L: 0° to 105°C	ZU = TBGA V V = Lead-free TBGA	333, 350 1.9 V to 2.2 V		

Notes:

1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by a hardware specifications addendum may support other maximum core frequencies.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC8245EC
Rev. 10
08/2007