Infineon Technologies - MB95F816KPMC-G-SNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f816kpmc-g-sne2

Part number / Parameter	MB95F814K	MB95F816K	MB95F818K
Standby mode	There are four standby modes as follows: • Stop mode • Sleep mode • Watch mode • Time-base timer mode In standby mode, two further options can be selected: normal standby mode and deep standby mode		
Package	FPT-64P-M38 FPT-64P-M39		

2. Packages And Corresponding Products

Part number / Package	MB95F814K	MB95F816K	MB95F818K
FPT-64P-M38	O	O	O
FPT-64P-M39	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash program/erase.
  For details of current consumption, see “Electrical Characteristics”.

- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

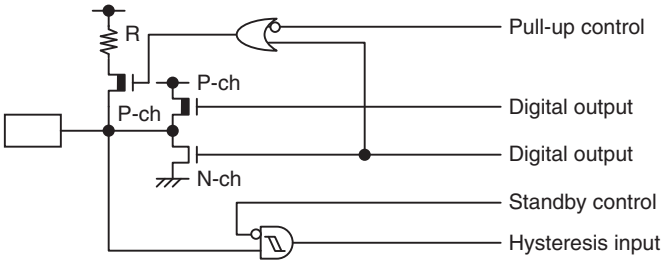
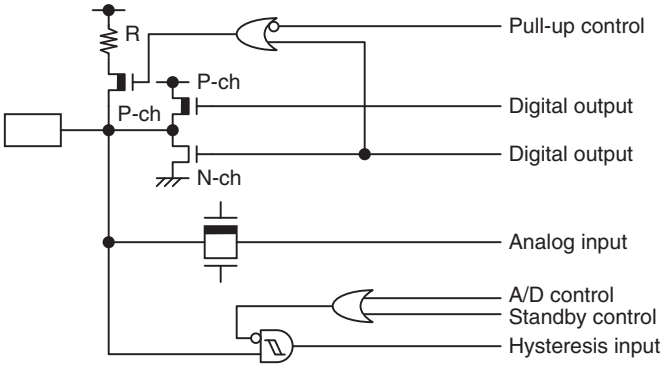
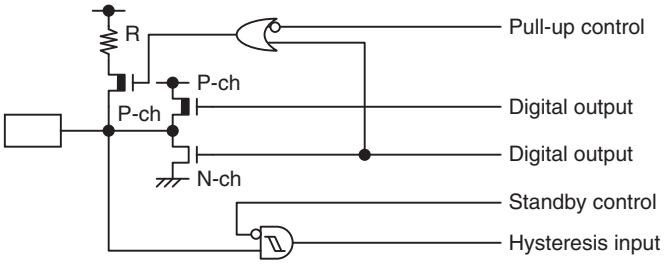
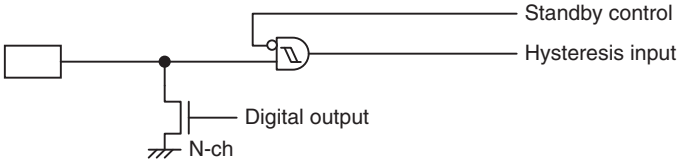
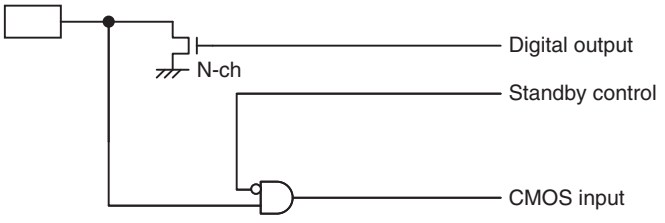
- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function
  The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 25 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95810K Series Hardware Manual”.

5. Pin Functions

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
1	AVCC	—	Analog power supply pin for 8/10-bit A/D converter	—	—	—	—
2	AVR	—	Reference input pin for 8/10-bit A/D converter	—	—	—	—
3	PE3	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT13		External interrupt input pin				
4	PE2	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT12		External interrupt input pin				
5	PE1	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT11		External interrupt input pin				
6	PE0	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT10		External interrupt input pin				
7	P83	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TRG0*4		16-bit PPG timer ch. 0 trigger input pin				
	ADTG*4		8/10-bit A/D converter trigger input pin				
8	P82	F	General-purpose I/O port	Hysteresis	CMOS	—	O
9	P81	F	General-purpose I/O port	Hysteresis	CMOS	—	O
10	P80	F	General-purpose I/O port	Hysteresis	CMOS	—	O
11	P71	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TI0		16-bit reload timer ch. 0 input pin				
12	P70	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO0		16-bit reload timer ch. 0 output pin				
13	P72	F	General-purpose I/O port	Hysteresis	CMOS	—	O
14	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
15	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
16	VSS	—	Power supply pin (GND)	—	—	—	—
17	VCC	—	Power supply pin	—	—	—	—
18	C	—	Decoupling capacitor connection pin	—	—	—	—
19	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
20	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
21	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	$\overline{RST}$		Reset pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
22	P00	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT00		External interrupt input pin				
23	P01	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT01		External interrupt input pin				
24	P02	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT02		External interrupt input pin				
25	P03	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT03		External interrupt input pin				
26	P04	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT04		External interrupt input pin				
27	P05	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT05		External interrupt input pin				
28	P06	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT06		External interrupt input pin				
29	P07	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT07		External interrupt input pin				
30	P10	I	General-purpose I/O port	CMOS	CMOS	—	O
	UI0		UART/SIO ch. 0 data input pin				
31	P11	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	UO0		UART/SIO ch. 0 data output pin				
32	P12	G	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
33	P13	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	UCK0		UART/SIO ch. 0 clock I/O pin				
	TRG0*4		16-bit PPG timer ch. 0 trigger input pin				
	ADTG*4		8/10-bit A/D converter trigger input pin				
34	P14	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG0		16-bit PPG timer ch. 0 output pin				
35	P20	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG00		8/16-bit PPG ch. 0 output pin				
36	P21	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG01		8/16-bit PPG ch. 0 output pin				
37	P22	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO00		8/16-bit composite timer ch. 0 output pin				
38	P23	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO01		8/16-bit composite timer ch. 0 output pin				

Type	Circuit	Remarks
D		• CMOS output • Hysteresis input • Pull-up control • High current output
E		• CMOS output • Hysteresis input • Pull-up control • Analog input
F		• CMOS output • Hysteresis input • Pull-up control
G		• N-ch open drain output • Hysteresis input
H		• N-ch open drain output • CMOS input

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

9. Pin Connection

- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin
  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

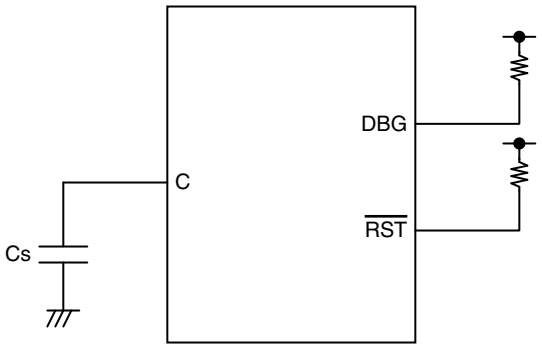
- $\overline{RST}$ pin
  Connect the $\overline{RST}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{RST}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
  The PF2/$\overline{RST}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{RST}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

- Analog power supply
  Always set the same potential to the AV_{CC} pin and the V_{CC} pin. When V_{CC} is larger than AV_{CC}, the current may flow through the AN00 to AN11 pins.

- Treatment of power supply pins on the 8/10-bit A/D converter
  Ensure that AV_{CC} is equal to V_{CC} and AV_{SS} equal to V_{SS} even when the 8/10-bit A/D converter is not in use.
  Noise riding on the AV_{CC} pin may cause accuracy degradation. Therefore, connect a ceramic capacitor of 0.1 µF (approx.) as a bypass capacitor between the AV_{CC} pin and the AV_{SS} pin in the vicinity of this device.

- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{\text{RST}}$/C pins connection diagram



- Note on serial communication
  In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

- Correspondence between registers and pins for port 4

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**P43**	**P42**	**P41**	**P40**
PDR4	-	-	-	-	bit3	bit2	bit1	bit0
DDR4								
PUL4								
AIDRH								

15.5.4 Port 4 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
  - If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR4 register returns the PDR4 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using a pin shared with the analog input function as an input port, set the corresponding bit in the A/D input disable register (upper) (AIDRH) to “1”.
  - If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
  - When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRH register corresponding to that pin to “1”.
  - Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

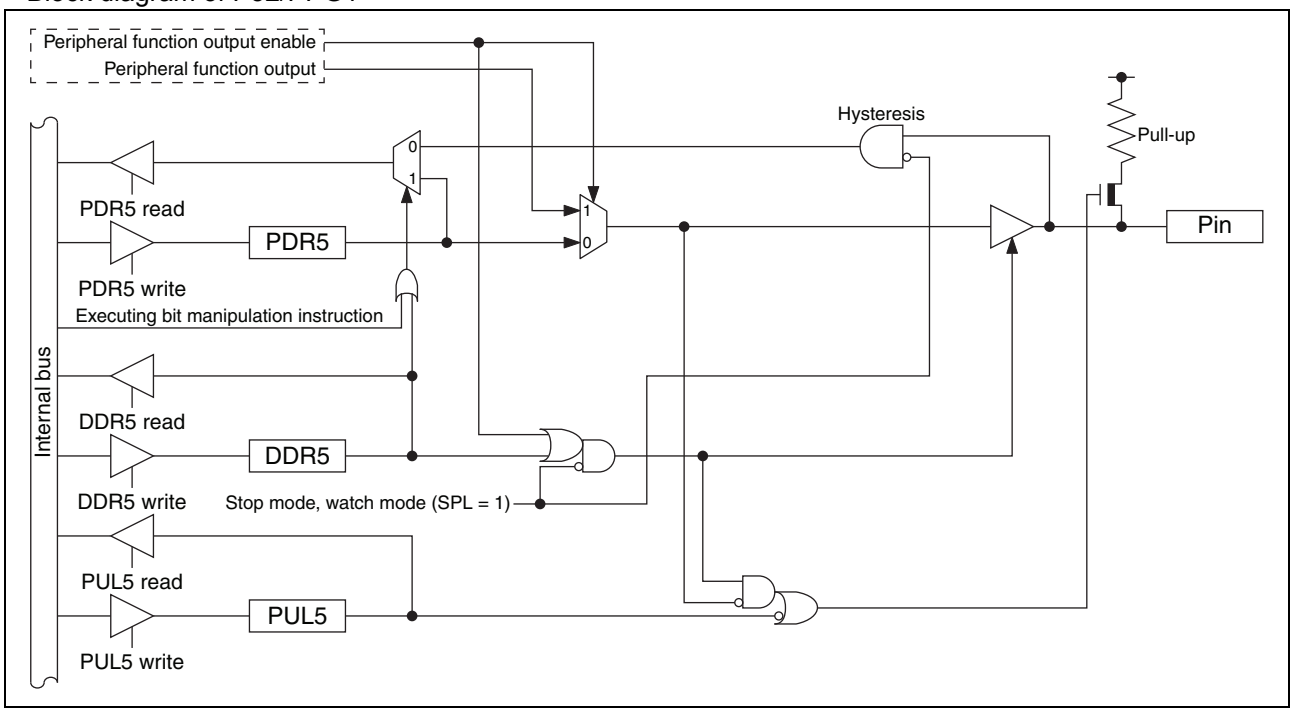
- Operation at reset
  If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRH register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an analog input pin
  - Set the bit in the DDR4 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin

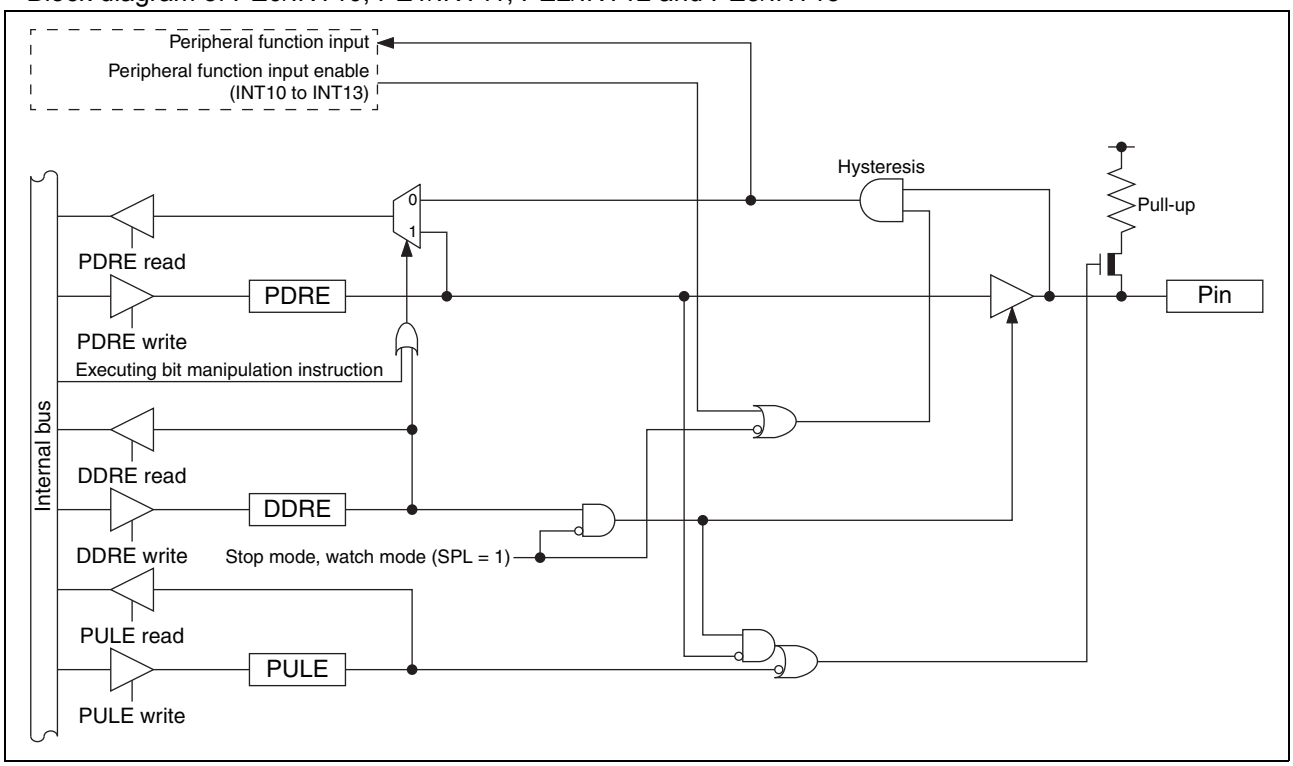
- P52/PPG1 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 1 output pin (PPG1)

- Block diagram of P52/PPG1



- P53/TRG1 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 1 trigger input pin (TRG1)

• Block diagram of PE0/INT10, PE1/INT11, PE2/INT12 and PE3/INT13



15.10.3 Port E registers

• Port E register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRE	0	Pin state is “L” level.	PDRE value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRE value is “1”.	As output port, outputs “H” level.
DDRE	0	Port input enabled		
	1	Port output enabled		
PULE	0	Pull-up disabled		
	1	Pull-up enabled		

• Correspondence between registers and pins for port E

	Correspondence between related register bits and pins							
Pin name	-	-	-	-	PE3	PE2	PE1	PE0
PDRE	-	-	-	-	bit3	bit2	bit1	bit0
DDRE								
PULE								

15.12.3 Port G registers

- Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

15.12.4 Port G operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
  - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRG register returns the PDRG register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P12/DBG	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z - Input blocked*2	- Hi-Z - Input enabled*3 (However, it does not function.)
P13/UCK0/ TRG0/ADTG	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *6	- Hi-Z*5 - Input blocked*2, *6	- Previous state kept - Input blocked*2, *6	- Hi-Z*5 - Input blocked*2, *6	- Hi-Z - Input enabled*3 (However, it does not function.)
P14/PPG0 P20/PPG00 P21/PPG01 P22/TO00 P23/TO01	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Hi-Z - Input enabled*3 (However, it does not function.)
P24/EC0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *6	- Hi-Z*5 - Input blocked*2, *6	- Previous state kept - Input blocked*2, *6	- Hi-Z*5 - Input blocked*2, *6	- Hi-Z - Input enabled*3 (However, it does not function.)
P32/AN02/ CMP0_O P35/AN05/ CMP1_O	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept*8 - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Previous state kept*8 - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Hi-Z - Input blocked*2
P30/AN00/ CMP0_N P31/AN01/ CMP0_P P33/AN03/ CMP1_N P34/AN04/ CMP1_P	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*2, *7	- Hi-Z*5 - Input blocked*2, *7	- Previous state kept - Input blocked*2, *7	- Hi-Z*5 - Input blocked*2, *7	- Hi-Z - Input blocked*2
P36/AN06 P37/AN07 P40/AN08 P41/AN09 P42/AN10 P43/AN11	I/O port/ analog input	I/O port/ analog input	- Previous state kept - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Hi-Z - Input blocked*2
P50/SCL P51/SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *9	- Hi-Z - Input blocked*2, *9	- Previous state kept - Input blocked*2, *9	- Hi-Z - Input blocked*2, *9	- Hi-Z - Input enabled*3 (However, it does not function.)

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	AV_{CC}, V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	*2
	AVR	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*3
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*4
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*4
"L" level maximum output current	I_{OL}	—	15	mA	
"L" level average current	I_{OLAV1}	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH}	—	–15	mA	
"H" level average current	I_{OHAV1}	—	–4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		–8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	–100	mA	
"H" level total average output current	ΣI_{OHAV}	—	–47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.
*2: Apply equal potential to AV_{CC} and V_{CC}. AVR must not exceed AV_{CC}.
*3: V_1 and V_0 must not exceed V_{CC} + 0.3 V. V_1 must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.
*4: Specific pins: P00 to P07, P10, P11, P13, P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P60 to P67, P70 to P72, P80 to P83, PE0 to PE3, PF0, PF1, PG1, PG2
- Use under recommended operating conditions.
- Use with DC voltage (current).

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

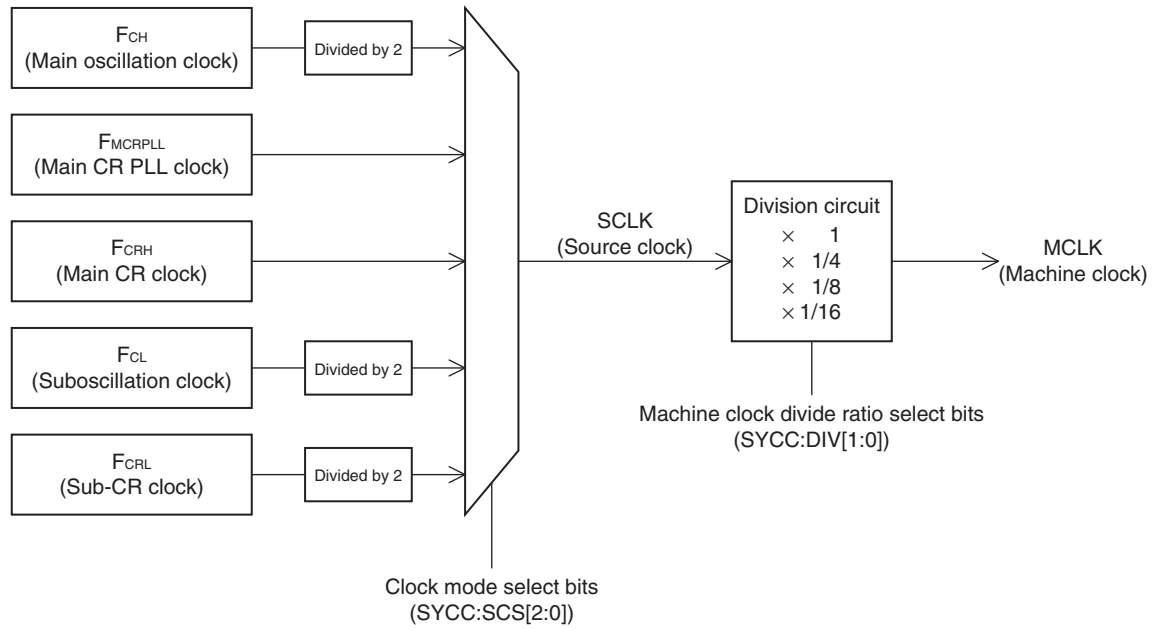
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*2		
Power supply current*3	I_V	V_{CC}	Current consumption of the comparator	—	60	160	µA	
	I_{LVD}		Current consumption of the low-voltage detection reset circuit	—	4	7	µA	With the LVD reset already enabled by the LVD reset circuit control register (LVDCC)
	I_{CRH}		Current consumption of the main CR oscillator	—	240	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	7	20	µA	
	I_{NSTBY}		Current consumption difference between normal standby mode and deep standby mode T_A = +25 °C	—	22	30	µA	
	I_A	AV_{CC}	V_{CC} = 5.5 V F_{CH} = 16 MHz Current consumption of the A/D converter	—	2	3.1	mA	
	I_{AH}		F_{CRH} = 4 MHz F_{MP} = 4 MHz Current consumption with the A/D converter halted T_A = +25 °C	—	1	5	µA	

*1: V_{CC} = 5.0 V, T_A = +25 °C

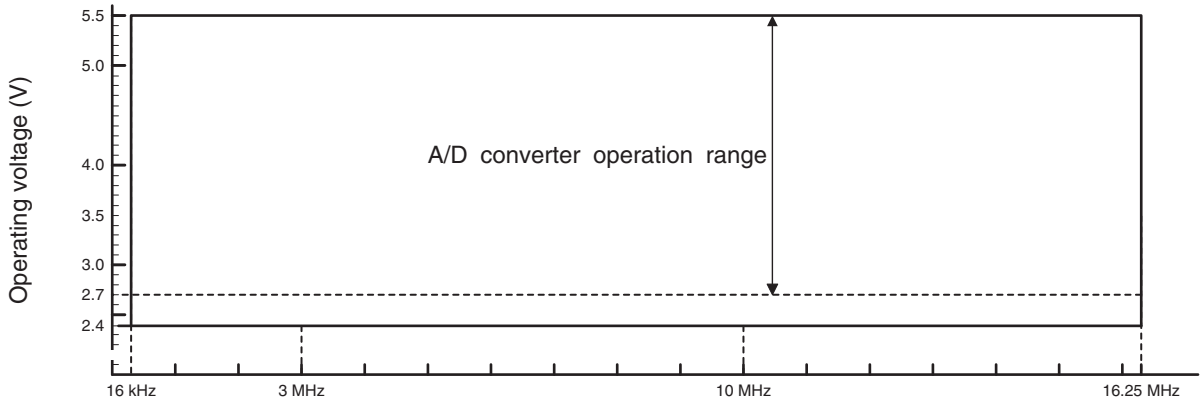
*2: V_{CC} = 5.5 V, T_A = +85 °C (unless otherwise specified)

*3:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (I_{LVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit (I_{LVD}), the current consumption of the CR oscillators (I_{CRH} or I_{CRL}) and one of the values from I_{CC} to I_{CCH}. In on-chip debug mode, the main CR oscillator (I_{CRH}) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.
- See “4. AC Characteristics Clock Timing” for F_{CH}, F_{CL}, F_{CRH} and F_{MCRPLL}.
- See “4. AC Characteristics Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current value in standby mode is measured in deep standby mode. The current consumption in normal standby mode is higher than that in deep standby mode. The power supply current value in normal standby mode can be found by adding the current consumption difference between normal standby mode and deep standby mode (I_{NSTBY}) to the power supply current value in deep standby mode. For details of normal standby mode and deep standby mode, refer to “CHAPTER 3 CLOCK CONTROLLER” in “New 8FX MB95810K Series Hardware Manual”.

• Schematic diagram of the clock generation block



• Operating voltage - Operating Frequency (T_A = –40 °C to +85 °C)

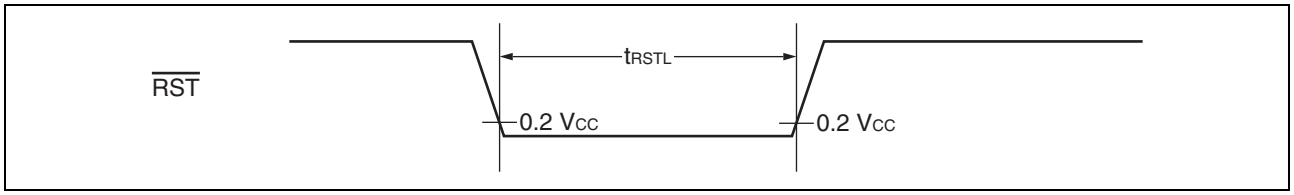


18.4.3 External Reset

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

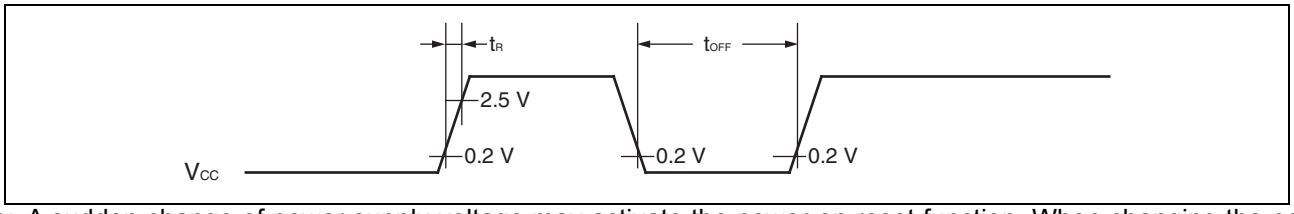
*: See "Source Clock/Machine Clock" for t_{MCLK}.



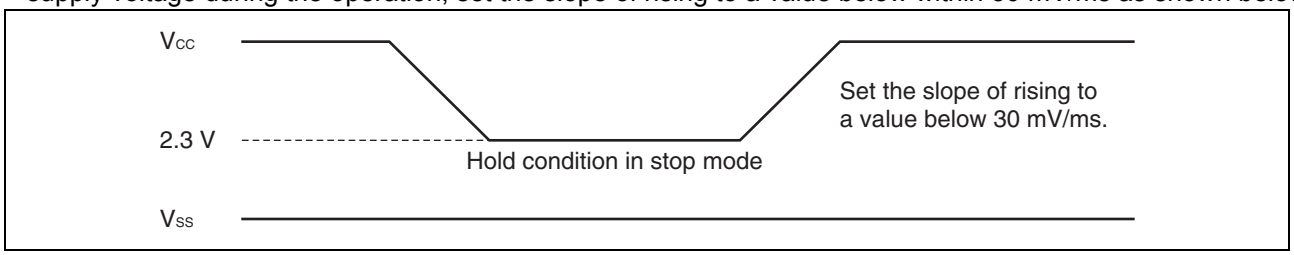
18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

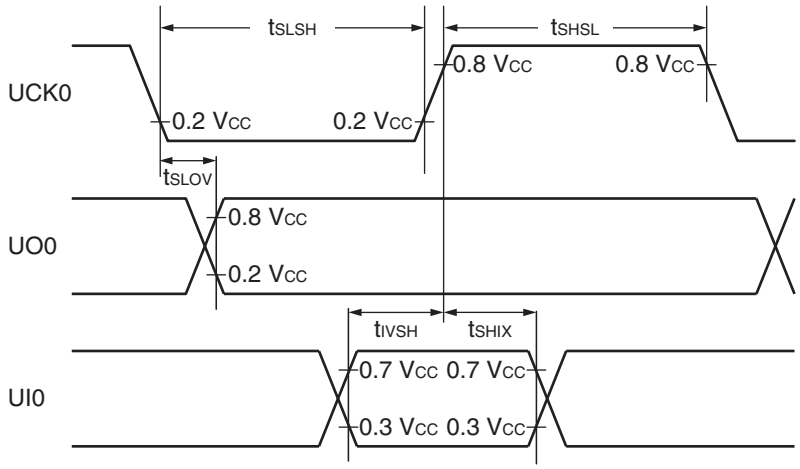
Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



- External shift clock mode



18.4.10 Comparator Timing

(V_{CC} = 2.88 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

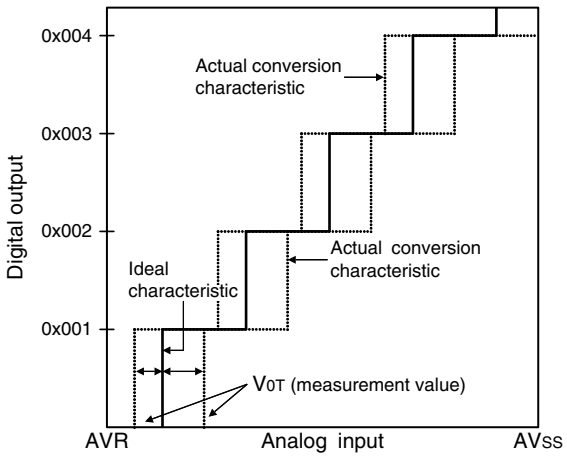
Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMP0_P, CMP0_N, CMP1_P, CMP1_N	0	—	V_{CC} – 1.3	V	
Offset voltage	CMP0_P, CMP0_N, CMP1_P, CMP1_N	–15	—	+15	mV	
Delay time	CMP0_O, CMP1_O	—	650	1200	ns	Overdrive 5 mV
		—	140	420	ns	Overdrive 50 mV
Power down delay	CMP0_O, CMP1_O	—	—	1200	ns	Power down recovery PD: 1 → 0
Power up stabilization wait time	CMP0_O, CMP1_O	—	—	1200	ns	Output stabilization time at power up

18.4.11 BGR for Comparator

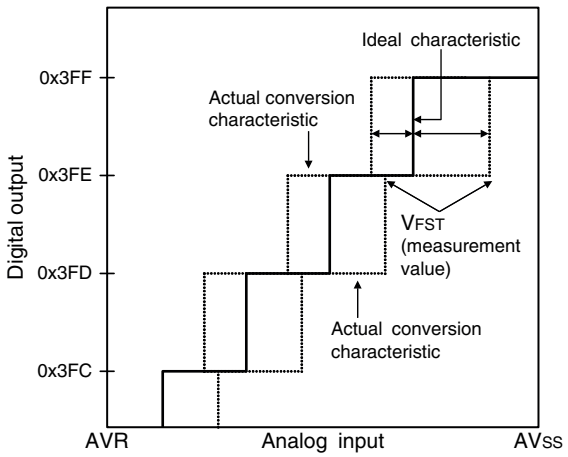
(V_{CC} = 2.88 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power up stabilization wait time	—	—	—	150	µs	Load: 10 pF
Output voltage	VBGR	1.1495	1.21	1.2705	V	

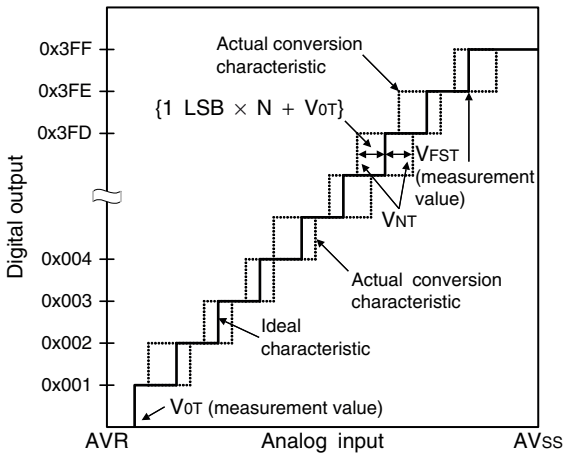
Zero transition error



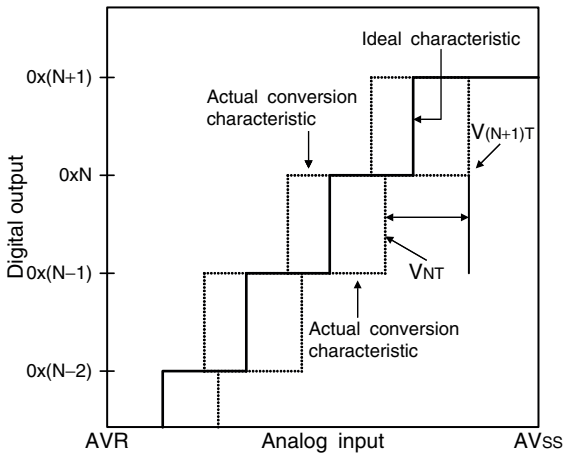
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

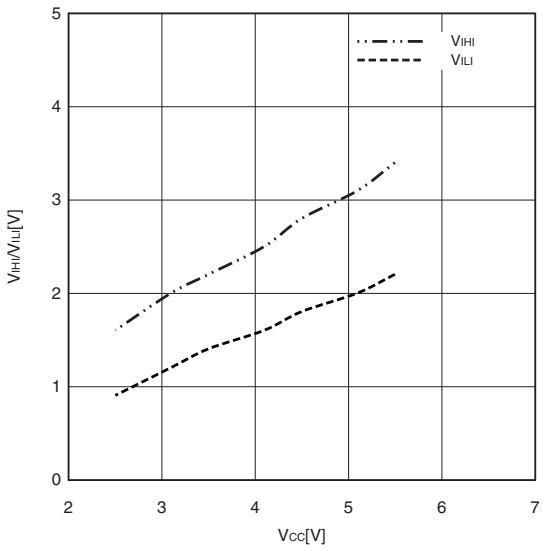
V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = AVR + 0.5 LSB [V]

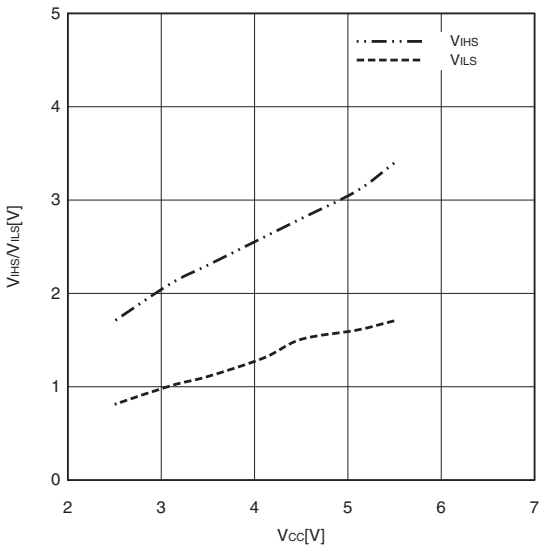
V_{FST} (ideal value) = AV_{SS} – 2 LSB [V]

- Input voltage characteristics

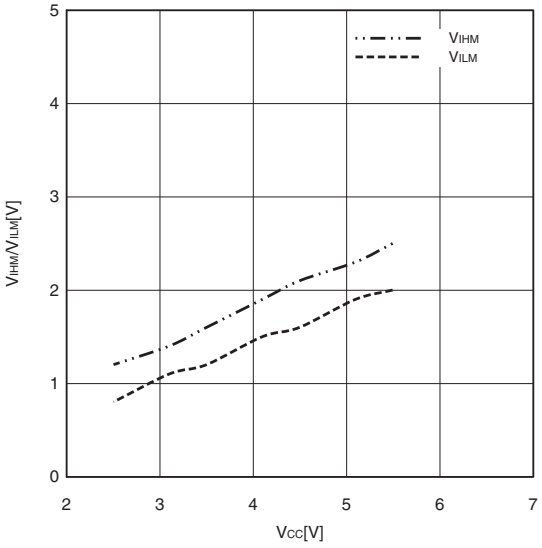
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25 °C



V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25 °C

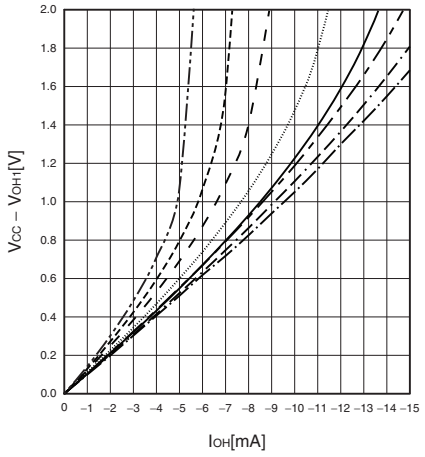


V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25 °C

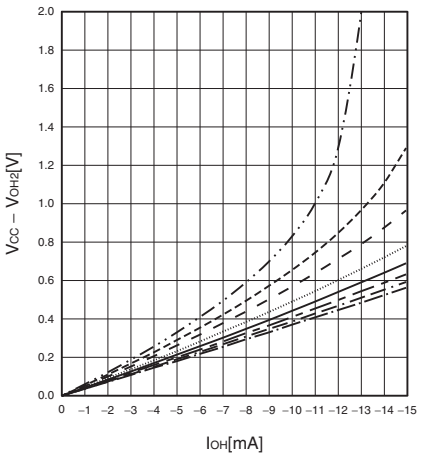


- Output voltage characteristics

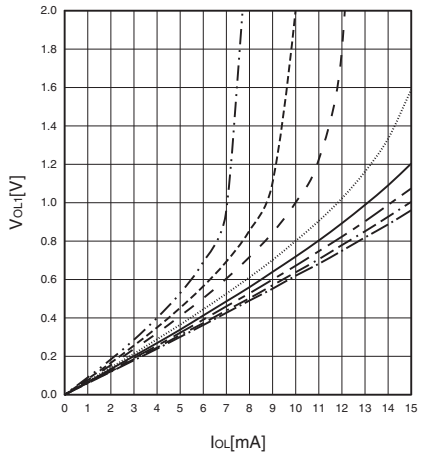
$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



$V_{OL1} - I_{OL}$
$T_A = +25\ °C$



$V_{OL2} - I_{OL}$
$T_A = +25\ °C$