Infineon Technologies - MB95F818KPMC-G-SNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

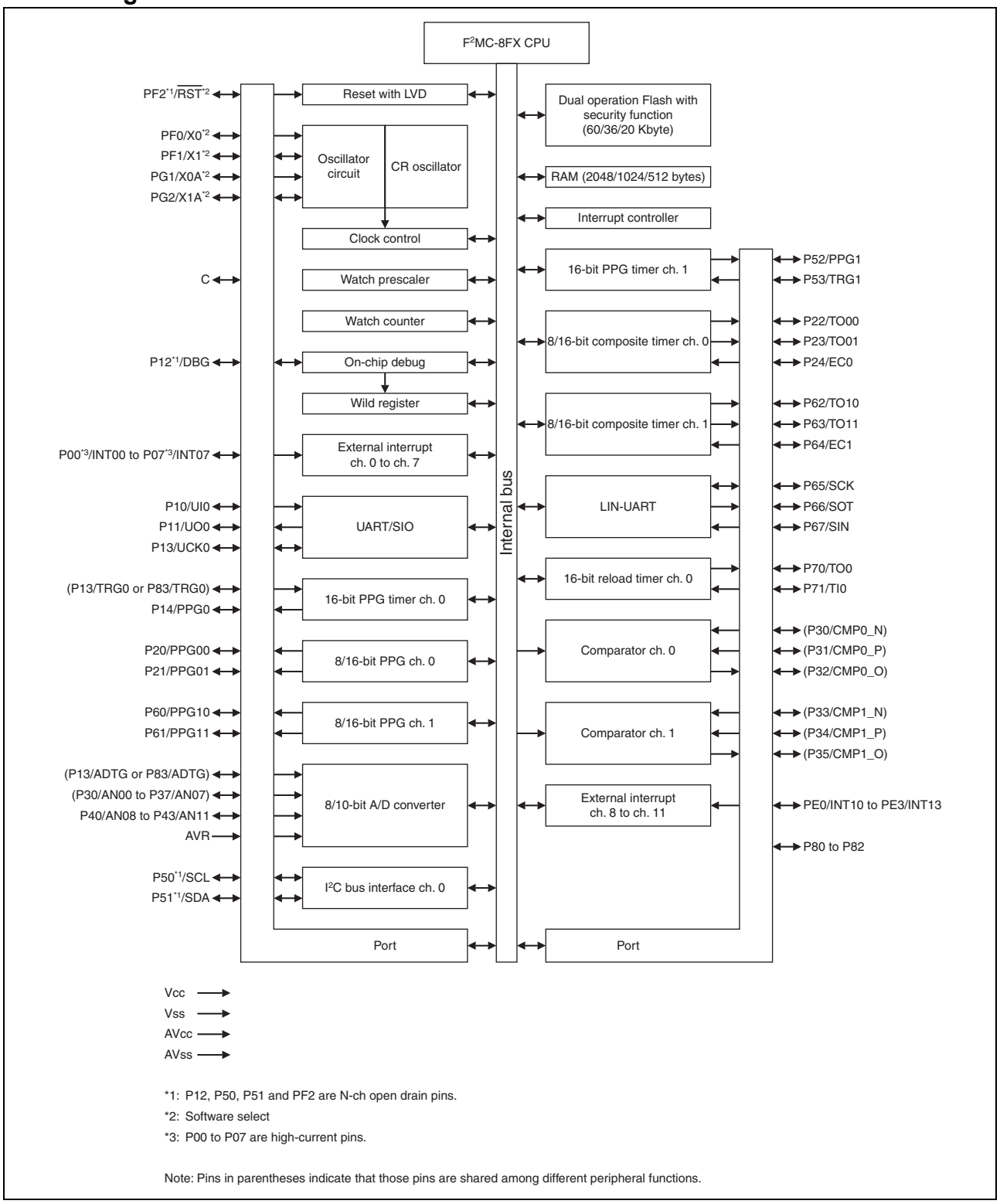
Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f818kpmc-g-sne2

Contents

5. Pin Functions

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
1	AVCC	—	Analog power supply pin for 8/10-bit A/D converter	—	—	—	—
2	AVR	—	Reference input pin for 8/10-bit A/D converter	—	—	—	—
3	PE3	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT13		External interrupt input pin				
4	PE2	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT12		External interrupt input pin				
5	PE1	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT11		External interrupt input pin				
6	PE0	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT10		External interrupt input pin				
7	P83	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TRG0*4		16-bit PPG timer ch. 0 trigger input pin				
	ADTG*4		8/10-bit A/D converter trigger input pin				
8	P82	F	General-purpose I/O port	Hysteresis	CMOS	—	O
9	P81	F	General-purpose I/O port	Hysteresis	CMOS	—	O
10	P80	F	General-purpose I/O port	Hysteresis	CMOS	—	O
11	P71	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TI0		16-bit reload timer ch. 0 input pin				
12	P70	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO0		16-bit reload timer ch. 0 output pin				
13	P72	F	General-purpose I/O port	Hysteresis	CMOS	—	O
14	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
15	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
16	VSS	—	Power supply pin (GND)	—	—	—	—
17	VCC	—	Power supply pin	—	—	—	—
18	C	—	Decoupling capacitor connection pin	—	—	—	—
19	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
20	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
21	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	$\overline{RST}$		Reset pin				

10. Block Diagram



*1: P12, P50, P51 and PF2 are N-ch open drain pins.

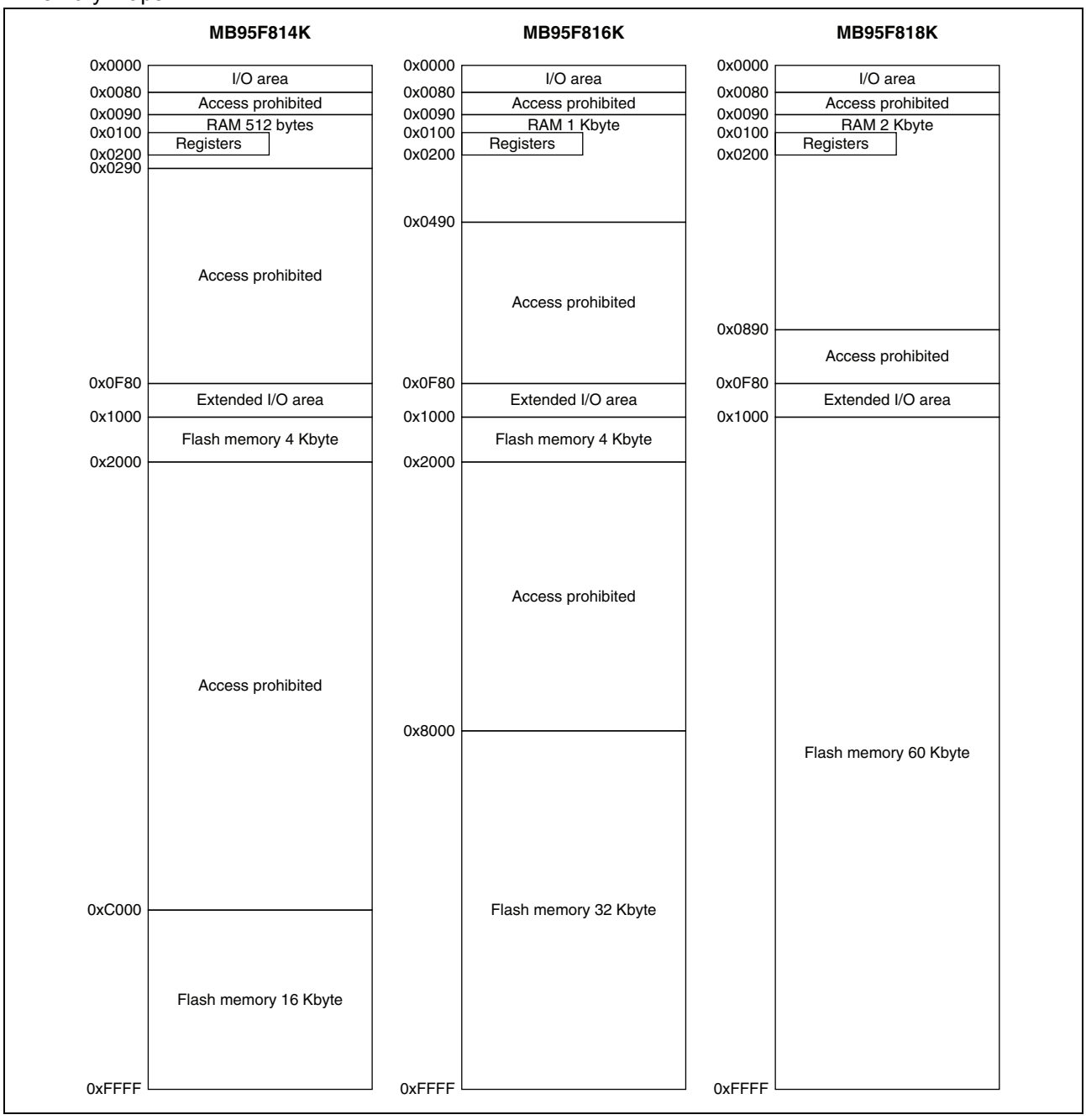
*2: Software select

*3: P00 to P07 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

11. CPU Core

- Memory space
  The memory space of the MB95810K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95810K Series are shown below.
- Memory maps



Address	Register abbreviation	Register name	R/W	Initial value
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	TMRH0	16-bit reload timer timer register (upper) ch. 0	R/W	0b00000000
	TMRLRH0	16-bit reload timer reload register (upper) ch. 0		
0x0FA7	TMRL0	16-bit reload timer timer register (lower) ch. 0	R/W	0b00000000
	TMRLRL0	16-bit reload timer reload register (lower) ch. 0		
0x0FA8, 0x0FA9	—	(Disabled)	—	—
0x0FAA	PDCRH0	16-bit PPG downcounter register (upper) ch. 0	R	0b00000000
0x0FAB	PDCRL0	16-bit PPG downcounter register (lower) ch. 0	R	0b00000000
0x0FAC	PCSRH0	16-bit PPG cycle setting buffer register (upper) ch. 0	R/W	0b11111111
0x0FAD	PCSRL0	16-bit PPG cycle setting buffer register (lower) ch. 0	R/W	0b11111111
0x0FAE	PDUTH0	16-bit PPG duty setting buffer register (upper) ch. 0	R/W	0b11111111
0x0FAF	PDUTL0	16-bit PPG duty setting buffer register (lower) ch. 0	R/W	0b11111111
0x0FB0	PDCRH1	16-bit PPG downcounter register (upper) ch. 1	R	0b00000000
0x0FB1	PDCRL1	16-bit PPG downcounter register (lower) ch. 1	R	0b00000000
0x0FB2	PCSRH1	16-bit PPG cycle setting buffer register (upper) ch. 1	R/W	0b11111111
0x0FB3	PCSRL1	16-bit PPG cycle setting buffer register (lower) ch. 1	R/W	0b11111111
0x0FB4	PDUTH1	16-bit PPG duty setting buffer register (upper) ch. 1	R/W	0b11111111
0x0FB5	PDUTL1	16-bit PPG duty setting buffer register (lower) ch. 1	R/W	0b11111111
0x0FB6 to 0x0FBB	—	(Disabled)	—	—
0x0FBC	BGR1	LIN-UART baud rate generator register 1	R/W	0b00000000
0x0FBD	BGR0	LIN-UART baud rate generator register 0	R/W	0b00000000
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0, 0x0FC1	—	(Disabled)	—	—
0x0FC2	AIDRH	A/D input disable register (upper)	R/W	0b00000000
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	LVDPW	LVD reset circuit password register	R/W	0b00000000

Register name		Read/Write	Initial value
A/D input disable register (upper)	AIDRH	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

15.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

15.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- Port 0 pull-up register (PUL0)

15.1.2 Block diagrams of port 0

- P00/INT00 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT00)

- P01/INT01 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT01)

- P02/INT02 pin
  This pin has the following peripheral function:
  External interrupt input pin (INT02)

- P03/INT03 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT03)

- P04/INT04 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT04)

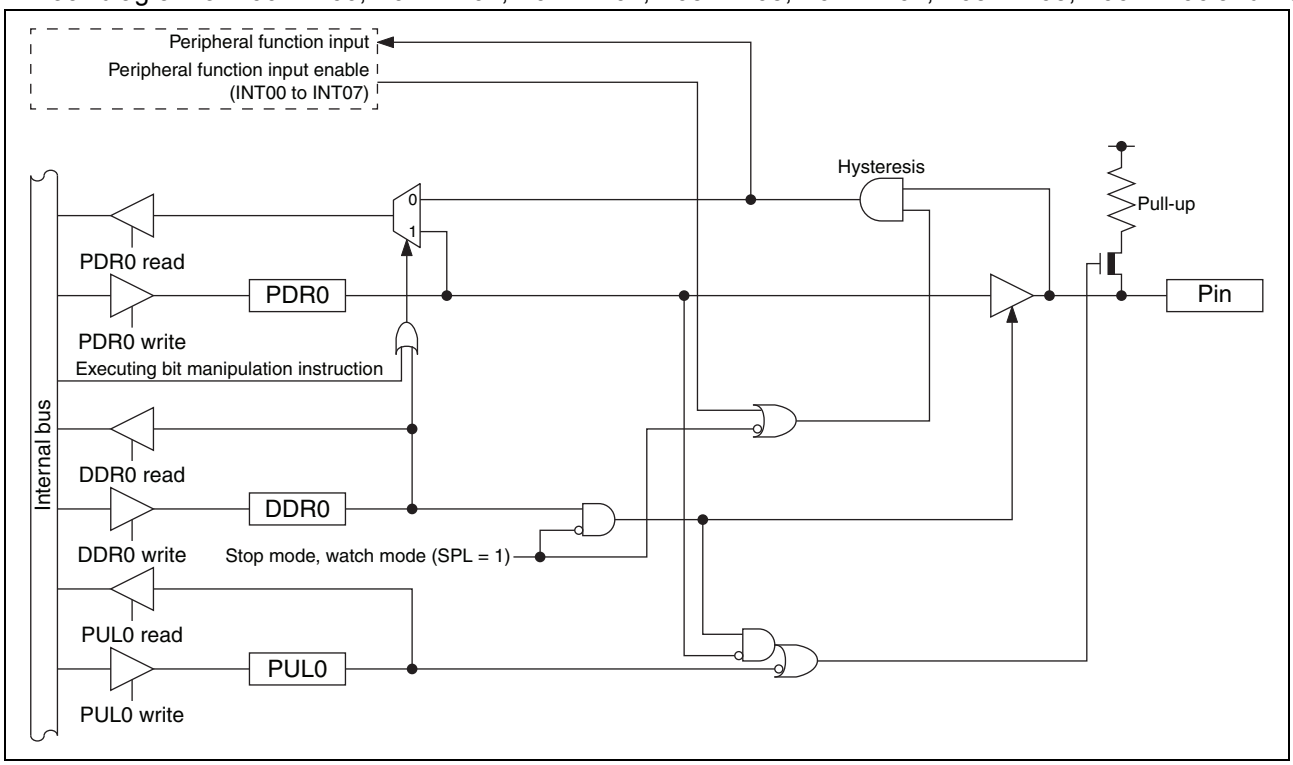
- P05/INT05 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT05)

- P06/INT06 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT06)

- P07/INT07 pin
  This pin has the following peripheral function:

- External interrupt input pin (INT07)

- Block diagram of P00/INT00, P01/INT01, P02/INT02, P03/INT03, P04/INT04, P05/INT05, P06/INT06 and P07/INT07



15.1.3 Port 0 registers

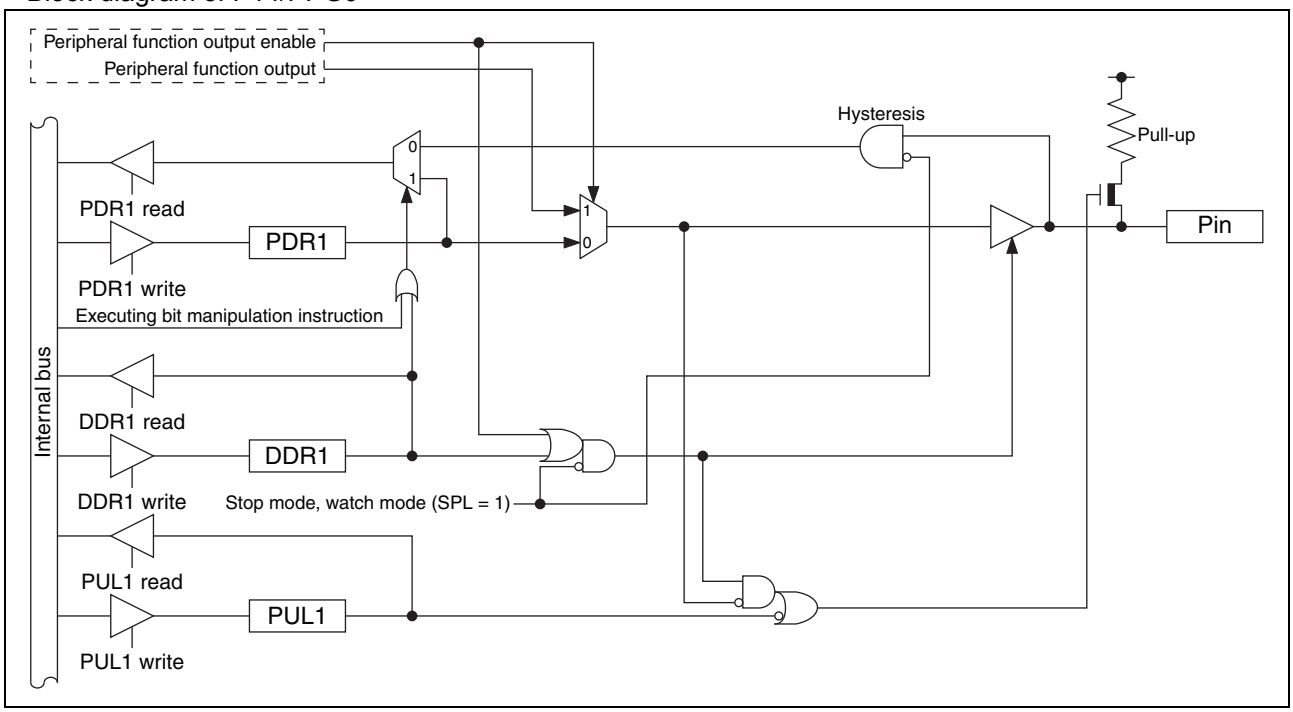
- Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port 0

	Correspondence between related register bits and pins							
Pin name	P07	P06	P05	P04	P03	P02	P01	P00
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
PUL0								

- P14/PPG0 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 0 output pin (PPG0)
- Block diagram of P14/PPG0



15.2.3 Port 1 registers

- Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**P14**	**P13**	**P12**	**P11**	**P10**
PDR1	-	-	-	bit4	bit3	bit2*	bit1	bit0
DDR1								
PUL1								

*: Though P12 has no pull-up function, bit2 in the PUL1 register can still be accessed. The operation of P12 is not affected by the setting of bit2 in the PUL1 register.

15.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

15.3.1 Port 2 configuration

Port 2 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

15.3.2 Block diagrams of port 2

- P20/PPG00 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG00)

- P21/PPG01 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG01)

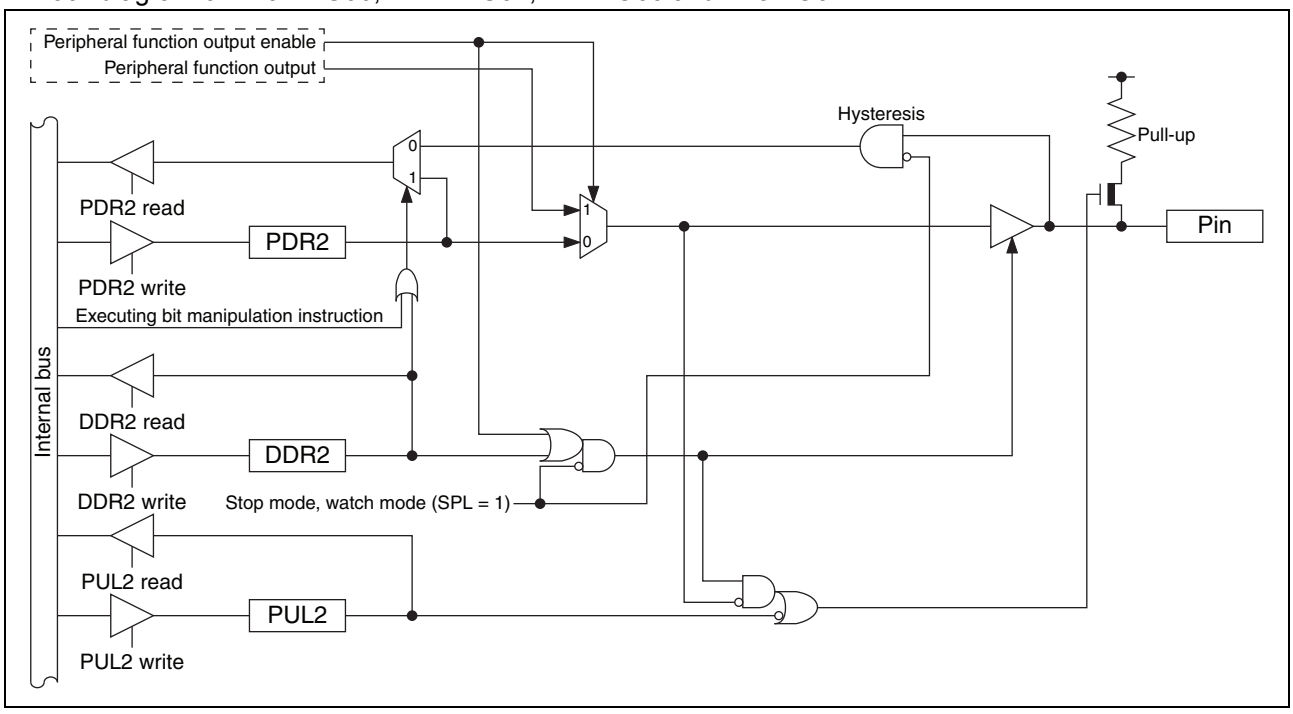
- P22/TO00 pin

  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 output pin (TO00)

- P23/TO01 pin

  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 output pin (TO01)

- Block diagram of P20/PPG00, P21/PPG01, P22/TO00 and P23/TO01



15.3.4 Port 2 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR2 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR2 register to external pins.
  - If data is written to the PDR2 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR2 register returns the PDR2 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR2 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR2 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR2 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR2 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR2 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR2 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR2 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR2 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR2 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P24/EC0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL2 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL2 register.

15.4 Port 3

Port 3 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

15.4.1 Port 3 configuration

Port 3 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 3 data register (PDR3)
- Port 3 direction register (DDR3)
- Port 3 pull-up register (PUL3)
- A/D input disable register (lower) (AIDRL)

15.4.2 Block diagrams of port 3

- P30/AN00/CMP0_N pin

  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN00)
  - Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

- P31/AN01/CMP0_P pin

  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN01)
  - Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

- P33/AN03/CMP1_N pin

  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN03)
  - Comparator ch. 1 inverting analog input (negative input) pin (CMP1_N)

- P34/AN04/CMP1_P pin

  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN04)
  - Comparator ch. 1 non-inverting analog input (positive input) pin (CMP1_P)

15.4.3 Port 3 registers

- Port 3 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR3	0	Pin state is “L” level.	PDR3 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR3 value is “1”.	As output port, outputs “H” level.
DDR3	0	Port input enabled		
	1	Port output enabled		
PUL3	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

- Correspondence between registers and pins for port 3

	Correspondence between related register bits and pins							
Pin name	P37	P36	P35	P34	P33	P32	P31	P30
PDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR3								
PUL3								
AIDRL								

in the AIDRH register to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL4 register to “0”.

- Operation of the pull-up register
  Setting the bit in the PUL4 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL4 register.

15.6 Port 5

Port 5 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

15.6.1 Port 5 configuration

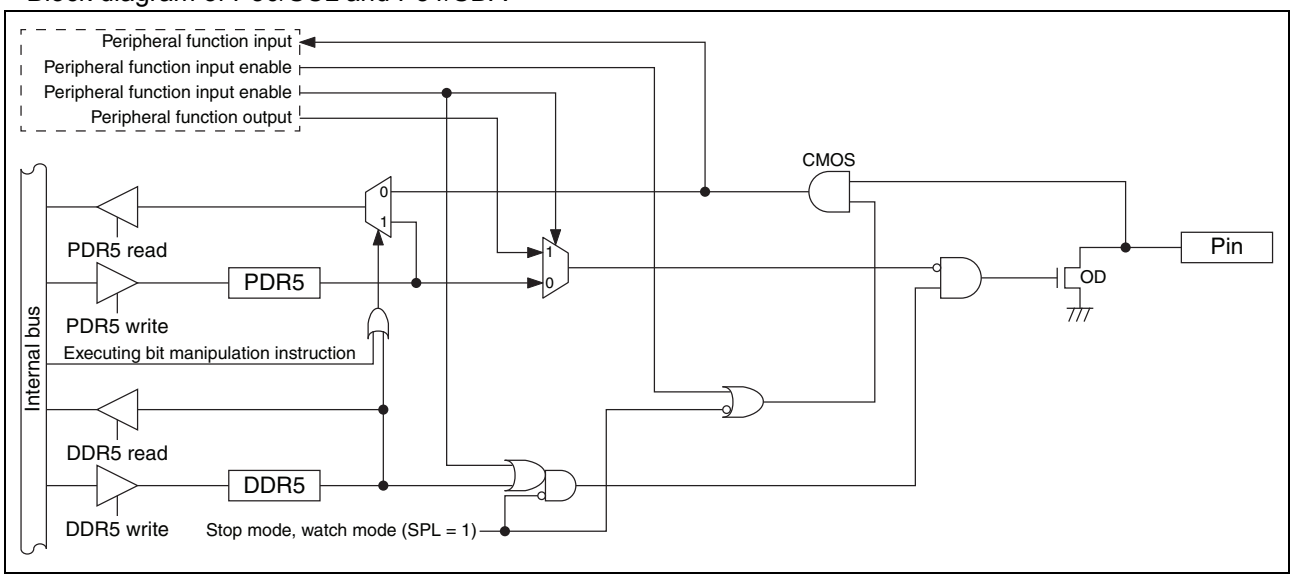
Port 5 is made up of the following elements.
- General-purpose I/O pins/peripheral function I/O pins
- Port 5 data register (PDR5)
- Port 5 direction register (DDR5)
- Port 5 pull-up register (PUL5)

15.6.2 Block diagrams of port 5

- P50/SCL pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 clock I/O pin (SCL)

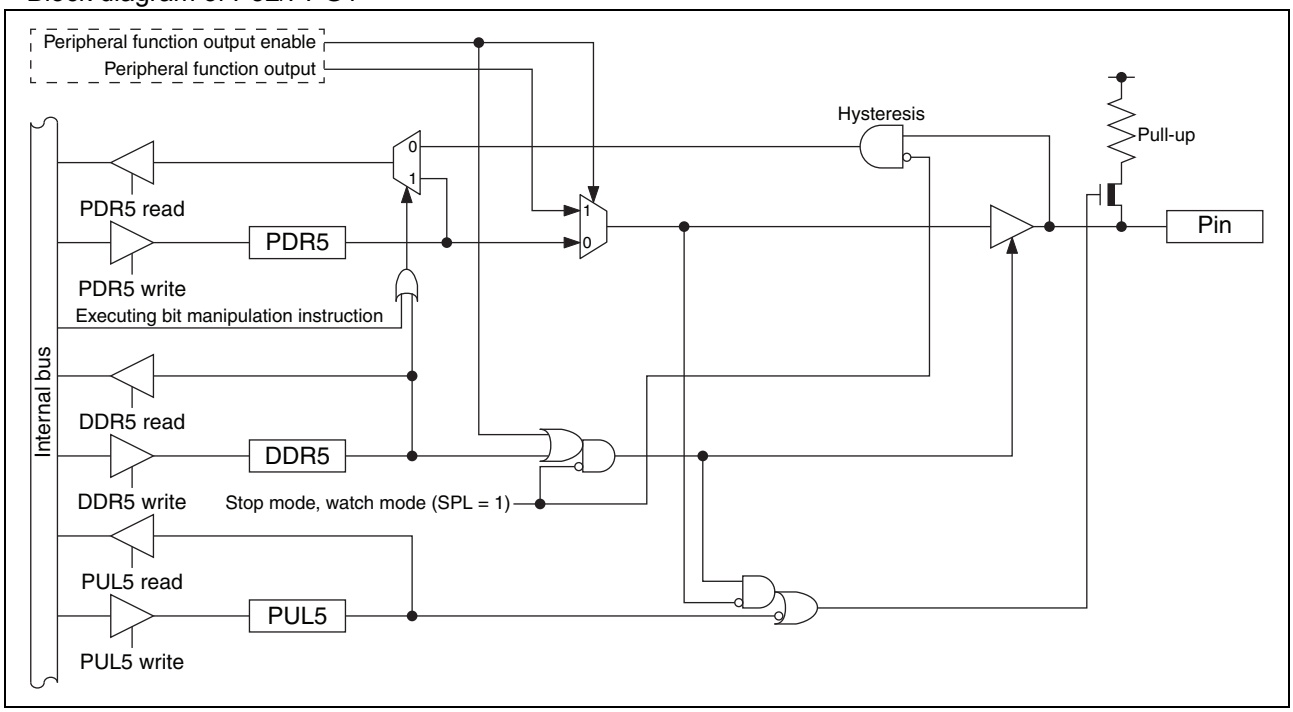
- P51/SDA pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 data I/O pin (SDA)

- Block diagram of P50/SCL and P51/SDA



- P52/PPG1 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 1 output pin (PPG1)

- Block diagram of P52/PPG1



- P53/TRG1 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 1 trigger input pin (TRG1)

15.7.4 Port 6 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
  - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR6 register returns the PDR6 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR6 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR6 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR6 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR6 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P65/SCK and P67/SIN is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

15.9 Port 8

Port 8 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

15.9.1 Port 8 configuration

Port 8 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 8 data register (PDR8)
- Port 8 direction register (DDR8)
- Port 8 pull-up register (PUL8)

15.9.2 Block diagrams of port 8

- P80 pin
- P81 pin
- P82 pin

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR8 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P83/TRG0/ADTG is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL8 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL8 register.

15.10 Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

15.10.1 Port E configuration

Port E is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)
- Port E pull-up register (PULE)

15.10.2 Block diagrams of port E

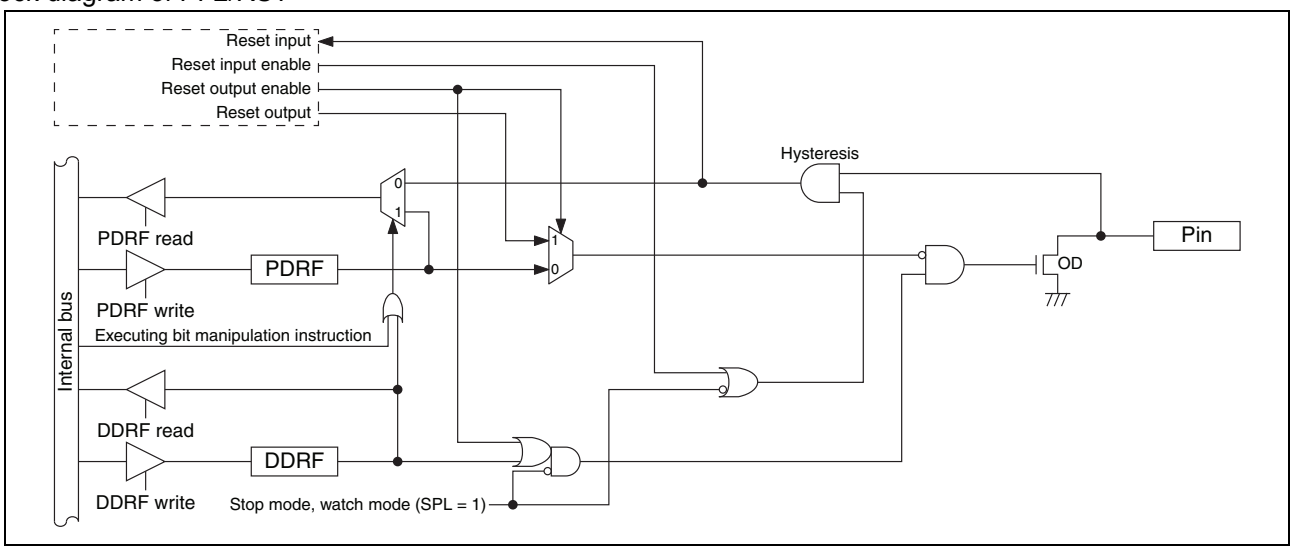
- PE0/INT10 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT10)

- PE1/INT11 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT11)

- PE2/INT12 pin
  This pin has the following peripheral function:
  External interrupt input pin (INT12)

- PE3/INT13 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT13)

- Block diagram of PF2/$\overline{\text{RST}}$



15.11.3 Port F registers

- Port F register functions

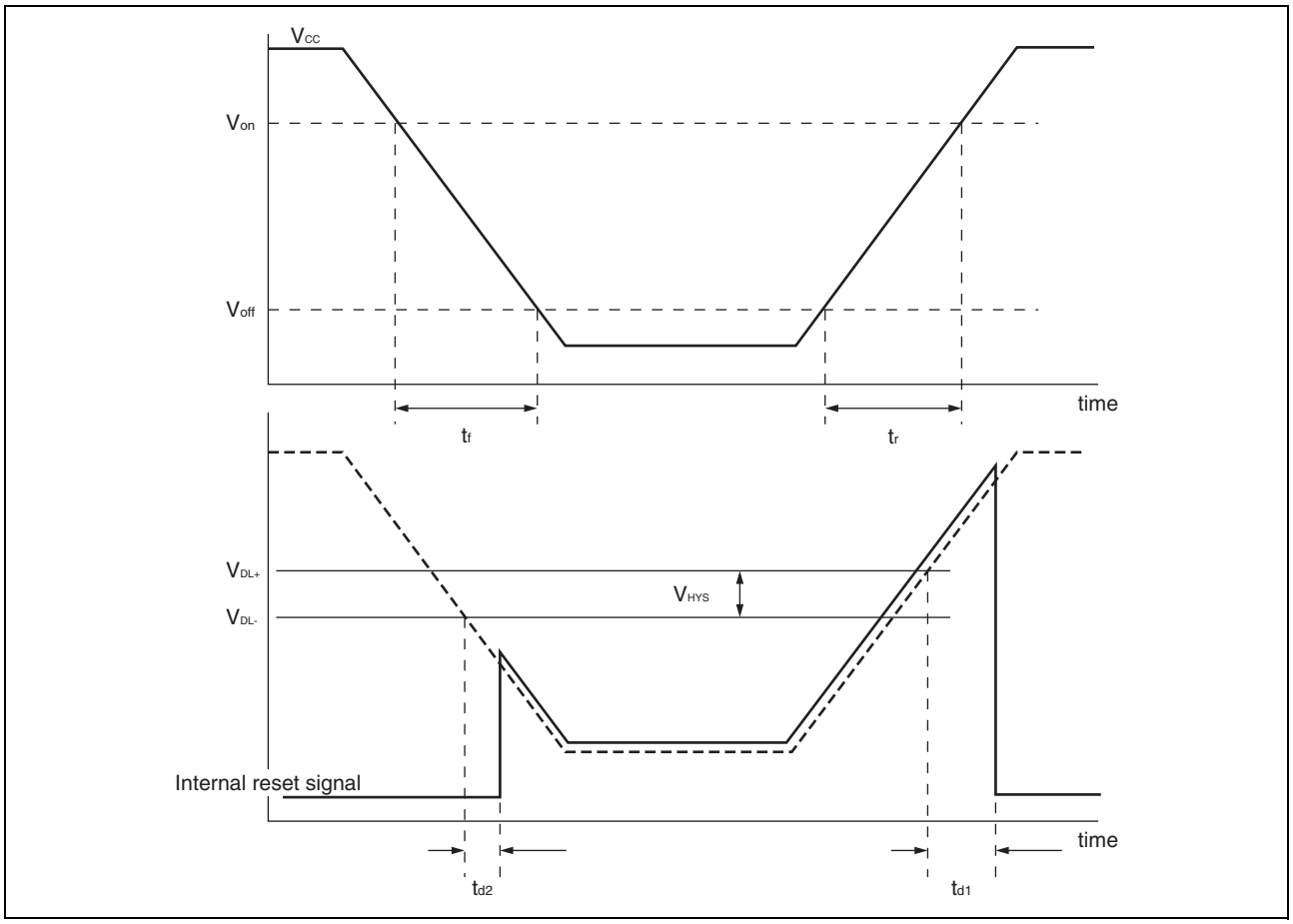
Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

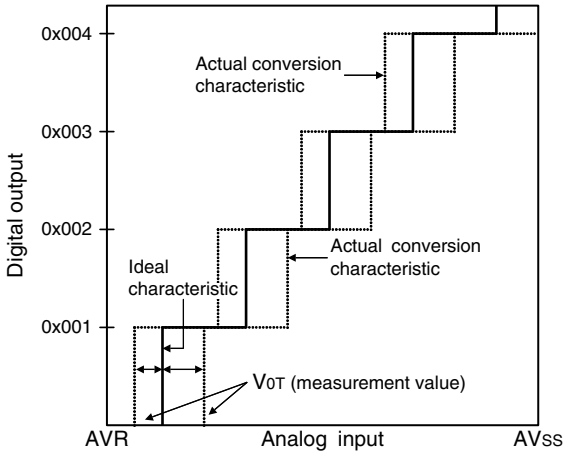
- Correspondence between registers and pins for port F

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PF2**	**PF1**	**PF0**
PDRF	-	-	-	-	-	bit2*	bit1	bit0
DDRF								

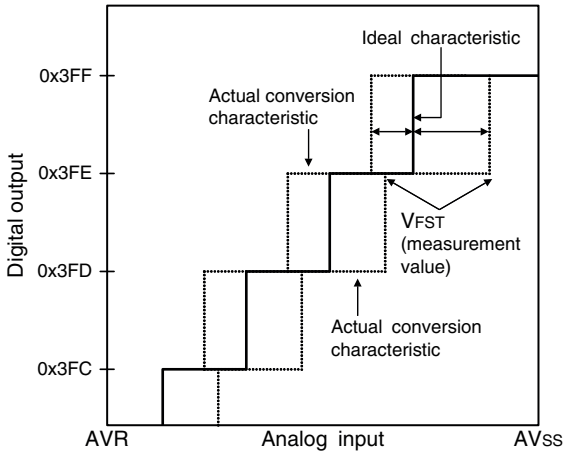
*: When the external reset is selected (SYSC:RSTEN = 1), the port function cannot be used.


Vcc
Von
Voff
time
tf
tr
VDL+
VDL-
VHYS
Internal reset signal
time
td2
td1

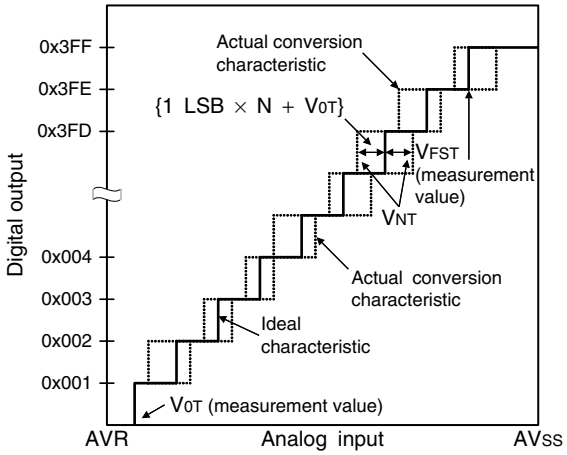
Zero transition error



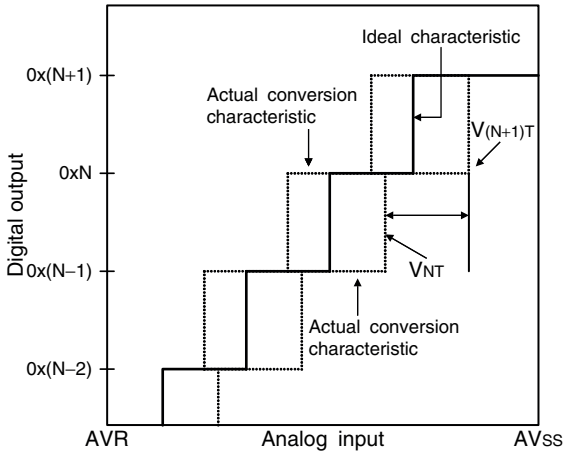
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = AVR + 0.5 LSB [V]

V_{FST} (ideal value) = AV_{SS} – 2 LSB [V]