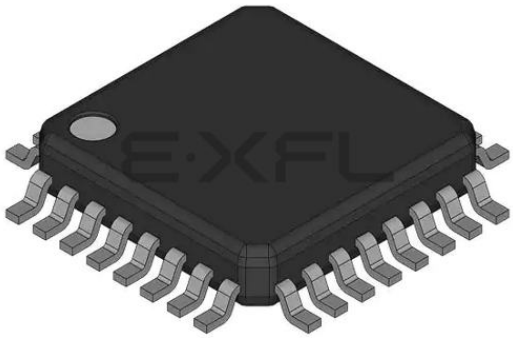

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	6MHz
Connectivity	SCI, USB
Peripherals	LED, LVD, POR, PWM
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908jb16fa

Table of Contents

Section 1. General Description

Section 2. Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001E	IRQ Status and Control Register (INTSCR)	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:						ACK		
		Reset:	0	0	0	0	0	0	0	0
$001F	Configuration Register (CONFIG)†	Read:	LVIDR	LVI5OR3	URSTD	LVID	SSREC	COPRS	STOP	COPD
		Write:								
		Reset:	0*	0*	0*	0*	0	0	0	0

† One-time writable register after each reset.
* LVIDR, LVI5OR3, URSTD, and LVID, are reset by POR or LVI reset only.

$0020	USB Endpoint 0 Data Register 0 (UE0D0)	Read:	UE0R07	UE0R06	UE0R05	UE0R04	UE0R03	UE0R02	UE0R01	UE0R00
		Write:	UE0T07	UE0T06	UE0T05	UE0T04	UE0T03	UE0T02	UE0T01	UE0T00
		Reset:	Unaffected by reset							
$0021	USB Endpoint 0 Data Register 1 (UE0D1)	Read:	UE0R17	UE0R16	UE0R15	UE0R14	UE0R13	UE0R12	UE0R11	UE0R10
		Write:	UE0T17	UE0T16	UE0T15	UE0T14	UE0T13	UE0T12	UE0T11	UE0T10
		Reset:	Unaffected by reset							
$0022	USB Endpoint 0 Data Register 2 (UE0D2)	Read:	UE0R27	UE0R26	UE0R25	UE0R24	UE0R23	UE0R22	UE0R21	UE0R20
		Write:	UE0T27	UE0T26	UE0T25	UE0T24	UE0T23	UE0T22	UE0T21	UE0T20
		Reset:	Unaffected by reset							
$0023	USB Endpoint 0 Data Register 3 (UE0D3)	Read:	UE0R37	UE0R36	UE0R35	UE0R34	UE0R33	UE0R32	UE0R31	UE0R30
		Write:	UE0T37	UE0T36	UE0T35	UE0T34	UE0T33	UE0T32	UE0T31	UE0T30
		Reset:	Unaffected by reset							
$0024	USB Endpoint 0 Data Register 4 (UE0D4)	Read:	UE0R47	UE0R46	UE0R45	UE0R44	UE0R43	UE0R42	UE0R41	UE0R40
		Write:	UE0T47	UE0T46	UE0T45	UE0T44	UE0T43	UE0T42	UE0T41	UE0T40
		Reset:	Unaffected by reset							
$0025	USB Endpoint 0 Data Register 5 (UE0D5)	Read:	UE0R57	UE0R56	UE0R55	UE0R54	UE0R53	UE0R52	UE0R51	UE0R50
		Write:	UE0T57	UE0T56	UE0T55	UE0T54	UE0T53	UE0T52	UE0T51	UE0T50
		Reset:	Unaffected by reset							
$0026	USB Endpoint 0 Data Register 6 (UE0D6)	Read:	UE0R67	UE0R66	UE0R65	UE0R64	UE0R63	UE0R62	UE0R61	UE0R60
		Write:	UE0T67	UE0T66	UE0T65	UE0T64	UE0T63	UE0T62	UE0T61	UE0T60
		Reset:	Unaffected by reset							
$0027	USB Endpoint 0 Data Register 7 (UE0D7)	Read:	UE0R77	UE0R76	UE0R75	UE0R74	UE0R73	UE0R72	UE0R71	UE0R70
		Write:	UE0T77	UE0T76	UE0T75	UE0T74	UE0T73	UE0T72	UE0T71	UE0T70
		Reset:	Unaffected by reset							

U = Unaffected X = Indeterminate = Unimplemented R = Reserved

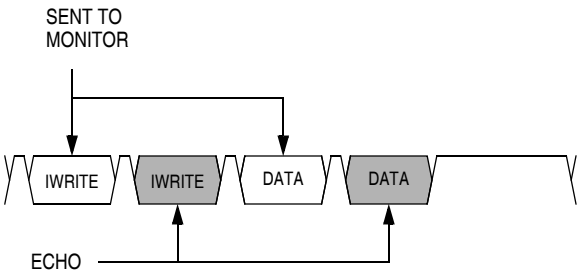
Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 12)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0050	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
$0051	PLL Bandwidth Control Register (PBWC)	Read:	R	LOCK1	R	PLLON1	R	LOCK2	R	PLLON2
		Write:								
		Reset:		0		0		0		0
$0052	VCO Control Register (PVCR)	Read:	VCO_7	VCO_6	VCO_5	VCO_4	VCO_3	VCO_2	VCO_1	VCO_0
		Write:								
		Reset:	0	0	1	1	0	0	0	0
$0053	PLL1 N & R Divider Select Register High (PNRH1)	Read:	VDS1_11	VDS1_10	VDS1_9	VDS1_8	0	0	RDS1_9	RDS1_8
		Write:								
		Reset:	0	0	1	0	0	0	0	0
$0054	PLL1 N Divider Select Register Low (PNSL1)	Read:	VDS1_7	VDS1_6	VDS1_5	VDS1_4	VDS1_3	VDS1_2	VDS1_1	VDS1_0
		Write:								
		Reset:	0	1	1	1	1	1	0	1
$0055	PLL1 R Divider Select Register Low (PRSL1)	Read:	RDS1_7	RDS1_6	RDS1_5	RDS1_4	RDS1_3	RDS1_2	RDS1_1	RDS1_0
		Write:								
		Reset:	1	0	0	1	0	0	0	0
$0056	PLL2 N & R Divider Select Register High (PNRH2)	Read:	VDS2_11	VDS2_10	VDS2_9	VDS2_8	0	0	RDS2_9	RDS2_8
		Write:								
		Reset:	0	0	1	0	0	0	0	0
$0057	PLL2 N Divider Select Register Low (PNSL1)	Read:	VDS2_7	VDS2_6	VDS2_5	VDS2_4	VDS2_3	VDS2_2	VDS2_1	VDS2_0
		Write:								
		Reset:	0	1	1	1	1	1	0	1
$0058	PLL2 R Divider Select Register Low (PRSL2)	Read:	RDS2_7	RDS2_6	RDS2_5	RDS2_4	RDS2_3	RDS2_2	RDS2_1	RDS2_0
		Write:								
		Reset:	1	0	0	1	0	0	0	0
$0059	Phase Detector Control Register (PDCR)	Read:	PHD_7	PHD_6	PHD_5	PHD_4	PHD_3	PHD_2	PHD_1	PHD_0
		Write:								
		Reset:	1	0	0	1	0	0	0	0

U = Unaffected X = Indeterminate = Unimplemented R = Reserved

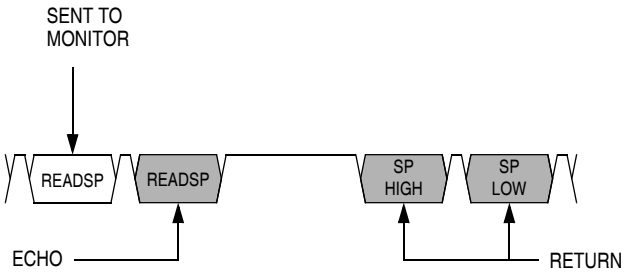
Figure 2-2. Control, Status, and Data Registers (Sheet 9 of 12)

Table 9-7. IWRITE (Indexed Write) Command

Description	Write to last address accessed + 1
Operand	Specifies single data byte
Data Returned	None
Opcode	$19
Command Sequence	

NOTE: *A sequence of IREAD or IWRITE commands can sequentially access a block of memory over the full 64k-byte memory map.*

Table 9-8. READSP (Read Stack Pointer) Command

Description	Reads stack pointer
Operand	None
Data Returned	Returns stack pointer in high byte:low byte order
Opcode	$0C
Command Sequence	

10.10 I/O Registers

NOTE: *References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TSC may generically refer to both T1SC and T2SC.*

These I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM counter registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0, TSC1)
- TIM channel registers (TCH0H:TCH0L, TCH1H:TCH1L)

10.10.1 TIM Status and Control Register

The TIM status and control register (TSC):

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: T1SC, $000A and T2SC, $0040

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 10-4. TIM Status and Control Register (TSC)

11.5.4 Resume After Suspend

The MCU can be activated from the suspend state by normal bus activity, a USB reset signal, or by a forced resume driven from the MCU.

11.5.4.1 Host Initiated Resume

The host signals resume by initiating resume signalling (K state) for at least 20ms followed by a standard low-speed EOP signal. This 20ms ensures that all devices in the USB network are awakened.

After resuming the bus, the host must begin sending bus traffic within 3ms to prevent the device from re-entering suspend mode.

11.5.4.2 USB Reset Signalling

Reset can wake a device from the suspended mode.

11.5.4.3 Remote Wakeup

The MCU also supports the remote wakeup feature. The firmware has the ability to exit suspend mode by signaling a resume state to the upstream host or hub. A non-idle state (K state) on the USB data lines is accomplished by asserting the FRESUM bit in the UCR1 register.

When using the remote wakeup capability, the firmware must wait for at least 5ms after the bus is in the idle state before sending the remote wakeup resume signaling. This allows the upstream devices to get into their suspend state and prepare for propagating resume signaling. The FRESUM bit should be asserted to cause the resume state on the USB data lines for at least 10ms, but not more than 15ms. Note that the resume signalling is controlled by the FRESUM bit and meeting the timing specifications is dependent on the firmware. When FRESUM is cleared by firmware, the data lines will return to their high-impedance state.

Refer to register definitions (see **11.8.6 USB Control Register 1**) for more information about how the force resume (FRESUM) bit can be used to initiate the remote wakeup feature.

11.8.8 USB Control Register 3

Address: $001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TX1ST	0	OSTALL0	ISTALL0	0	PULLEN	ENABLE2	ENABLE1
Write:		TX1STR						
Reset:	0	0	0	0	0	0*	0	0

= Unimplemented

* PULLEN bit is reset by POR or LVI reset only.

Figure 11-22. USB Control Register 3 (UCR3)

TX1ST — Endpoint 0 Transmit First Flag

This read-only bit is set if the endpoint 0 data transmit flag (TXD0F) is set when the USB control logic is setting the endpoint 0 data receive flag (RXD0F). In other words, if an unserviced endpoint 0 transmit flag is still set at the end of an endpoint 0 reception, then this bit will be set. This bit lets the firmware know that the endpoint 0 transmission happened before the endpoint 0 reception.

Reset clears this bit.

1 = IN transaction occurred before SETUP/OUT
0 = IN transaction occurred after SETUP/OUT

TX1STR — Clear Endpoint 0 Transmit First Flag

Writing a logic 1 to this write-only bit will clear the TX1ST bit if it is set. Writing a logic 0 to the TX1STR has no effect. Reset clears this bit.

OSTALL0 — Endpoint 0 Force STALL Bit for OUT token

This read/write bit causes endpoint 0 to return a STALL handshake when polled by an OUT token by the USB host controller. The USB hardware clears this bit when a SETUP token is received. Reset clears this bit.

1 = Send STALL handshake
0 = Default

11.9.1.3 Transmit Endpoint 1

For an IN transaction directed at endpoint 1, the USB module will generate an interrupt by setting the TXD1F in the UIR1 register. The conditions necessary for the interrupt to occur are shown in **Figure 11-32**.

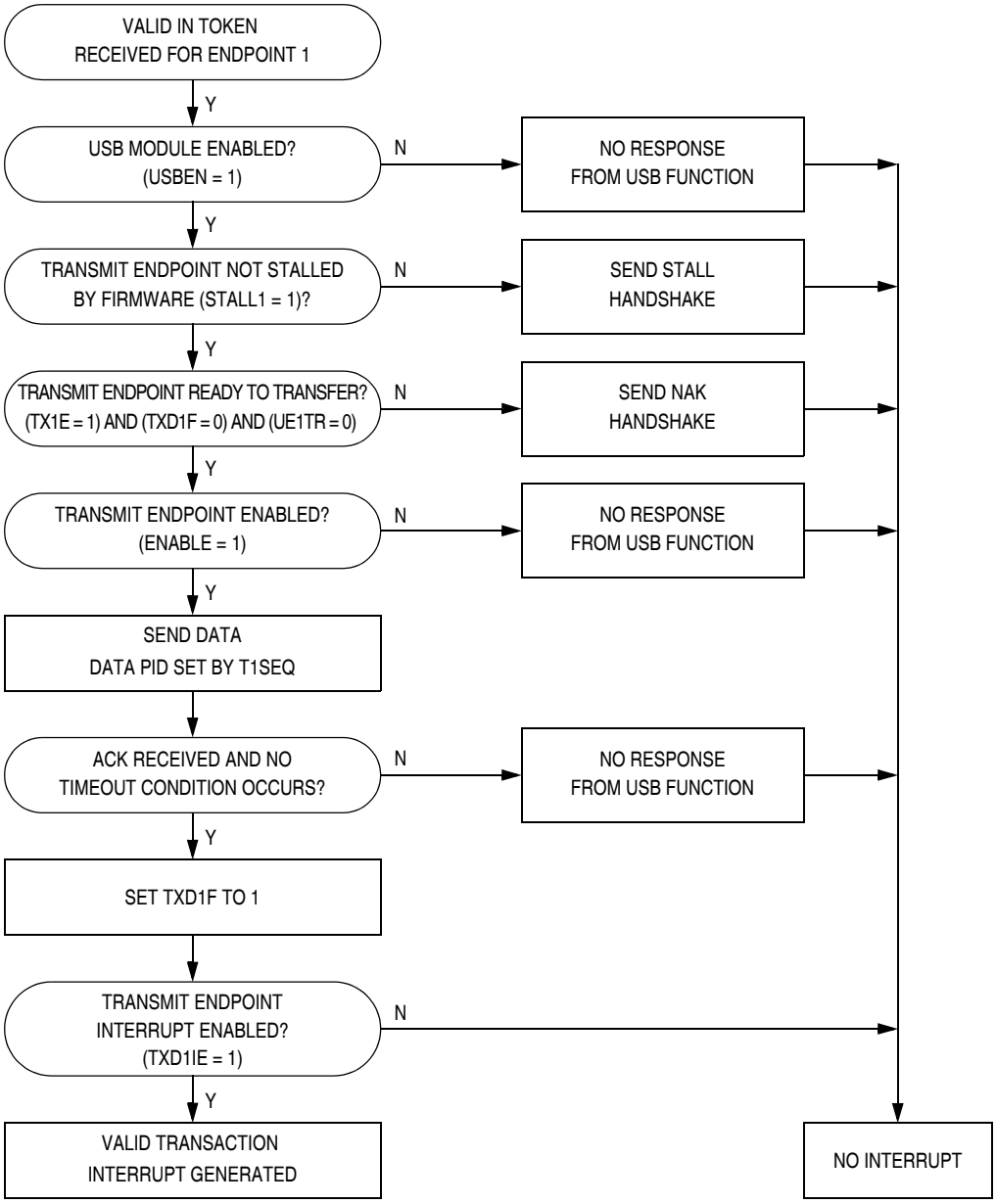


Figure 11-32. IN Token Data Flow for Transmit Endpoint 1

Address: $005A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	ENSCI	TXINV	M	WAKE	ILTY	PEN	PTY
Reset:	0	0	0	0	0	0	0	0

Figure 12-9. SCI Control Register 1 (SCC1)

LOOPS — Loop Mode Select Bit

This read/write bit enables loop mode operation. In loop mode the RxD pin is disconnected from the SCI, and the transmitter output goes into the receiver input. Both the transmitter and the receiver must be enabled to use loop mode. Reset clears the LOOPS bit.

1 = Loop mode enabled
0 = Normal operation enabled

ENSCI — Enable SCI Bit

This read/write bit enables the SCI and the SCI baud rate generator. Clearing ENSCI sets the SCTE and TC bits in SCI status register 1 and disables transmitter interrupts. Reset clears the ENSCI bit.

1 = SCI enabled
0 = SCI disabled

TXINV — Transmit Inversion Bit

This read/write bit reverses the polarity of transmitted data. Reset clears the TXINV bit.

1 = Transmitter output inverted
0 = Transmitter output not inverted

NOTE: *Setting the TXINV bit inverts all transmitted values, including idle, break, start, and stop bits.*

12.9.6 SCI Data Register

The SCI data register (SCDR) is the buffer between the internal data bus and the receive and transmit shift registers.

Address: $005F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	Unaffected by reset							

Figure 12-15. SCI Data Register (SCDR)

R7/T7–R0/T0 — Receive/Transmit Data Bits

Reading the SCI data register accesses the read-only received data bits, R7:R0. Writing to the SCI data register writes the data to be transmitted, T7:T0. Reset has no effect on the SCI data register.

NOTE: *Do not use read/modify/write instructions on the SCI data register.*

13.6 CGMOUT External Connections

The output of CGM clock is a standard CMOS output with push-pull configuration. The output logic high and low levels are specified with corresponding DC loading current (see **20.13 CGM Electrical Characteristics**). The transient current is mainly determined by the maximum loading capacitor value.

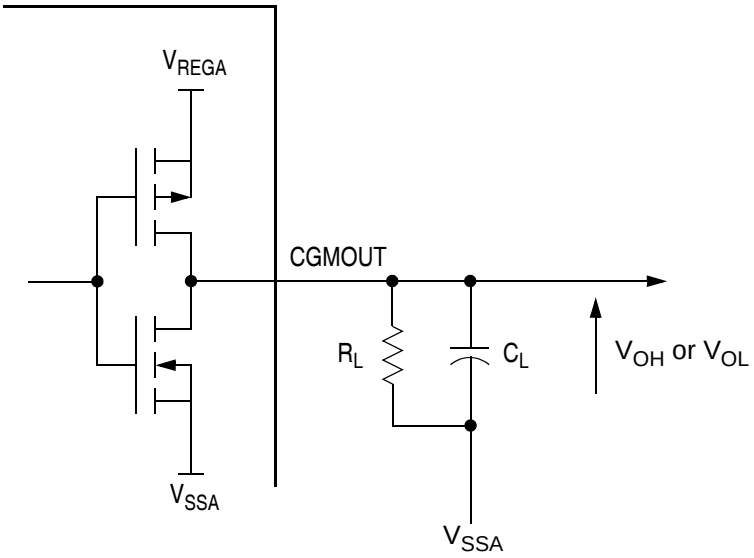


Figure 13-5. CGMOUT External Connections

13.7 Calculation of VCO Frequency

The relationship between the VCO frequency, f_{VCLK}, and the crystal reference frequency, f_{XCLK}, is:

$$f_{VCLK} = \frac{N}{R} \times f_{XCLK}$$

13.9.6 Phase Detector Control Register (PDCR)

The phase detector control register configures the phase detector for both PLLs.

Address: $0059

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PHD_7	PHD_6	PHD_5	PHD_4	PHD_3	PHD_2	PHD_1	PHD_0
Reset:	1	0	0	1	0	0	0	0

Figure 13-14. Phase Detector Control Register (PDCR)

PHD_[7:0] — Phase detector Control Bits for both PLLs

Set PHD_[7:0] = $70 for maximum performance.

13.10 Pre-Defined VCO Output Frequency Settings

The exact frequency values for the following required channels cannot be synthesized by using a reference frequency higher than 10kHz. An absolute offset frequency from +1.66kHz to +1.89kHz will be introduced for different channels and the maximum relative offset is only ±115Hz with 1.775kHz as the center point (see **Table 13-1 . Predefined Programming Setting for PLL**). The absolute offset frequency can be further minimized by reducing the crystal frequency by 60 ppm (360Hz) in actual application.

Table 13-1. Predefined Programming Setting for PLL

Channel Frequency (MHz)	Crystal Frequency (MHz)	Divider R	Reference Frequency (kHz)	Divider N	VCO Frequency (MHz)	Absolute Offset (kHz)
26.54	12	288	41.67	637	26.54166	+1.66
26.59	12	338	35.50	749	26.59171	+1.71
26.64	12	268	44.78	595	26.64179	+1.79
26.69	12	370	32.43	823	26.69189	+1.89
26.74	12	302	39.74	673	26.74172	+1.72

14.6 Port E

Port E is a 5-bit special function port that shares three of its pins with the timer interface modules (TIMs) and two of its pins with the USB data pins D+ and D–. PTE4 and PTE3 are open-drain when configured as output.

14.6.1 Port E Data Register

The port E data register contains a data latch for each of the five port E pins.

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	PTE4	PTE3	PTE2	PTE1	PTE0
Write:								
Reset:	Unaffected by reset							
Alternative Function:				D–	D+	T2CH01	T1CH01	TCLK
Additional Function:				Optional pullup	Optional pullup	Optional pullup	Optional pullup	Optional pullup
Additional Function:				External interrupt				
				Open-drain	Open-drain			

= Unimplemented

Figure 14-11. Port E Data Register (PTE)

PTE[4:0] — Port E Data Bits

PTE[4:0] are read/write, software-programmable bits. Data direction of each port E pin is under the control of the corresponding bit in data direction register E.

The PTE4 and PTE3 pullup enable bits, PTE4P and PTE3P, in the port option control register (POCR) enable 5kΩ pullups on PTE4 and PTE3 if the respective pin is configured as an input and the USB module is disabled. (See **14.7 Port Options**.)

15.8 IRQ Status and Control Register

The IRQ status and control register (ISCR) controls and monitors operation of the IRQ module. The ISCR has the following functions:

- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks IRQ interrupt request
- Controls triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

Address: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF	0	IMASK	MODE
Write:						ACK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-3. IRQ Status and Control Register (ISCR)

IRQF — IRQ Flag

This read-only status bit is high when the IRQ interrupt is pending.
1 = IRQ interrupt pending
0 = IRQ interrupt not pending

ACK — IRQ Interrupt Request Acknowledge Bit

Writing a logic 1 to this write-only bit clears the IRQ latch. ACK always reads as logic 0. Reset clears ACK.

IMASK — IRQ Interrupt Mask Bit

Writing a logic 1 to this read/write bit disables IRQ interrupt requests. Reset clears IMASK.
1 = IRQ interrupt requests disabled
0 = IRQ interrupt requests enabled

MODE — IRQ Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin. Reset clears MODE.
1 = $\overline{\text{IRQ}}$ pin interrupt requests on falling edges and low levels
0 = $\overline{\text{IRQ}}$ pin interrupt requests on falling edges only

16.7.2 Keyboard Interrupt Enable Register

The keyboard interrupt enable register enables or disables each port A pin to operate as a keyboard interrupt pin.

Address: $0017

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	KBIE7	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Reset:	0	0	0	0	0	0	0	0

Figure 16-4. Keyboard Interrupt Enable Register (KBIER)

KBIE7–KBIE0 — Keyboard Interrupt Enable Bits

Each of these read/write bits enables the corresponding keyboard interrupt pin to latch interrupt requests. Reset clears the keyboard interrupt enable register.

1 = PTAx/KBAx pin enabled as keyboard interrupt pin
0 = PTAx/KBAx not enabled as keyboard interrupt pin

16.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

16.8.1 Wait Mode

The keyboard module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

16.8.2 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

17.5 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clears COP counter (any value)							
Reset:	Unaffected by reset							

Figure 17-3. COP Control Register (COPCTL)

17.6 Interrupts

The COP does not generate CPU interrupt requests.

17.7 Monitor Mode

When monitor mode is entered with V_{TST} on the $\overline{IRQ}$ pin, the COP is disabled as long as V_{TST} remains on the $\overline{IRQ}$ pin or the $\overline{RST}$ pin. When monitor mode is entered by having blank reset vectors and not having V_{TST} on the $\overline{IRQ}$ pin, the COP is automatically disabled until a POR occurs.

17.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

Section 18. Low-Voltage Inhibit (LVI)

18.1 Contents

18.2 Introduction

This section describes the low-voltage inhibit (LVI) module, which monitors the voltage on the V_{DD} pin and V_{REG} pin. and can force a reset when the V_{DD} or V_{REG} voltage falls below the LVI trip falling voltage.

18.3 Features

Features of the LVI module include:

- Independent voltage monitoring circuits for V_{DD} and V_{REG}
- Independent LVI circuit disable for V_{DD} and V_{REG}
- Selectable LVI trip voltage for V_{DD}

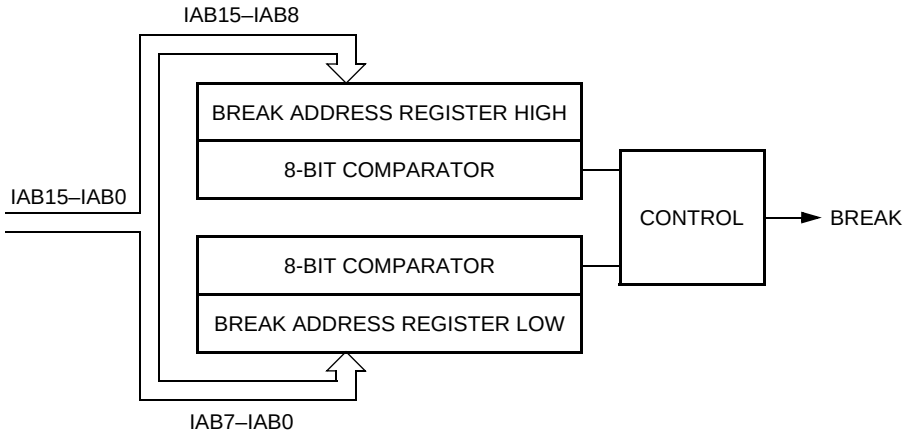


Figure 19-1. Break Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE00	SIM Break Status Register (SBSR)	Read:	R	R	R	R	R	R	SBSW	R
		Write:							Note	
		Reset:							0	
$FE03	SIM Break Flag Control Register (SBFCR)	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
$FE0C	Break Address Register High (BRKH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Register Low (BRKL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BRKSCR)	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

Note: Writing a logic 0 clears SBSW.

= Unimplemented R = Reserved

Figure 19-2. Break Module I/O Register Summary

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a logic 1 to BRKA generates a break interrupt. Clear BRKA by writing a logic 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = (When read) Break address match

0 = (When read) No break address match

19.6.2 Break Address Registers

The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

Address: $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	0	0	0	0	0	0	0	0

Figure 19-4. Break Address Register High (BRKH)

Address: $FE0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 19-5. Break Address Register Low (BRKL)

19.6.3 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from wait mode. The flag is useful in applications requiring a return to wait mode after exiting from a break interrupt.

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