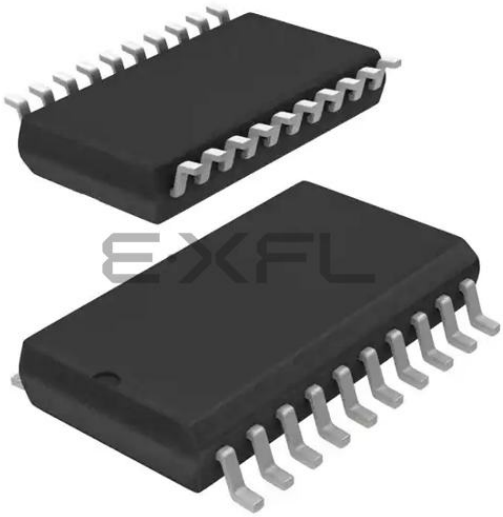

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	6MHz
Connectivity	SCI, USB
Peripherals	LED, LVD, POR, PWM
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jb16jdw

Section 13. Clock Generator Module (CGM)

Section 20. Electrical Specifications

The SIM disables the oscillator signals (OSCOUT and OSCDCLK) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register (CONFIG). If SSREC is set, stop recovery is reduced from the normal delay of 4096 OSCDCLK cycles down to 2048. This is ideal for applications using canned oscillators that do not require long startup times from stop mode.

NOTE: *External crystal applications should use the full stop recovery time by clearing the SSREC bit.*

A break interrupt during stop mode sets the SIM break stop/wait bit (SBSW) in the SIM break status register (SBSR).

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. **Figure 8-17** shows stop mode entry timing.

NOTE: *To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.*

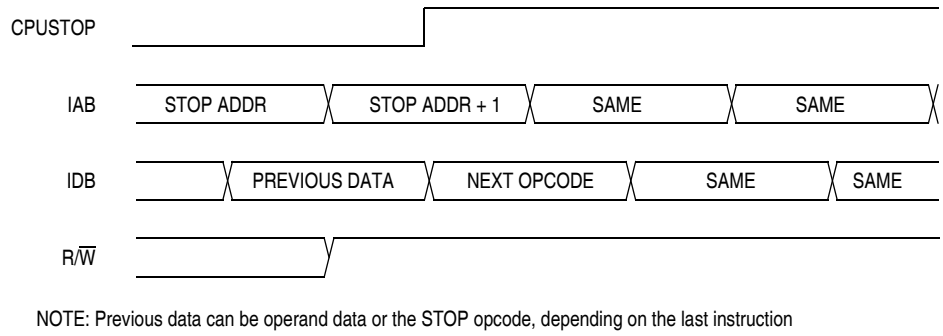


Figure 8-17. Stop Mode Entry Timing

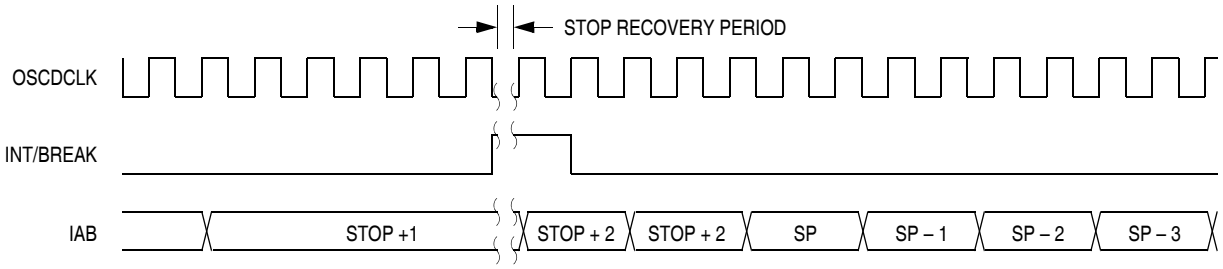


Figure 8-18. Stop Mode Recovery from Interrupt or Break

Section 9. Monitor ROM (MON)

9.1 Contents

9.2 Introduction

This section describes the monitor ROM (MON) and the monitor mode entry methods. The monitor ROM allows complete testing of the MCU through a single-wire interface with host computer. This mode is also used for programming and erasing of FLASH memory in the MCU. Monitor mode entry can be achieved without use of the higher voltage, V_{TST}, as long as vector addresses $FFFE and $FFFF are blank, thus reducing the hardware requirements for in-circuit programming.

9.4.1 Entering Monitor Mode

Table 9-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a POR and will allow communication at 19200 baud provided one of the following sets of conditions is met:

1. If $\overline{IRQ}$ = V_{TST}:
   - External clock on OSC1 is 12 MHz
   - PTA3 = high
   - PTE3 = high
2. If $FFFE & $FFFF is blank (contains $FF):
   - External clock on OSC1 is 12 MHz
   - $\overline{IRQ}$ = V_{DD}
   - PTE3 = high

Table 9-1. Mode Entry Requirements and Options

$\overline{IRQ}$	$FFFE and $FFFF	PTE3	PTA3[1]	PTA2	PTA1	PTA0	External Clock, f_{XCLK}	Bus Frequency, f_{BUS}	Comments
V_{TST}[2]	X	1	0	0	1	1	12 MHz	12 MHz (f_{XCLK})	High-voltage entry to monitor mode. 38400 baud communication on PTA0. COP disabled.
V_{TST}[2]	X	1	1	0	1	1	12 MHz	6 MHz (f_{XCLK} ÷ 2)	High-voltage entry to monitor mode. 19200 baud communication on PTA0. COP disabled.
V_{DD}	BLANK (contain $FF)	1	X	X	X	1	12 MHz	6 MHz (f_{XCLK} ÷ 2)	Low-voltage entry to monitor mode. 19200 baud communication on PTA0. COP disabled.
V_{DD}	NOT BLANK	1	X	X	X	X	12 MHz	6 MHz (f_{XCLK} ÷ 2)	Enters user mode. If $FFFE and $FFFF is blank, MCU will encounter an illegal address reset.

Factory use only

Notes:
1. PTA3 = 0: Bypasses the divide-by-two prescaler to SIM when using V_{TST} for monitor mode entry.
2. See **Section 20. Electrical Specifications** for V_{TST} voltage level requirements.

Section 10. Timer Interface Module (TIM)

10.1 Contents

10.4 Pin Name Conventions

The text that follows describes both timers, TIM1 and TIM2. The TIM input/output (I/O) pin names are T[1,2]CH01 (timer channel 01), where “1” is used to indicate TIM1 and “2” is used to indicate TIM2. The two TIMs share two I/O pins with two I/O port pins. The full names of the TIM I/O pins are listed in **Table 10-1**. The generic pin names appear in the text that follows.

Table 10-1. Pin Name Conventions

TIM Generic Pin Names:		T[1,2]CH01	TCLK
Full TIM Pin Names:	TIM1	PTE1/T1CH01	PTE0/TCLK
	TIM2	PTE2/T2CH01	

NOTE: *References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TCH01 may refer generically to T1CH01 and T2CH01.*

10.5 Functional Description

Figure 10-1 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

Channel 0 and channel 1 I/Os are connected together, forming a common I/O. Although the two TIM channels are programmable independently as input capture channels, the input capture signal will be the same for both channels. Output compare functions should only be enabled for one channel to avoid I/O contention.

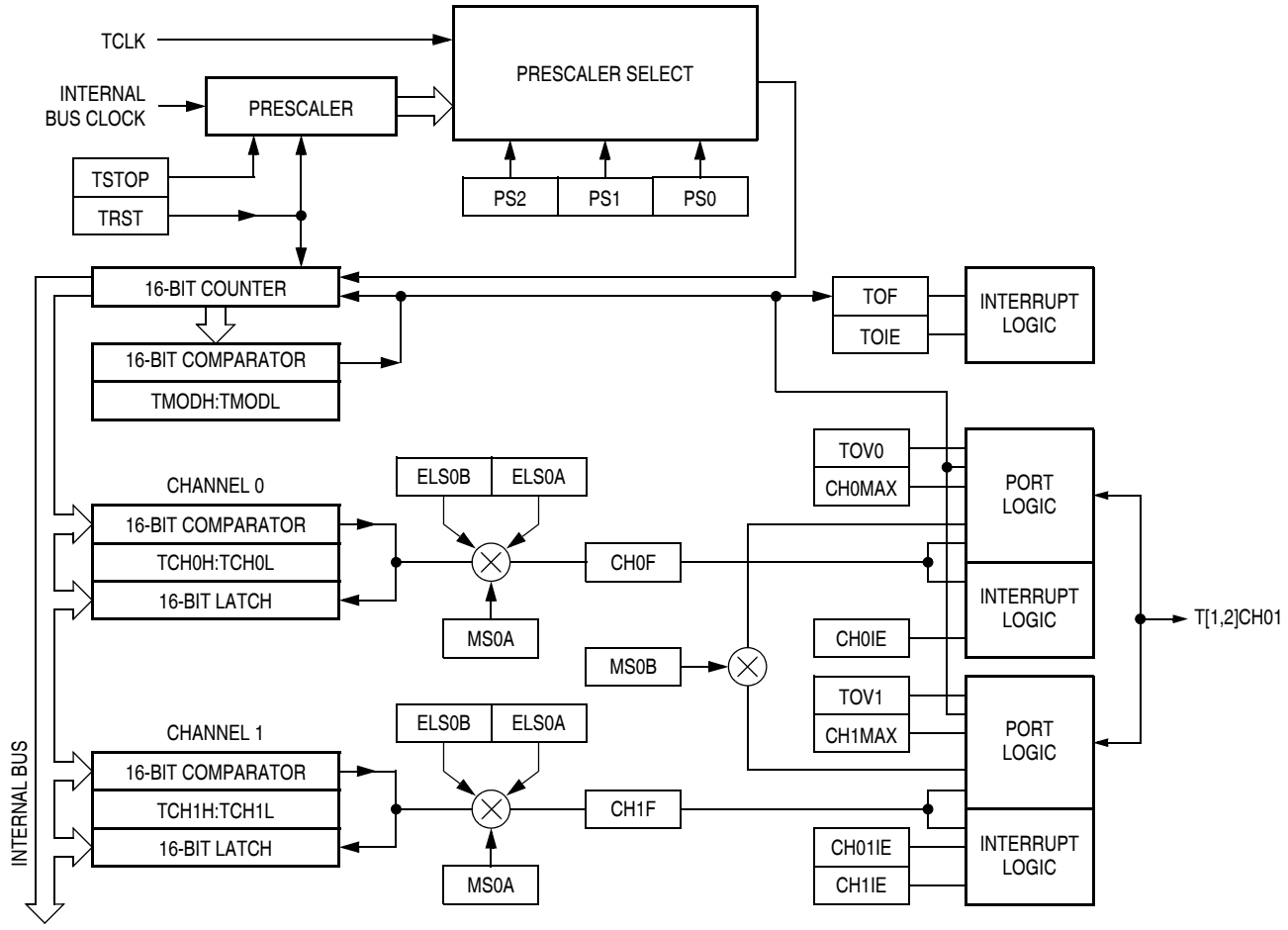


Figure 10-1. TIM Block Diagram

Figure 10-2 summarizes the timer registers.

NOTE: *References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TSC may generically refer to both T1SC and T2SC.*

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing $00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is $000. See **10.10.1 TIM Status and Control Register**.

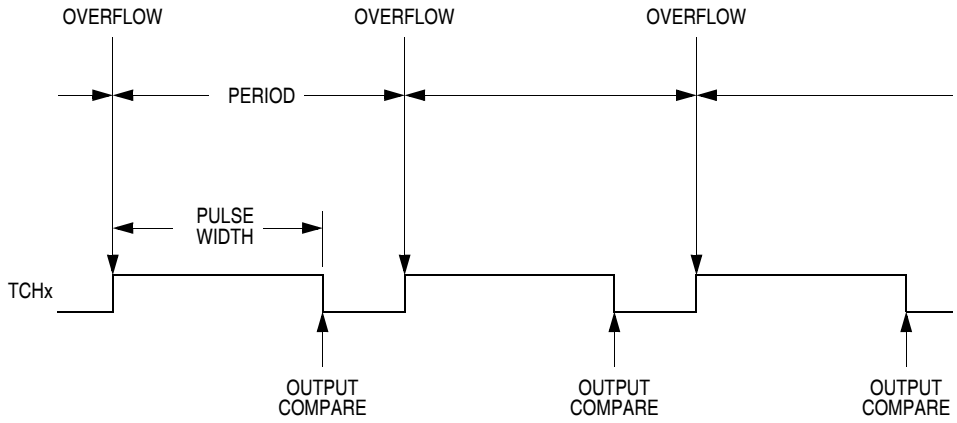


Figure 10-3. PWM Period and Pulse Width

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing $0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.

10.5.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in **10.5.4 Pulse Width Modulation (PWM)**. The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM may pass the new value before it is written.

Section 11. Universal Serial Bus Module (USB)

11.1 Contents

11.5.1 USB Protocol

Figure 11-3 shows the various transaction types supported by the USB module. The transactions are portrayed as error free. The effect of errors in the data flow are discussed later.

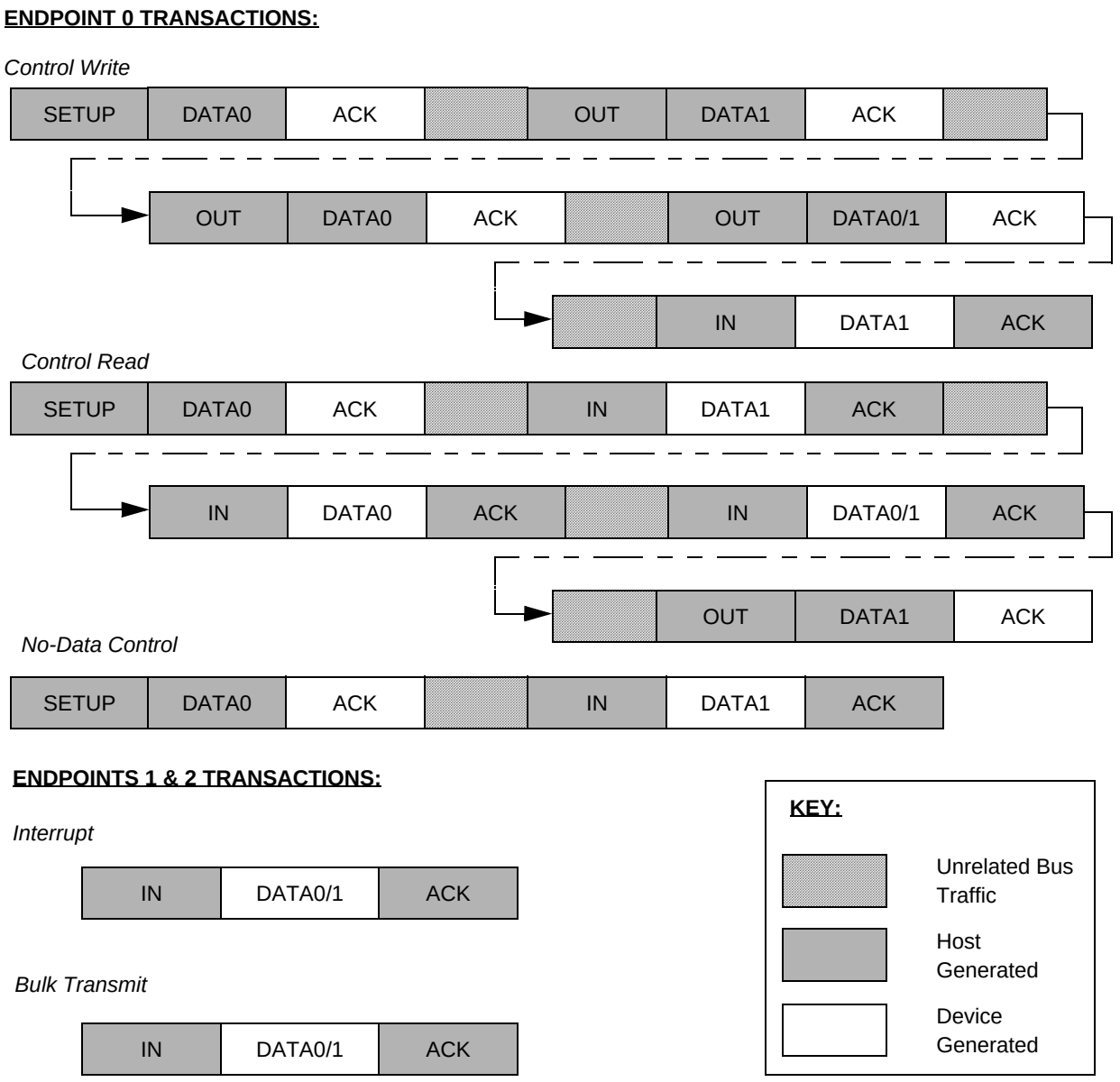


Figure 11-3. Supported Transaction Types Per Endpoint

11.8.12 USB Endpoint 0 Data Registers

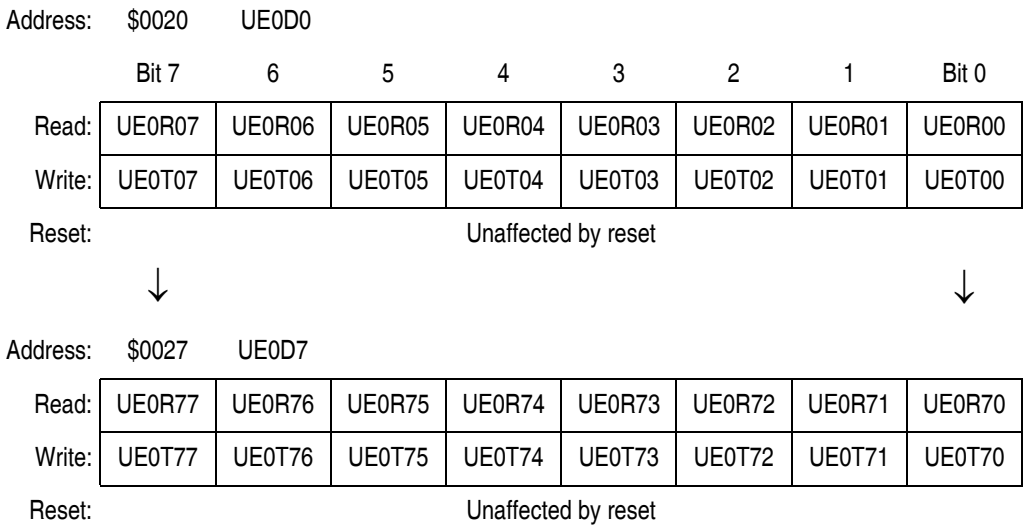


Figure 11-26. USB Endpoint 0 Data Registers (UE0D0–UE0D7)

UE0Rx7–UE0Rx0 — Endpoint 0 Receive Data Buffer

These read-only bits are serially loaded with OUT token or SETUP token data directed at endpoint 0. The data is received over the USB's D+ and D– pins.

UE0Tx7–UE0Tx0 — Endpoint 0 Transmit Data Buffer

These write-only buffers are loaded by software with data to be sent on the USB bus on the next IN token directed at endpoint 0.

11.9 USB Interrupts

The USB module is capable of generating interrupts and causing the CPU to execute the USB interrupt service routine. There are three types of USB interrupts:

- End-of-transaction interrupts signify either a completed transaction receive or transmit transaction.
- Resume interrupts signify that the USB bus is reactivated after having been suspended.
- End-of-packet interrupts signify that a low-speed end-of-packet signal was detected.

All USB interrupts share the same interrupt vector. Firmware is responsible for determining which interrupt is active.

11.9.1 USB End-of-Transaction Interrupt

There are five possible end-of-transaction interrupts:

- Endpoint 0 or 2 receive
- Endpoint 0, 1 or 2 transmit

End-of-transaction interrupts occur as detailed in the following sections.

- Framing error (FE) — The FE bit in SCS1 is set when a logic 0 occurs where the receiver expects a stop bit. The framing error interrupt enable bit, FEIE, in SCC3 enables FE to generate SCI error CPU interrupt requests.
- Parity error (PE) — The PE bit in SCS1 is set when the SCI detects a parity error in incoming data. The parity error interrupt enable bit, PEIE, in SCC3 enables PE to generate SCI error CPU interrupt requests.

12.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

12.6.1 Wait Mode

The SCI module remains active after the execution of a WAIT instruction. In wait mode, the SCI module registers are not accessible by the CPU. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

Refer to **8.7 Low-Power Modes** for information on exiting wait mode.

12.6.2 Stop Mode

The SCI module is inactive after the execution of a STOP instruction. The STOP instruction does not affect SCI register states. SCI module operation resumes after an external interrupt.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

Refer to **8.7 Low-Power Modes** for information on exiting stop mode.

Address: $005A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	ENSCI	TXINV	M	WAKE	ILTY	PEN	PTY
Reset:	0	0	0	0	0	0	0	0

Figure 12-9. SCI Control Register 1 (SCC1)

LOOPS — Loop Mode Select Bit

This read/write bit enables loop mode operation. In loop mode the RxD pin is disconnected from the SCI, and the transmitter output goes into the receiver input. Both the transmitter and the receiver must be enabled to use loop mode. Reset clears the LOOPS bit.

1 = Loop mode enabled
0 = Normal operation enabled

ENSCI — Enable SCI Bit

This read/write bit enables the SCI and the SCI baud rate generator. Clearing ENSCI sets the SCTE and TC bits in SCI status register 1 and disables transmitter interrupts. Reset clears the ENSCI bit.

1 = SCI enabled
0 = SCI disabled

TXINV — Transmit Inversion Bit

This read/write bit reverses the polarity of transmitted data. Reset clears the TXINV bit.

1 = Transmitter output inverted
0 = Transmitter output not inverted

NOTE: *Setting the TXINV bit inverts all transmitted values, including idle, break, start, and stop bits.*

14.4 Port C

Port C is a 2-bit special function port that shares its pins with the serial communications interface (SCI) module. These pins have software configurable pullups.

14.4.1 Port C Data Register

The port C data register contains a data latch for each of the two port C pins.

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	PTC1	PTC0
Write:								
Reset:	Unaffected by reset							
Alternative Function:							RxD	TxD
Additional Function:							Optional pullup	Optional pullup

Figure 14-5. Port C Data Register (PTC)

PTC[1:0] — Port C Data Bits

These read/write bits are software-programmable. Data direction of each port C pin is under the control of the corresponding bit in data direction register C. Reset has no effect on port C data.

The port C pullup enable bit, PCP, in the port option control register (POCR) enables pullups on PTC[1:0] if the respective pin is configured as an input. (See **14.7 Port Options**.)

TxD, RxD — SCI Data I/O Pins

The TxD and RxD pins are the transmit data output and receive data input for the SCI module. The SCI enable bit, ENSCI, in the SCI control register 1 enables the PTC0/TxD and PTC1/RxD pins as SCI TxD and RxD pins and overrides any control from the port I/O. See **Section 12. Serial Communications Interface Module (SCI)**.

Section 15. External Interrupt (IRQ)

15.1 Contents

15.2 Introduction

The IRQ module provides two external interrupt inputs: one dedicated $\overline{\text{IRQ}}$ pin and one shared port pin, PTE4/D–.

15.3 Features

Features of the IRQ module include:

- Two external interrupt pins, $\overline{\text{IRQ}}$ and PTE4/D–
- $\overline{\text{IRQ}}$ interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Low leakage $\overline{\text{IRQ}}$ pin for external RC wake up input
- Selectable internal pullup resistor

20.4 Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating temperature range	T_A	0 to 70	°C
Operating voltage range	V_{DD}	4.0 to 5.5	V

20.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance LQFP (32 pins) SOIC (28 pins)	θ_{JA}	 95 70	°C/W
I/O pin power dissipation	$P_{I/O}$	User-Determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + (I_{DDA} \times V_{DDA}) + P_{I/O} = K/(T_J + 273\ °C)$	W
Constant(2)	K	$P_D \times (T_A + 273\ °C) + P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	T_{JM}	100	°C

Notes:
1. Power dissipation is a function of temperature.
2. K is a constant unique to the device. K can be determined for a known T_A and measure P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

20.9 TImer Interface Module Characteristics

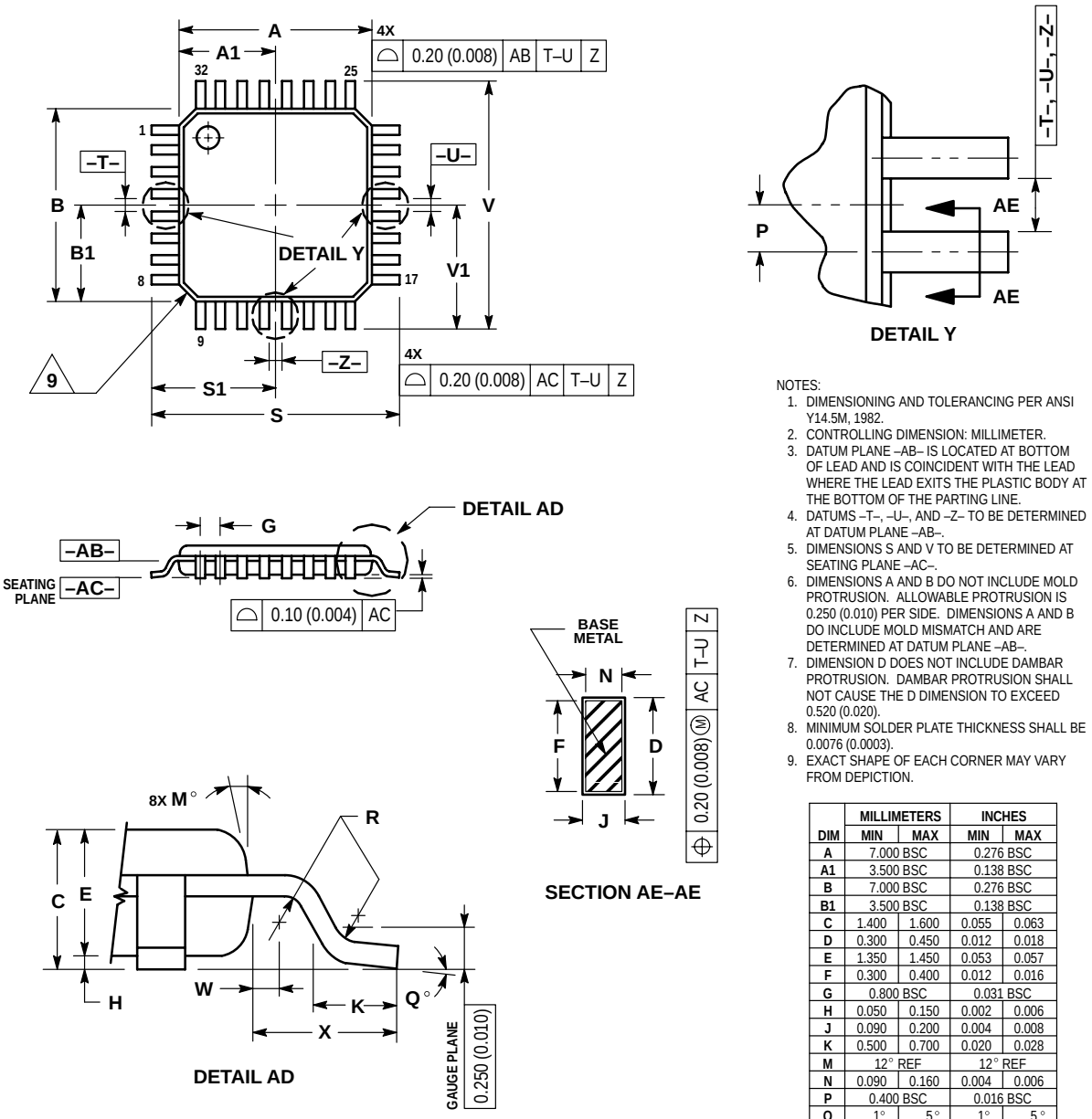
Characteristic	Symbol	Min	Max	Unit
Input capture pulse width	t_{TIH}, t_{TIL}	$1/f_{OP}$	—	ns
Input clock pulse width	t_{TCH}, t_{TCL}	$(1/f_{OP}) + 5$	—	ns

20.10 USB DC Electrical Characteristics

Characteristic[1]	Symbol	Conditions	Min	Typ	Max	Unit
Hi-Z state data line leakage	I_{LO}	0 V<V_{IN}<3.3 V	–10		+10	µA
Voltage input high (driven)	V_{IH}		2.0			V
Voltage input high (floating)	V_{IHZ}		2.7		3.6	V
Voltage input low	V_{IL}				0.8	V
Differential input sensitivity	V_{DI}	|(D+) – (D–)|	0.2			V
Differential common mode range	V_{CM}	Includes V_{DI} Range	0.8		2.5	V
Static output low	V_{OL}	R_L of 1.425 K to 3.6 V			0.3	V
Static output high	V_{OH}	R_L of 14.25 K to GND	2.8		3.6	V
Output signal crossover voltage	V_{CRS}		1.3	—	2.0	V
Regulator bypass capacitor	$C_{REGBYPASS}$			0.1		µF
Regulator bulk capacitor	$C_{REGBULK}$		4.7			µF

Notes:
1. V_{DD} = 4.0 to 5.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted.

21.3 32-Pin Low-Profile Quad Flat Pack (LQFP)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Figure 21-1. 32-Pin LQFP (Case #873A)