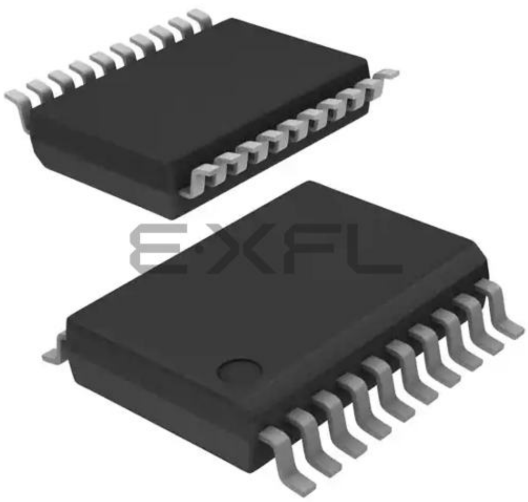

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08ka101-e-ss

20/28-Pin General Purpose, 16-Bit Flash Microcontrollers with nanoWatt XLP Technology

Power Management Modes:

- Run – CPU, Flash, SRAM and Peripherals On
- Doze – CPU Clock Runs Slower than Peripherals
- Idle – CPU Off, Flash, SRAM and Peripherals On
- Sleep – CPU, Flash and Peripherals Off and SRAM On
- Deep Sleep – CPU, Flash, SRAM and Most Peripherals Off:
  - Run mode currents down to 8 µA typical
  - Idle mode currents down to 2 µA typical
  - Deep Sleep mode currents down to 20 nA typical
  - RTCC 490 nA, 32 kHz, 1.8V
  - Watchdog Timer 350 nA, 1.8V typical

High-Performance CPU:

- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Internal Oscillator with 4x PLL Option and Multiple Divide Options
- 17-Bit by 17-Bit Single-Cycle Hardware Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16-Bit x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture

Peripheral Features:

- Hardware Real-Time Clock and Calendar (RTCC):
  - Provides clock, calendar and alarm functions
  - Can run in Deep Sleep Mode
- Programmable Cyclic Redundancy Check (CRC)
- Serial Communication modules:
  - SPI, I²C™ and two UART modules
- Three 16-Bit Timers/Counters with Programmable Prescaler
- 16-Bit Capture Inputs
- 16-Bit Compare/PWM Output
- Configurable Open-Drain Outputs on Digital I/O Pins
- Up to Three External Interrupt Sources

Analog Features:

- 10-Bit, up to 9-Channel Analog-to-Digital Converter:
  - 500 ksps conversion rate
  - Conversion available during Sleep and Idle
- Dual Analog Comparators with Programmable Input/ Output Configuration
- Charge Time Measurement Unit (CTMU):
  - Used for capacitance sensing
  - Time measurement, down to 1 ns resolution
  - Delay/pulse generation, down to 1 ns resolution

Special Microcontroller Features:

- Operating Voltage Range of 1.8V to 3.6V
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Flash Program Memory:
  - Erase/write cycles: 10,000 minimum
  - 40-years' data retention minimum
- Data EEPROM:
  - Erase/write cycles: 100,000 minimum
  - 40-years' data retention minimum
- Fail-Safe Clock Monitor
- System Frequency Range Declaration bits:
  - Declaring the frequency range optimizes the current consumption.
- Flexible Watchdog Timer (WDT) with On-Chip, Low-Power RC Oscillator for Reliable Operation
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Debug (ICD) via two Pins
- Programmable High/Low-Voltage Detect (HLVD)
- Brown-out Reset (BOR):
  - Standard BOR with three programmable trip points; can be disabled in Sleep
- Extreme Low-Power DSBOR for Deep Sleep, LPBOR for all other modes

PIC24F Device	Pins	Program Memory (bytes)	SRAM (bytes)	Data EEPROM (bytes)	Timers 16-Bit	Capture Input	Output Compare/ PWM	UART/ IrDA®	SPI	I²C™	10-Bit A/D (ch)	Comparators	CTMU (ch)	RTCC
08KA101	20	8K	1.5K	512	3	1	1	2	1	1	9	2	9	Y
16KA101	20	16K	1.5K	512	3	1	1	2	1	1	9	2	9	Y
08KA102	28	8K	1.5K	512	3	1	1	2	1	1	9	2	9	Y
16KA102	28	16K	1.5K	512	3	1	1	2	1	1	9	2	9	Y

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all the devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also helps in migrating to the next larger device. This is true when moving between devices with the same pin count, or even jumping from 20-pin to 28-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex.

1.2 Other Special Features

- **Communications:** The PIC24F16KA102 family incorporates a range of serial communication peripherals to handle a range of application requirements. There is an I^{2}C™ module that supports both the Master and Slave modes of operation. It also comprises UARTs with built-in IrDA® encoders/decoders and an SPI module.
- **Real-Time Clock/Calendar:** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speed. The 16-deep result buffer can be used either in Sleep to reduce power, or in Active mode to improve throughput.
- **Charge Time Measurement Unit (CTMU) Interface:** The PIC24F16KA102 family includes the new CTMU interface module, which can be used for capacitive touch sensing, proximity sensing and also for precision time measurement and pulse generation.

1.3 Details on Individual Family Members

Devices in the PIC24F16KA102 family are available in 20-pin and 28-pin packages. The general block diagram for all devices is displayed in Figure 1-1.

The devices are different from each other in two ways:

1. Flash program memory (8 Kbytes for PIC24F08KA devices, 16 Kbytes for PIC24F16KA devices).
2. Available I/O pins and ports (18 pins on two ports for 20-pin devices and 24 pins on two ports for 28-pin devices).
3. Alternate SCLx and SDAx pins are available only in 28-pin devices and not in 20-pin devices.

All other features for devices in this family are identical; these are summarized in Table 1-1.

A list of the pin features available on the PIC24F16KA102 family devices, sorted by function, is provided in Table 1-2.

Note:	Table 1-1 provides the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams on pages 4, 5 and 6 of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 4-12: PORTA REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5[1]	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	TRISA7[4]	TRISA6	—	TRISA4	TRISA3[5,6]	TRISA2[5]	TRISA1	TRISA0	00DF
PORTA	02C2	—	—	—	—	—	—	—	—	RA7[4]	RA6	RA5	RA4[3]	RA3[5,6]	RA2[5]	RA1[2]	RA0[2]	xxxx
LATA	02C4	—	—	—	—	—	—	—	—	LATA7[4]	LATA6	—	LATA4	LATA3[5,6]	LATA2[5]	LATA1	LATA0	xxxx
ODCA	02C6	—	—	—	—	—	—	—	—	ODA7[4]	ODA6	—	ODA4	ODA3[5,6]	ODA2[5]	ODA1	ODA0	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: This bit is available only when MCLRE = 0.

2: A read of RA1 and RA0 results in ‘0’ when debug is active on the PGC2/PGD2 pin.

3: A read of RA4 results in ‘0’ when debug is active on the PGC3/PGD3 pin.

4: These bits are not implemented in 20-pin devices.

5: These bits are available only when the primary oscillator is disabled (POSCMD<1:0> = 00); otherwise read as ‘0’.

6: These bits are available only when the primary oscillator is disabled or EC mode is selected (POSCMD<1:0> = 00 or 11) and CLKO is disabled (OSCIOFNC = 0); otherwise read as ‘0’.

TABLE 4-13: PORTB REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11[3]	TRISB10[3]	TRISB9	TRISB8	TRISB7	TRISB6[3]	TRISB5[3]	TRISB4	TRISB3[3]	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02CA	RB15	RB14	RB13	RB12	RB11[3]	RB10[3]	RB9	RB8	RB7	RB6[3]	RB5[3]	RB4[2]	RB3[3]	RB2	RB1[1]	RB0[1]	xxxx
LATB	02CC	LATB15	LATB14	LATB13	LATB12	LATB11[3]	LATB10[3]	LATB9	LATB8	LATB7	LATB6[3]	LATB5[3]	LATB4	LATB3[3]	LATB2	LATB1	LATB0	xxxx
ODCB	02CE	ODB15	ODB14	ODB13	ODB12	ODB11	ODB10	ODB9	ODB8	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: A read of RB1 and RB0 results in ‘0’ when debug is active on the PGEC1/PGED1 pins.

2: A read of RB4 results in ‘0’ when debug is active on the PGEC3/PGED3 pins.

3: PORTB bits, 11, 10, 6, 5 and 3, are not implemented in 20-pin devices.

TABLE 4-14: PAD CONFIGURATION REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PADCFG1	02FC	—	—	—	—	—	—	—	—	—	—	—	SMBUSDEL	OC1TRIS	RTSECSEL1	RTSECSEL0	—	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

4.3.2 DATA ACCESS FROM PROGRAM MEMORY AND DATA EEPROM MEMORY USING TABLE INSTRUCTIONS

The `TBLRDL` and `TBLWTL` instructions offer a direct method of reading or writing the lower word of any address within the program memory without going through data space. It also offers a direct method of reading or writing a word of any address within data EEPROM memory. The `TBLRDH` and `TBLWTH` instructions are the only method to read or write the upper 8 bits of a program space word as data.

> **Note:** The `TBLRDH` and `TBLWTH` instructions are not used while accessing data EEPROM memory.

The PC is incremented by 2 for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit, word-wide address spaces, residing side by side, each with the same address range. `TBLRDL` and `TBLWTL` access the space which contains the least significant data word, and `TBLRDH` and `TBLWTH` access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. `TBLRDL` (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '`1`'; the lower byte is selected when it is '`0`'.

2. `TBLRDH` (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '`0`'.

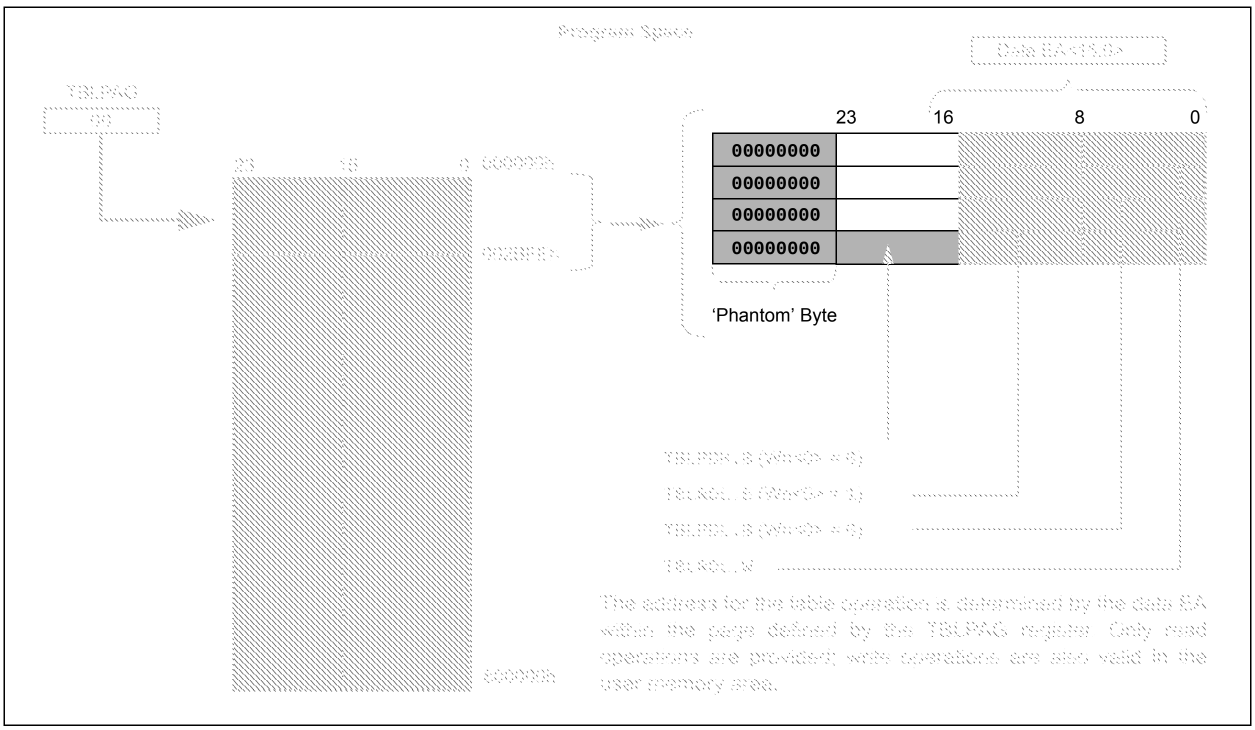
   In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '`0`' when the upper 'phantom' byte is selected (byte select = `1`).

In a similar fashion, two table instructions, `TBLWTH` and `TBLWTL`, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = `0`, the table page is located in the user memory space. When TBLPAG<7> = `1`, the page is located in configuration space.

> **Note:** Only table read operations will execute in the configuration memory space, and only then, in implemented areas, such as the Device ID. Table write operations are not allowed.

FIGURE 4-6: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



5.2 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 32 instructions or 96 bytes. RTSP allows the user to erase blocks of 1 row, 2 rows and 4 rows (32, 64 and 128 instructions) at a time and to program one row at a time. It is also possible to program single words.

The 1-row (96 bytes), 2-row (192 bytes) and 4-row (384 bytes) erase blocks, and single row write block (96 bytes) are edge-aligned, from the beginning of program memory.

When data is written to program memory using `TBLWT` instructions, the data is not written directly to memory. Instead, data written using table writes is stored in holding latches until the programming sequence is executed.

Any number of `TBLWT` instructions can be executed and a write will be successfully performed. However, 32 `TBLWT` instructions are required to write the full row of memory.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

Note:	Writing to a location multiple times without erasing it is not recommended.

All of the table write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

5.3 Enhanced In-Circuit Serial Programming

Enhanced ICSP uses an on-board bootloader, known as the program executive, to manage the programming process. Using an SPI data frame format, the program executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

5.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls the blocks that need to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. Refer to **Section 5.5 “Programming Operations”** for further details.

5.5 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

TABLE 8-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	000104h	Reserved
1	000006h	000106h	Oscillator Failure
2	000008h	000108h	Address Error
3	00000Ah	00010Ah	Stack Error
4	00000Ch	00010Ch	Math Error
5	00000Eh	00010Eh	Reserved
6	000010h	000110h	Reserved
7	000012h	000112h	Reserved

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	Vector Number	IVT Address	AIVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
ADC1 Conversion Done	13	00002Eh	00012Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
Comparator Event	18	000038h	000138h	IFS1<2>	IEC1<2>	IPC4<10:8>
CRC Generator	67	00009Ah	00019Ah	IFS4<3>	IEC4<3>	IPC16<14:12>
CTMU	77	0000AEh	0001AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
External Interrupt 0	0	000014h	000114h	IFS0<0>	IEC0<0>	IPC0<2:0>
External Interrupt 1	20	00003Ch	00013Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
External Interrupt 2	29	00004Eh	00014Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
I2C1 Master Event	17	000036h	000136h	IFS1<1>	IEC1<1>	IPC4<6:4>
I2C1 Slave Event	16	000034h	000134h	IFS1<0>	IEC1<0>	IPC4<2:0>
Input Capture 1	1	000016h	000116h	IFS0<1>	IEC0<1>	IPC0<6:4>
Input Change Notification	19	00003Ah	00013Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
HLVD High/Low-Voltage Detect	72	0000A4h	0001A4h	IFS4<8>	IEC4<8>	IPC17<2:0>
NVM – NVM Write Complete	15	000032h	000132h	IFS0<15>	IEC0<15>	IPC3<14:12>
Output Compare 1	2	000018h	000118h	IFS0<2>	IEC0<2>	IPC0<10:8>
Real-Time Clock/Calendar	62	000090h	000190h	IFS3<14>	IEC3<14>	IPC15<10:8>
SPI1 Error	9	000026h	000126h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Event	10	000028h	000128h	IFS0<10>	IEC0<10>	IPC2<10:8>
Timer1	3	00001Ah	00011Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
Timer2	7	000022h	000122h	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3	8	000024h	000124h	IFS0<8>	IEC0<8>	IPC2<2:0>
UART1 Error	65	000096h	000196h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART1 Receiver	11	00002Ah	00012Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter	12	00002Ch	00012Ch	IFS0<12>	IEC0<12>	IPC3<2:0>
UART2 Error	66	000098h	000198h	IFS4<2>	IEC4<2>	IPC16<10:8>
UART2 Receiver	30	000050h	000150h	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2 Transmitter	31	000052h	000152h	IFS1<15>	IEC1<15>	IPC7<14:12>

REGISTER 8-10: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
U2TXIE	U2RXIE	INT2IE	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIE:** UART2 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **U2RXIE:** UART2 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **MI2C1IE:** Master I2C1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SI2C1IE:** Slave I2C1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-19: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 16-1: SPI1STAT: SPI1 STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0
bit 15							bit 8

R-0,HSC	R/C-0, HS	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R-0, HSC	R-0, HSC
SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	H = Hardware Settable bit	C = Clearable bit
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **SPIEN:** SPI1 Enable bit
1 = Enables module and configures SCK1, SDO1, SDI1 and $\overline{SS1}$ as serial port pins
0 = Disables module

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SPISIDL:** Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as ‘0’

bit 10-8 **SPIBEC<2:0>:** SPI1 Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPI transfers are pending.
Slave mode:
Number of SPI transfers are unread.

bit 7 **SRMPT:** Shift Register (SPI1SR) Empty bit (valid in Enhanced Buffer mode)
1 = SPI1 Shift register is empty and ready to send or receive
0 = SPI1 Shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded
The user software has not read the previous data in the SPI1BUF register.
0 = No overflow has occurred

bit 5 **SRXMPT:** Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = Receive FIFO is empty
0 = Receive FIFO is not empty

bit 4-2 **SISEL<2:0>:** SPI1 Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPI1 transmit buffer is full (SPITBF bit is set)
110 = Interrupt when the last bit is shifted into SPI1SR; as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPI1SR; now the transmit is complete
100 = Interrupt when one data byte is shifted into the SPI1SR; as a result, the TX FIFO has one open spot
011 = Interrupt when the SPI1 receive buffer is full (SPIRBF bit set)
010 = Interrupt when the SPI1 receive buffer is 3/4 or more full
001 = Interrupt when data is available in receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer is read; as a result, the buffer is empty (SRXMPT bit is set)

17.3 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator (BRG) reload value, use Equation 17-1.

EQUATION 17-1: COMPUTING BAUD RATE RELOAD VALUE(1)

$$F_{SCL} = \frac{F_{CY}}{I2C1BRG + 1 + \frac{F_{CY}}{10,000,000}}$$

or

$$I2C1BRG = \left(\frac{F_{CY}}{F_{SCL}} - \frac{F_{CY}}{10,000,000}\right) - 1$$

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

17.4 Slave Address Masking

The I2C1MSK register (Register 17-3) designates address bit positions as "don't care" for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= `1`) in the I2C1MSK register causes the slave module to respond whether the corresponding address bit value is '`0`' or '`1`'. For example, when I2C1MSK is set to '`00100000`', the slave module will detect both addresses: '`0000000`' and '`00100000`'.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the IPMIEN bit (I2C1CON<11>).

> **Note:** As a result of changes in the I^{2}C protocol, the addresses in Table 17-2 are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

TABLE 17-1: I^{2}C™ CLOCK RATES(1)

Required System FSCL	FCY	I2C1BRG Value (Decimal)	I2C1BRG Value (Hexadecimal)	Actual FSCL
100 kHz	16 MHz	157	9D	100 kHz
100 kHz	8 MHz	78	4E	100 kHz
100 kHz	4 MHz	39	27	99 kHz
400 kHz	16 MHz	37	25	404 kHz
400 kHz	8 MHz	18	12	404 kHz
400 kHz	4 MHz	9	9	385 kHz
400 kHz	2 MHz	4	4	385 kHz
1 MHz	16 MHz	13	D	1.026 MHz
1 MHz	8 MHz	6	6	1.026 MHz
1 MHz	4 MHz	3	3	0.909 MHz

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled;

TABLE 17-2: I^{2}C™ RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
`0000 000`	`0`	General Call Address(2)
`0000 000`	`1`	Start Byte
`0000 001`	`x`	Cbus Address
`0000 010`	`x`	Reserved
`0000 011`	`x`	Reserved
`0000 1xx`	`x`	HS Mode Master Code
`1111 1xx`	`x`	Reserved
`1111 0xx`	`x`	10-Bit Slave Upper Byte(3)

Note 1: The address bits listed here will never cause an address match, independent of the address mask settings.
2: The address will be Acknowledged only if GCEN = `1`.
3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

REGISTER 17-2: I2C1STAT: I2C1 STATUS REGISTER (CONTINUED)

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 2 **R/$\overline{\text{W}}$:** Read/$\overline{\text{Write}}$ Information bit (when operating as I^2C slave)
1 = Read – indicates the data transfer is output from slave
0 = Write – indicates the data transfer is input to slave
Hardware is set or clear after reception of I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2C1RCV is full
0 = Receive not complete, I2C1RCV is empty
Hardware is set when I2C1RCV is written with received byte; hardware is clear when software reads I2C1RCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2C1TRN is full
0 = Transmit complete, I2C1TRN is empty
Hardware is set when software writes to I2C1TRN; hardware is clear at completion of data transmission.

REGISTER 18-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0(2)	R/W-0(2)
UARTEN	—	USIDL	IREN(1)	RTSMD	—	UEN1	UEN0
bit 15							bit 8

R/C-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **USIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(1)
1 = IrDA encoder and decoder are enabled
0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **UEN<1:0>:** UARTx Enable bits(2)
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
1 = UARTx will continue to sample the UxRX pin; interrupt generated on falling edge, bit is cleared in hardware on the following rising edge
0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Enable Loopback mode
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is ‘0’
0 = UxRX Idle state is ‘1’

Note 1: This feature is only available for the 16x BRG mode (BRGH = 0).
2: Bit availability depends on pin availability.

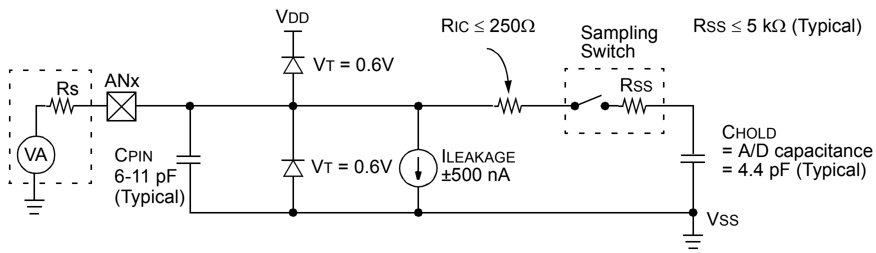
EQUATION 22-1: A/D CONVERSION CLOCK PERIOD[1]

$$ADCS = \frac{T_{AD}}{T_{CY}} - 1$$

$$T_{AD} = T_{CY} \cdot (ADCS + 1)$$

Note 1: Based on T_{CY} = 2 * T_{OSC}; Doze mode and PLL are disabled.

FIGURE 22-2: 10-BIT A/D CONVERTER ANALOG INPUT MODEL



Legend:		
	C_{PIN}	= Input Capacitance
	V_T	= Threshold Voltage
	$I_{LEAKAGE}$	= Leakage Current at the pin due to various junctions
	R_{IC}	= Interconnect Resistance
	R_{SS}	= Sampling Switch Resistance
	C_{HOLD}	= Sample/Hold Capacitance (from A/D)

Note: C_{PIN} value depends on device package and is not tested. Effect of C_{PIN} negligible if $R_S \le 5\ k\Omega$.

REGISTER 24-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = CVREF circuit is powered on
0 = CVREF circuit is powered down

bit 6 **CVROE:** Comparator VREF Output Enable bit
1 = CVREF voltage level is output on CVREF pin
0 = CVREF voltage level is disconnected from CVREF pin

bit 5 **CVRR:** Comparator VREF Range Selection bit
1 = CVRSRC range should be 0 to 0.625 CVRSRC with CVRSRC/24 step size
0 = CVRSRC range should be 0.25 to 0.719 CVRSRC with CVRSRC/32 step size

bit 4 **CVRSS:** Comparator VREF Source Selection bit
1 = Comparator reference source, CVRSRC = VREF+ – VREF-
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR3:CVR0:** Comparator VREF Value Selection 0 ≤ CVR<3:0> ≤ 15 bits

When CVRR = 1 and CVRSS = 0:
CVREF = (CVR<3:0>/24) * (CVRSRC)

When CVRR = 0 and CVRSS = 0:
CVREF = 1/4 (CVRSRC) + (CVR<3:0>/32) * (CVRSRC)

When CVRR = 1 and CVRSS = 1:
CVREF = ((CVR<3:0>/24) * (CVRSRC)) + VREF-

When CVRR = 0 and CVRSS = 1:
CVREF = (1/4 (CVRSRC) + (CVR<3:0>/32) * (CVRSRC)) + VREF-

REGISTER 26-8: FDS: DEEP SLEEP CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
DSWDTEN	DSBOREN	RTCOSC	DSWDTOSC	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
1 = DSWDT is enabled
0 = DSWDT is disabled

bit 6 **DSBOREN:** Deep Sleep/Low-Power BOR Enable bit (does not affect operation in non Deep Sleep modes)
1 = Deep Sleep BOR is enabled in Deep Sleep
0 = Deep Sleep BOR is disabled in Deep Sleep

bit 5 **RTCOSC:** RTCC Reference Clock Select bit
1 = RTCC uses SOSC as a reference clock
0 = RTCC uses LPRC as a reference clock

bit 4 **DSWDTOSC:** DSWDT Reference Clock Select bit
1 = DSWDT uses LPRC as a reference clock
0 = DSWDT uses SOSC as a reference clock

bit 3-0 **DSWDTPS<3:0>:** Deep Sleep Watchdog Timer Postscale Select bits
The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms.
1111 = 1:2,147,483,648 (25.7 days) nominal
1110 = 1:536,870,912 (6.4 days) nominal
1101 = 1:134,217,728 (38.5 hours) nominal
1100 = 1:33,554,432 (9.6 hours) nominal
1011 = 1:8,388,608 (2.4 hours) nominal
1010 = 1:2,097,152 (36 minutes) nominal
1001 = 1:524,288 (9 minutes) nominal
1000 = 1:131,072 (135 seconds) nominal
0111 = 1:32,768 (34 seconds) nominal
0110 = 1:8,192 (8.5 seconds) nominal
0101 = 1:2,048 (2.1 seconds) nominal
0100 = 1:512 (528 ms) nominal
0011 = 1:128 (132 ms) nominal
0010 = 1:32 (33 ms) nominal
0001 = 1:8 (8.3 ms) nominal
0000 = 1:2 (2.1 ms) nominal

REGISTER 26-9: DEVID: DEVICE ID REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as '0'

bit 15-8 **FAMID<7:0>:** Device Family Identifier bits
00001011 = PIC24F16KA102 family

bit 7-0 **DEV<7:0>:** Individual Device Identifier bits
00000011 = PIC24F16KA102
00001010 = PIC24F08KA102
00000001 = PIC24F16KA101
00001000 = PIC24F08KA101

REGISTER 26-10: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-4 **Unimplemented:** Read as '0'

bit 3-0 **REV<3:0>:** Minor Revision Identifier bits

FIGURE 29-18: SPIx MODULE MASTER MODE TIMING CHARACTERISTICS (CKE = 1)

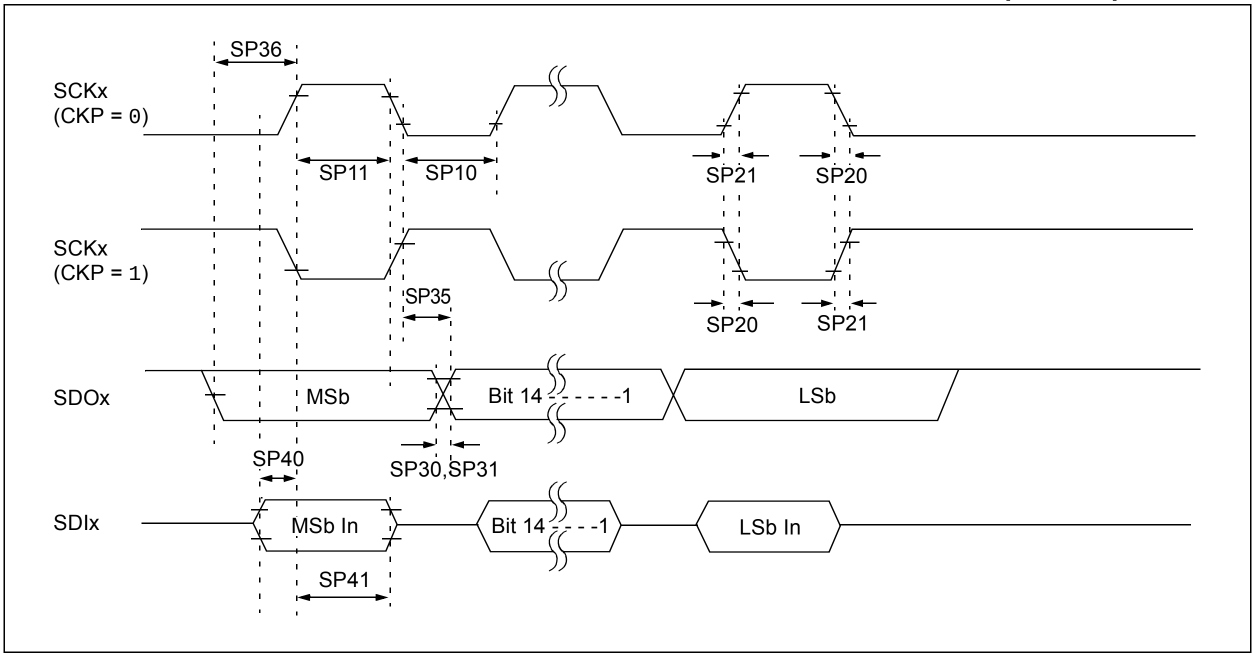


TABLE 29-37: SPIx MODULE MASTER MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
SP10	TscL	SCKx Output Low Time(2)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(2)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(3)	—	10	25	ns	
SP21	TscR	SCKx Output Rise Time(3)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(3)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(3)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

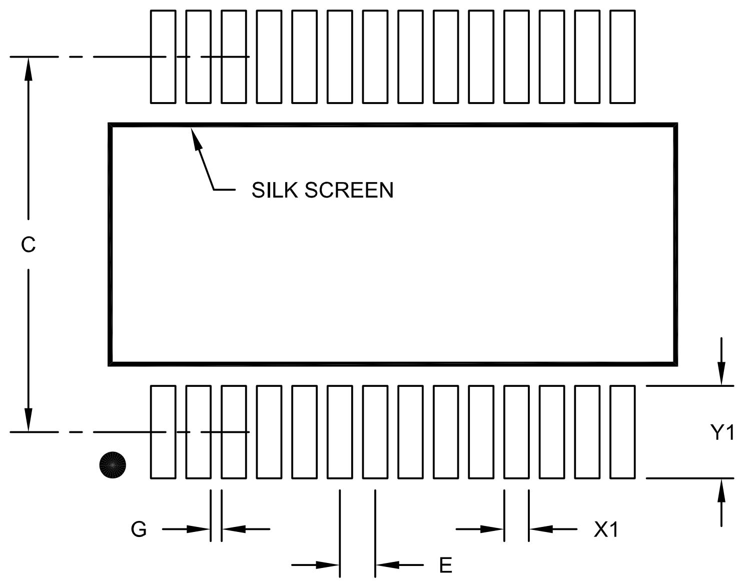
Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

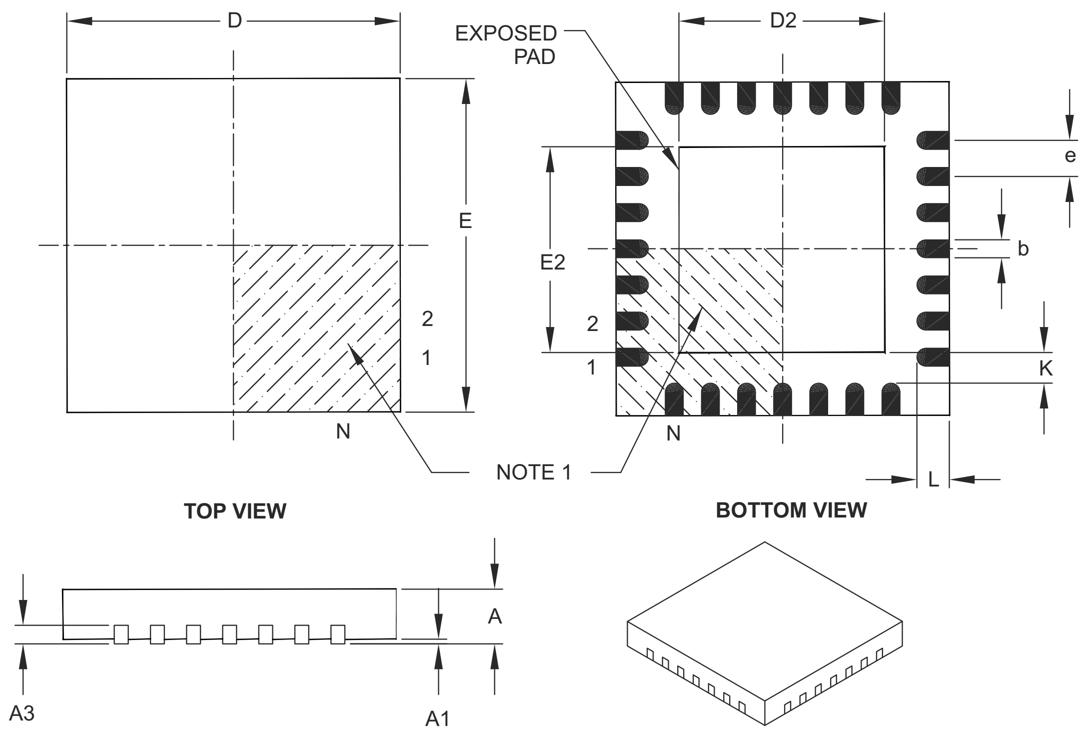
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

APPENDIX A: REVISION HISTORY

Revision A (November 2008)

Original data sheet for the PIC24F16KA102 family of devices.

Revision B (March 2009)

Section 29.0 "Electrical Characteristics" was revised and minor text edits were made throughout the document.

Revision C (October 2011)

- Changed all instances of DSWSRC to DSWAKE.
- Corrected Example 5-2.
- Corrected Example 5-4.
- Corrected Example 6-1.
- Corrected Example 6-3.
- Added a comment to Example 6-5.
- Corrected Figure 9-1 to connect the SOSCI and SOSCO pins to the Schmitt trigger correctly.
- Added register descriptions for PMD1, PMD2, PMD3 and PMD4.
- Added note that RTCC will run in Reset.
- Corrected time values of ADCS (AD1CON3<5:0>).
- Corrected CH0SB and CH0SA (AD1CHS<11:8> and AD1CHS<3:0>) to correctly reference AVDD and AN3.
- Added description of PGCF15 and PGCF14 (AD1PCFG<15:14>).
- Edited Figure 22-2 to correctly reference RIC and the A/D capacitance.
- Changed all references from CTEDG1 to CTED1.
- Changed all references from CTEDG2 to CTED2.
- Changed description of CMIDL: it used to say it disables all comparators in Idle, now only disables interrupts in Idle mode.
- Changed all references of RTCCKSEL to RTCOSC.
- Changed all references of DSLPBOR to DSBOREN.
- Changed all references of DSWCKSEL to DSWDTOSC
- Imported Figure 40-9 from PIC24F FRM, Section 40.
- Added spec for BOR hysteresis.
- Edited Note 1 for Table 29-5 to further describe LPBOR.
- Edited max values of DC20d and DC20e on Table 29-6.
- Edited typical value for DC61-DC61c in Table 29-8.
- Edited Note 2 of Table 29-8.
- Added Note 5 to Table 29-9.
- Added Table 29-15.
- Added AD08 and AD09 in Table 29-26.
- Added Note 3 to Table 29-26.
- Imported Figure 40.10 from PIC24F FRM, Section 40.
- Deleted TVREG spec.
- Imported Figure 15-5 from PIC24F FRM, Section 15.
- Imported Table 15-4 from PIC24F FRM, Section 15.
- Imported Figure 16-22 from PIC24F FRM, Section 16.
- Imported Table 16-9 from PIC24F FRM, Section 16.
- Imported Figure 16-23 from PIC24F FRM, Section 16.
- Imported Table 16-10 from PIC24F FRM, Section 16.
- Imported Figure 21-24 from PIC24F FRM. Section 21.
- Imported Figure 21-25 from PIC24F FRM, Section 21.
- Imported Table 21-5 from PIC24F FRM, Section 21.
- Imported Figure 23-17 from PIC24F FRM, Section 23.
- Imported Table 23-3 from PIC24F FRM, Section 23.
- Imported Figure 23-18 from PIC24F FRM, Section 23.
- Imported Table 23-4 from PIC24F FRM, Section 23.
- Imported Figure 23-19 from PIC24F FRM, Section 23.
- Imported Table 23-5 from PIC24F FRM, Section 23.
- Imported Figure 23-20 from PIC24F FRM, Section 23.
- Imported Table 23-6 from PIC24F FRM, Section 23.
- Imported Figure 24-33 from PIC24F FRM, Section 24.
- Imported Table 24-6 from PIC24F FRM, Section 24.
- Imported Figure 24-34 from PIC24F FRM, Section 24.
- Imported Table 24-7 from PIC24F FRM, Section 24.
- Imported Figure 24-35 from PIC24F FRM, Section 24.
- Imported Table 24-8 from PIC24F FRM, Section 24.
- Imported Figure 24-36 from PIC24F FRM, Section 24.
- Imported Table 24-9 from PIC24F FRM, Section 24.