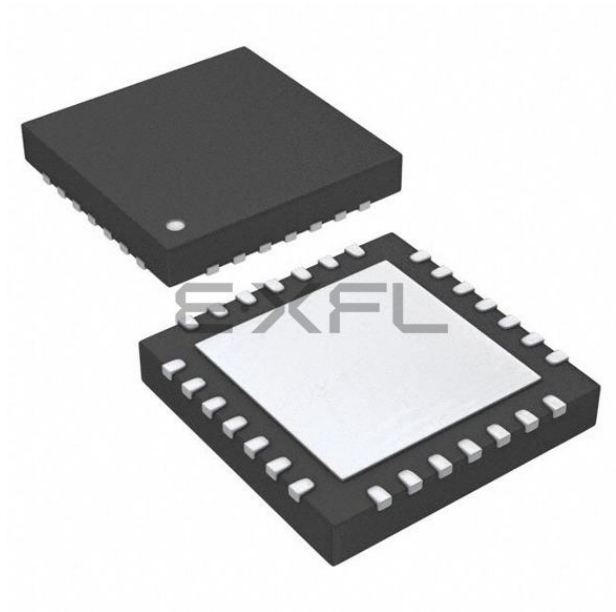


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08ka102-i-ml

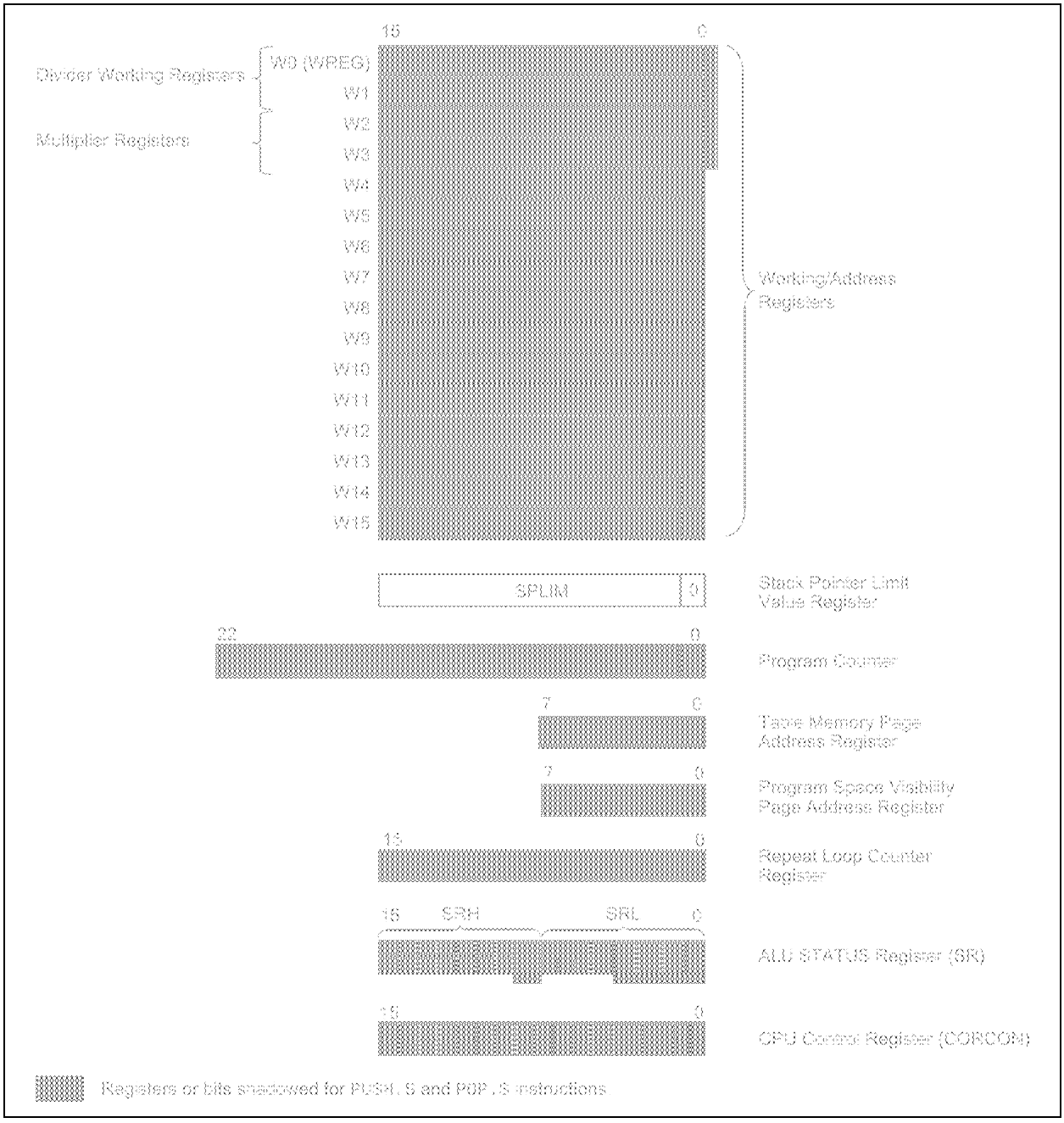
TABLE 1-2: PIC24F16KA102 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number				I/O	Input Buffer	Description
	20-Pin PDIP/SSOP/ SOIC	20-Pin QFN	28-Pin SPDIP/ SSOP/SOIC	28-Pin QFN			
PGC1	5	2	5	2	I/O	ST	In-Circuit Debugger and ICSP™ Programming Clock
PGD1	4	1	4	1	I/O	ST	In-Circuit Debugger and ICSP Programming Data
PGC2	2	19	22	19	I/O	ST	In-Circuit Debugger and ICSP Programming Clock
PGD2	3	20	21	18	I/O	ST	In-Circuit Debugger and ICSP Programming Data
PGC3	10	7	15	12	I/O	ST	In-Circuit Debugger and ICSP Programming Clock
PGD3	9	6	14	11	I/O	ST	In-Circuit Debugger and ICSP Programming Data
RA0	2	19	2	27	I/O	ST	PORTA Digital I/O
RA1	3	20	3	28	I/O	ST	
RA2	7	4	9	6	I/O	ST	
RA3	8	5	10	7	I/O	ST	
RA4	10	7	12	9	I/O	ST	
RA5	1	18	1	26	I/O	ST	
RA6	14	11	20	17	I/O	ST	
RA7	—	—	19	16	I/O	ST	
RB0	4	1	4	1	I/O	ST	PORTB Digital I/O
RB1	5	2	5	2	I/O	ST	
RB2	6	3	6	3	I/O	ST	
RB3	—	—	7	4	I/O	ST	
RB4	9	6	11	8	I/O	ST	
RB5	—	—	14	11	I/O	ST	
RB6	—	—	15	12	I/O	ST	
RB7	11	8	16	13	I/O	ST	
RB8	12	9	17	14	I/O	ST	
RB9	13	10	18	15	I/O	ST	
RB10	—	—	21	18	I/O	ST	
RB11	—	—	22	19	I/O	ST	
RB12	15	12	23	20	I/O	ST	
RB13	16	13	24	21	I/O	ST	
RB14	17	14	25	22	I/O	ST	
RB15	18	15	26	23	I/O	ST	
REFO	18	15	26	23	O	—	Reference Clock Output
RTCC	17	14	25	22	O	—	Real-Time Clock Alarm Output
SCK1	15	12	22	19	I/O	ST	SPI1 Serial Clock Input/Output
SCL1	12	9	17, 15(1)	14, 12 (1)	I/O	I^2C	I2C1 Synchronous Serial Clock Input/Output
SDA1	13	10	18, 14(1)	15, 11(1)	I/O	I^2C	I2C1 Data Input/Output
SDI1	17	14	21	18	I	ST	SPI1 Serial Data Input
SDO1	16	13	24	21	O	—	SPI1 Serial Data Output
SOSCI	9	6	11	8	I	ANA	Secondary Oscillator Input
SOSCO	10	7	12	9	O	ANA	Secondary Oscillator Output
$\overline{SS1}$	18	15	26	23	I/O	ST	Slave Select Input/Frame Select Output (SPI1)

Legend: ST = Schmitt Trigger input buffer, ANA = Analog level input/output, I^2C™ = I^2C/SMBus input buffer

Note 1: Alternative multiplexing when the I2C1SEL Configuration bit is cleared.

FIGURE 3-2: PROGRAMMER'S MODEL



5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Flash Programming, refer to the *"PIC24F Family Reference Manual"*, **Section 4. "Program Memory"** (DS39715).

The PIC24FJ64GA family of devices contains internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable when operating with VDD over 1.8V.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24F16KA102 device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (which are named PGCx and PGDx, respectively), and three other lines for power (VDD), ground (VSS) and Master Clear/Program Mode Entry Voltage (MCLR/VPP). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or custom firmware to be programmed.

Real-Time Self-Programming (RTSP) is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user may write program memory data in blocks of 32 instructions (96 bytes) at a time, and erase program memory in blocks of 32, 64 and 128 instructions (96,192 and 384 bytes) at a time.

The NVMOP<1:0> (NVMCON<1:0>) bits decide the erase block size.

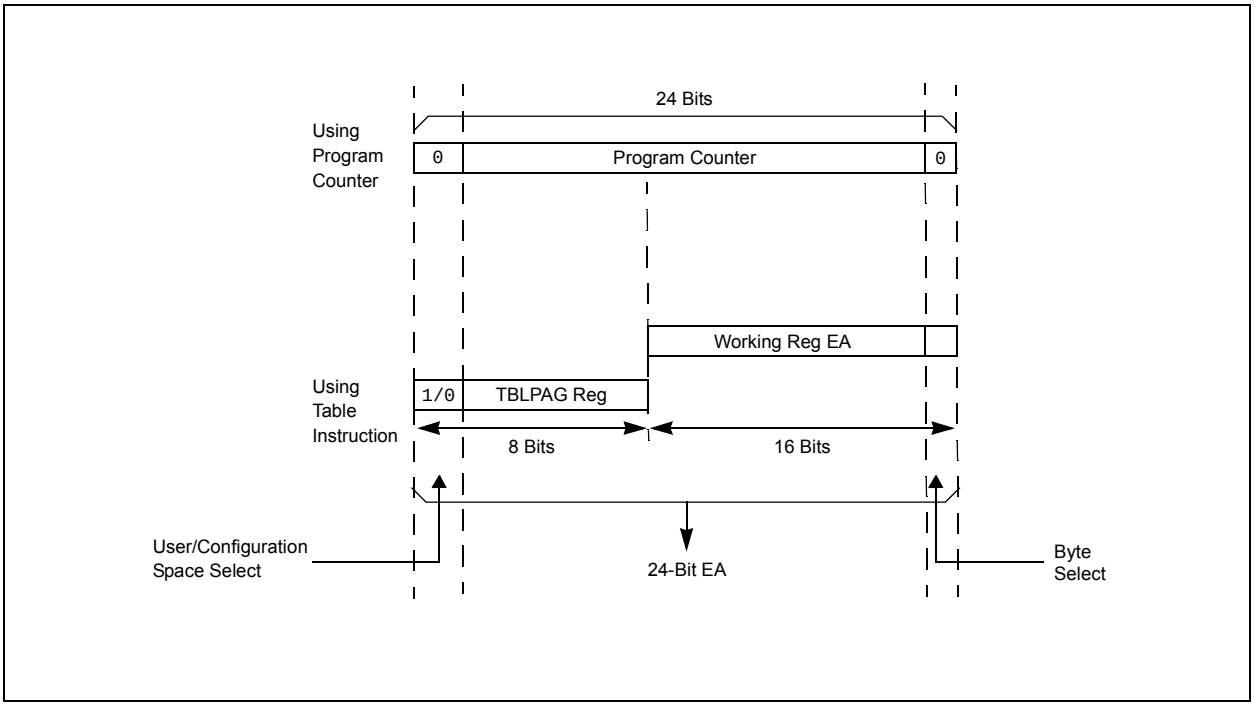
5.1 Table Instructions and Flash Programming

Regardless of the method used, Flash memory programming is done with the table read and write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as depicted in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



REGISTER 7-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-up Reset has occurred
0 = A Power-up Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #SLEEP Instruction	POR
IDLE (RCON<2>)	PWRSAV #IDLE Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—
DPSLP (RCON<10>)	PWRSAV #SLEEP instruction with DSCON <DSEN> set	POR

Note: All Reset flag bits may be set or cleared by the user software.

REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5(1)	TUN4(1)	TUN3(1)	TUN2(1)	TUN1(1)	TUN0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

011111 = Maximum frequency deviation
011110
.
.
.
000001
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111
.
.
.
100001
100000 = Minimum frequency deviation

Note 1: Increments or decrements of TUN<5:0> may not change the FRC frequency in equal steps over the FRC tuning range and may not be monotonic.

REGISTER 10-1: DSCON: DEEP SLEEP CONTROL REGISTER(1)

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DSEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/C-0, HS
—	—	—	—	—	—	DSBOR(2)	RELEASE
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DSEN:** Deep Sleep Enable bit
1 = Enters Deep Sleep on execution of PWRSAV #0
0 = Enters normal Sleep on execution of PWRSAV #0

bit 14-2 **Unimplemented:** Read as '0'

bit 1 **DSBOR:** Deep Sleep BOR Event bit(2)
1 = The DSBOR was active and a BOR event was detected during Deep Sleep
0 = The DSBOR was not active, or was active but did not detect a BOR event during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
1 = Upon waking from Deep Sleep, I/O pins maintain their states previous to Deep Sleep entry
0 = Release I/O pins from their state previous to Deep Sleep entry, and allow their respective TRIS and LAT bits to control their states

Note 1: All register bits are reset only in the case of a POR event outside of Deep Sleep mode.
2: Unlike all other events, a Deep Sleep BOR event will NOT cause a wake-up from Deep Sleep; this re-arms POR.

14.0 INPUT CAPTURE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Input Capture, refer to the *"PIC24F Family Reference Manual"*, **Section 15. "Input Capture"** (DS39701).

The input capture module is used to capture a timer value from one of two selectable time bases upon an event on an input pin.

The input capture features are quite useful in applications requiring frequency (Time Period) and pulse measurement. Figure 14-1 depicts a simplified block diagram of the input capture module.

The PIC24F16KA102 family devices have one input capture channel. The input capture module has multiple operating modes, which are selected via the IC1CON register. The operating modes include:

- Capture timer value on every falling edge of input applied at the IC1 pin
- Capture timer value on every rising edge of input applied at the IC1 pin
- Capture timer value on every 4th rising edge of input applied at the IC1 pin
- Capture timer value on every 16th rising edge of input applied at the IC1 pin
- Capture timer value on every rising and every falling edge of input applied at the IC1 pin
- Device wake-up from capture pin during CPU Sleep and Idle modes

The input capture module has a four-level FIFO buffer. The number of capture events required to generate a CPU interrupt can be selected by the user.

FIGURE 14-1: INPUT CAPTURE BLOCK DIAGRAM

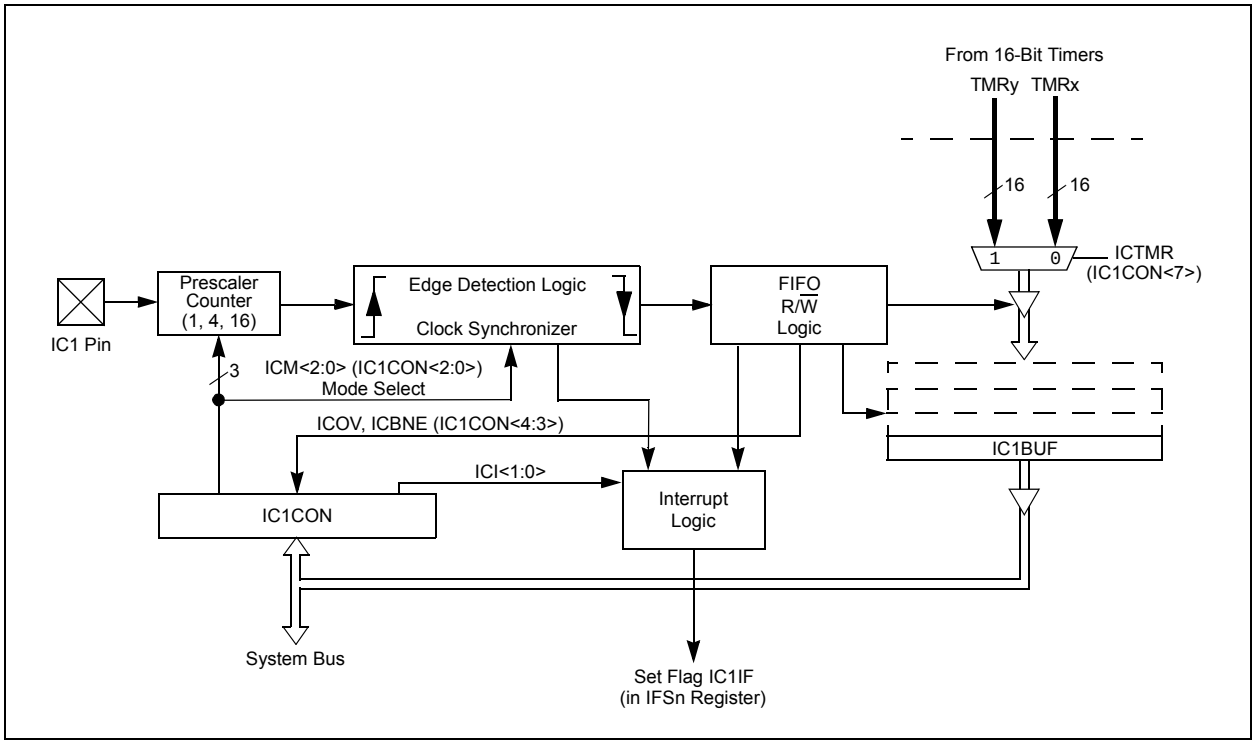
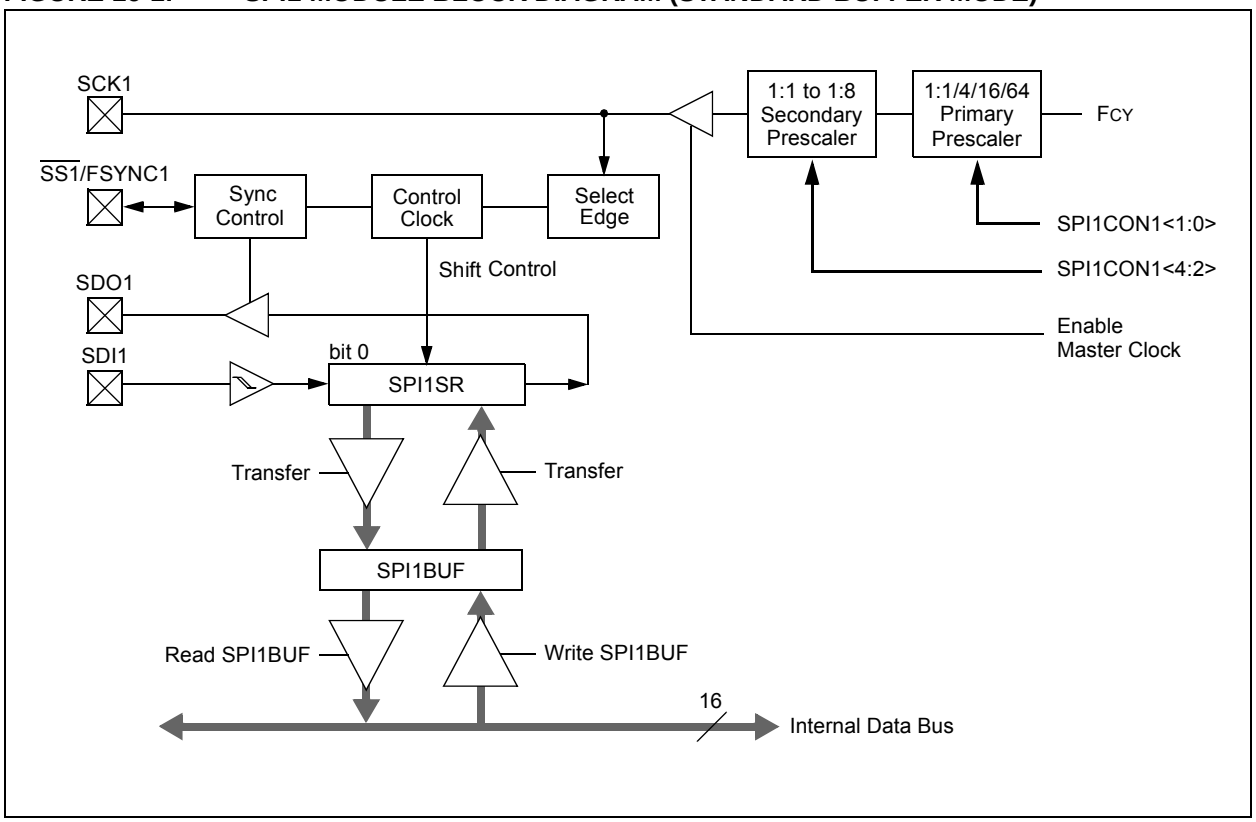


FIGURE 16-1: SPI1 MODULE BLOCK DIAGRAM (STANDARD BUFFER MODE)



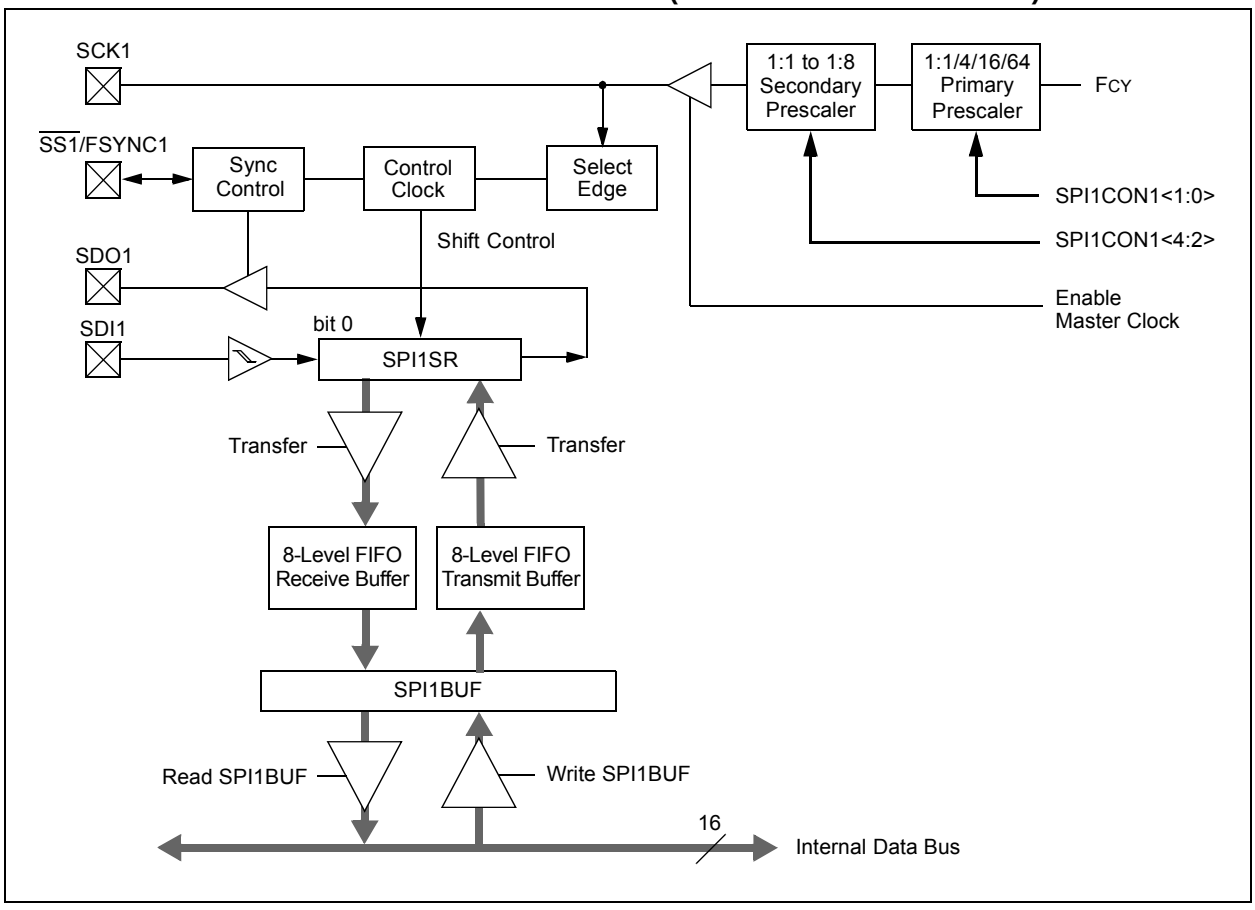
To set up the SPI module for the Enhanced Buffer Master (EBM) mode of operation:

1. If using interrupts:
   a) Clear the respective SPI1IF bit in the IFS0 register.
   b) Set the respective SPI1IE bit in the IEC0 register.
   c) Write the respective SPI1IPx bits in the IPC2 register.
2. Write the desired settings to the SPI1CON1 and SPI1CON2 registers with the MSTEN bit (SPI1CON1<5>) = 1.
3. Clear the SPIROV bit (SPI1STAT<6>).
4. Select Enhanced Buffer mode by setting the SPIBEN bit (SPI1CON2<0>).
5. Enable SPI operation by setting the SPIEN bit (SPI1STAT<15>).
6. Write the data to be transmitted to the SPI1BUF register. Transmission (and reception) will start as soon as data is written to the SPI1BUF register.

To set up the SPI module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPI1BUF register.
2. If using interrupts:
   a) Clear the respective SPI1IF bit in the IFS0 register.
   b) Set the respective SPI1IE bit in the IEC0 register.
   c) Write the respective SPI1IPx bits in the IPC2 register to set the interrupt priority.
3. Write the desired settings to the SPI1CON1 and SPI1CON2 registers with the MSTEN bit (SPI1CON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SS1}$ pin.
6. Clear the SPIROV bit (SPI1STAT<6>).
7. Select Enhanced Buffer mode by setting the SPIBEN bit (SPI1CON2<0>).
8. Enable SPI operation by setting the SPIEN bit (SPI1STAT<15>).

FIGURE 16-2: SPI1 MODULE BLOCK DIAGRAM (ENHANCED BUFFER MODE)



REGISTER 16-1: SPI1STAT: SPI1 STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPI1 Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPI1TXB is full
0 = Transmit has started, SPI1TXB is empty

In Standard Buffer mode:
Automatically set in hardware when the CPU writes to the SPITBF location, loading SPITBF.
Automatically cleared in hardware when the SPI1 module transfers data from SPI1TXB to SPIRBF.

In Enhanced Buffer mode:
Automatically set in hardware when CPU writes to the SPI1BUF location, loading the last available buffer location.
Automatically cleared in hardware when a buffer location is available for a CPU write.

bit 0 **SPIRBF:** SPI1 Receive Buffer Full Status bit

1 = Receive is complete; SPI1RXB is full
0 = Receive is not complete; SPI1RXB is empty

In Standard Buffer mode:
Automatically set in hardware when SPI1 transfers data from SPIRBF to SPIRBF.
Automatically cleared in hardware when the core reads the SPI1BUF location, reading SPIRBF.

In Enhanced Buffer mode:
Automatically set in hardware when SPI1 transfers data from SPI1SR to buffer, filling the last unread buffer location.
Automatically cleared in hardware when a buffer location is available for a transfer from SPI1SR.

REGISTER 16-2: SPI1CON1: SPI1 CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCK1 pin bit (SPI Master modes only)
1 = Internal SPI clock is disabled, pin functions as I/O
0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disables SDO1 pin bit
1 = SDO1 pin is not used by module; pin functions as I/O
0 = SDO1 pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPI1 Data Input Sample Phase bit
Master mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave mode:
SMP must be cleared when SPI1 is used in Slave mode.

bit 8 **CKE:** SPI1 Clock Edge Select bit(1)
1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)
1 = $\overline{SS1}$ pin is used for Slave mode
0 = $\overline{SS1}$ pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)
111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
.
.
.
000 = Secondary prescale 8:1

Note 1: The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).

REGISTER 16-2: SPI1CON1: SPI1 CONTROL REGISTER 1 (CONTINUED)

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).

REGISTER 16-3: SPI1CON2: SPI1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	SPIFPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SPIFE	SPIBEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN:** Framed SPI1 Support bit
1 = Framed SPI1 support is enabled
0 = Framed SPI1 support is disabled

bit 14 **SPIFSD:** Frame Sync Pulse Direction Control on $\overline{SS1}$ Pin bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)

bit 13 **SPIFPOL:** Frame Sync Pulse Polarity bit (Frame mode only)
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with the first bit clock
0 = Frame sync pulse precedes the first bit clock

bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced Buffer is enabled
0 = Enhanced Buffer is disabled (Legacy mode)

REGISTER 20-2: CRCXOR: CRC XOR POLYNOMIAL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X15	X14	X13	X12	X11	X10	X9	X8
bit 15							bit 8

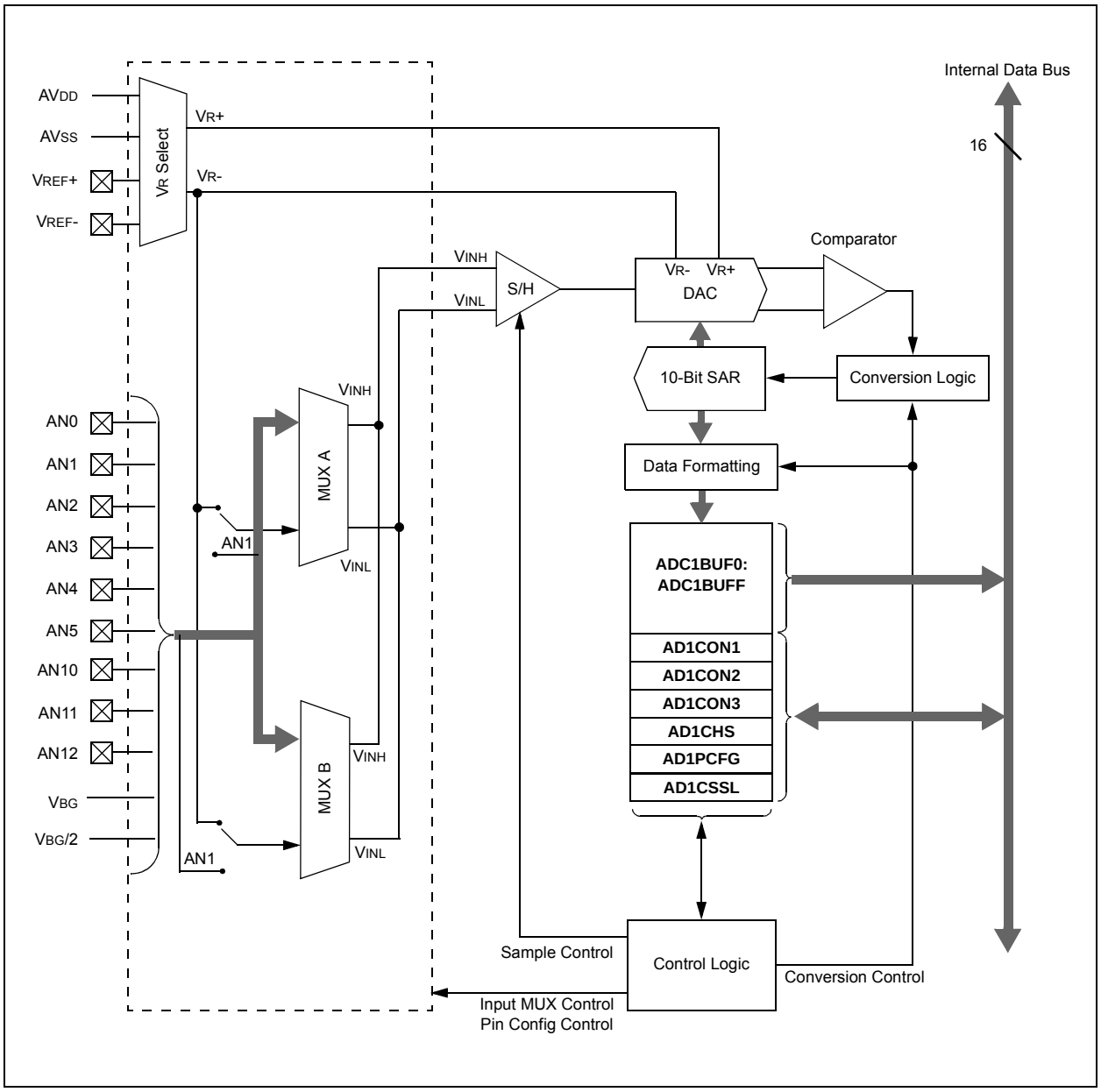
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X7	X6	X5	X4	X3	X2	X1	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **X<15:1>:** XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented:** Read as ‘0’

FIGURE 22-1: 10-BIT HIGH-SPEED A/D CONVERTER BLOCK DIAGRAM



REGISTER 26-6: FPOR: RESET CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-0	R/P-1	R/P-1
MCLRE(2)	BORV1(3)	BORV0(3)	I2C1SEL(1)	PWRTEN	—	BOREN1	BOREN0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit(2)
1 = $\overline{\text{MCLR}}$ pin is enabled; RA5 input pin is disabled
0 = RA5 input pin is enabled; $\overline{\text{MCLR}}$ is disabled

bit 6-5 **BORV<1:0>:** Brown-out Reset Enable bits(3)
11 = Brown-out Reset is set to the lowest voltage
10 = Brown-out Reset
01 = Brown-out Reset is set to the highest voltage
00 = Low-Power Brown-out Reset occurs around 2.0V

bit 4 **I2C1SEL:** Alternate I2C1 Pin Mapping bit(1)
0 = Alternate location for SCL1/SDA1 pins
1 = Default location for SCL1/SDA1 pins

bit 3 **PWRTEN:** Power-up Timer Enable bit
0 = PWRT is disabled
1 = PWRT is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

Note 1: Applies only to 28-pin devices.
2: The MCLRE fuse can only be changed when using the VPP-Based ICSP™ mode entry. This prevents a user from accidentally locking out the device from the low-voltage test entry.
3: Refer to Section 29.0, Electrical Characteristics for the BOR voltages.

27.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

27.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

27.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

27.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

27.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
ULNK	ULNK		Unlink Frame Pointer	1	1	None
XOR	XOR	f	f = f .XOR. WREG	1	1	N, Z
	XOR	f,WREG	WREG = f .XOR. WREG	1	1	N, Z
	XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
	XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N, Z
	XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N, Z
ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C, Z, N

TABLE 29-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**	
Power-Down Current (IPD): PMD Bits are Set, PMSLP Bit is '0'(2)					
DC62	0.450	0.650	μA	-40°C	1.8V, Timer1 w/32 kHz Crystal: T132 (SOSC – LP)(3)
DC62a		0.650		+25°C	
DC62b		0.650		+60°C	
DC62c		0.650		+85°C	
DC62d		—		+125°C	
DC62e	0.730	0.980	μA	-40°C	3.3V, Timer1 w/32 kHz Crystal: T132 (SOSC – LP)(3)
DC62f		0.980		+25°C	
DC62g		0.980		+60°C	
DC62h		0.980		+85°C	
DC62i		—		+125°C	
DC64	5.5	7.10	μA	-40°C	1.8V, HLVD(3,4)
DC64a		7.10		+25°C	
DC64b		7.80		+60°C	
DC64c		8.30		+85°C	
DC64d		10.00		+125°C	
DC64e	6.2	7.10	μA	-40°C	3.3V, HLVD(3,4)
DC64f		7.10		+25°C	
DC64g		7.80		+60°C	
DC64h		8.30		+85°C	
DC64i		9.00		+125°C	
DC63	4.5	6.60	μA	-40°C	3.3V, BOR(3,4)
DC63a		6.60		+25°C	
DC63b		6.60		+60°C	
DC63c		6.60		+85°C	
DC63d		9.00		+125°C	
DC62	0.49	0.65	μA	-40°C	1.8V, RTCC(3,5)
DC62a		0.65		+25°C	
DC62b		0.65		+60°C	
DC62c		0.65		+85°C	
DC62d		0.98		+125°C	
DC62e	0.80	0.98	μA	-40°C	3.3V, RTCC(3,5)
DC62f		0.98		+25°C	
DC62g		0.98		+60°C	
DC62h		0.98		+85°C	
DC62i		0.98		+125°C	

Note 1: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low. WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

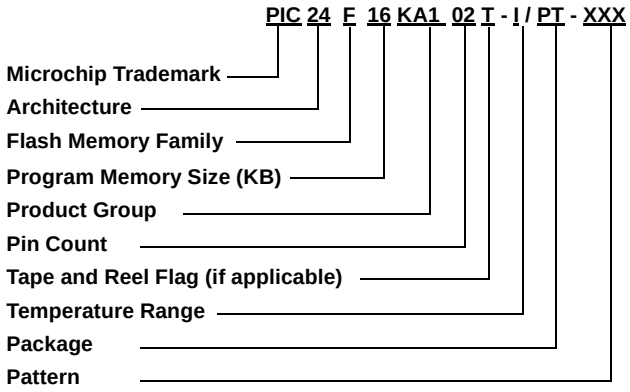
4: Current applies to Sleep only.

5: Current applies to Sleep and Deep Sleep.

6: Current applies to Deep Sleep only.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	F	= Flash program memory
Product Group	KA1	= General purpose microcontrollers
Pin Count	01 02	= 20-pin = 28-pin
Temperature Range	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package	SP SO SS ML P	= SPDIP = SOIC = SSOP = QFN = PDIP
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample	

Examples:

a) PIC24F16KA102-I/ML: General purpose, 16-Kbyte program memory, 28-pin, Industrial temp., QFN package.