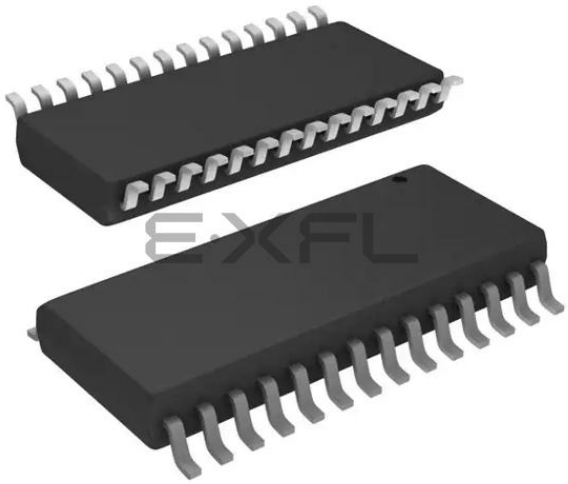

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Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08ka102-i-so

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2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins and other signals, in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

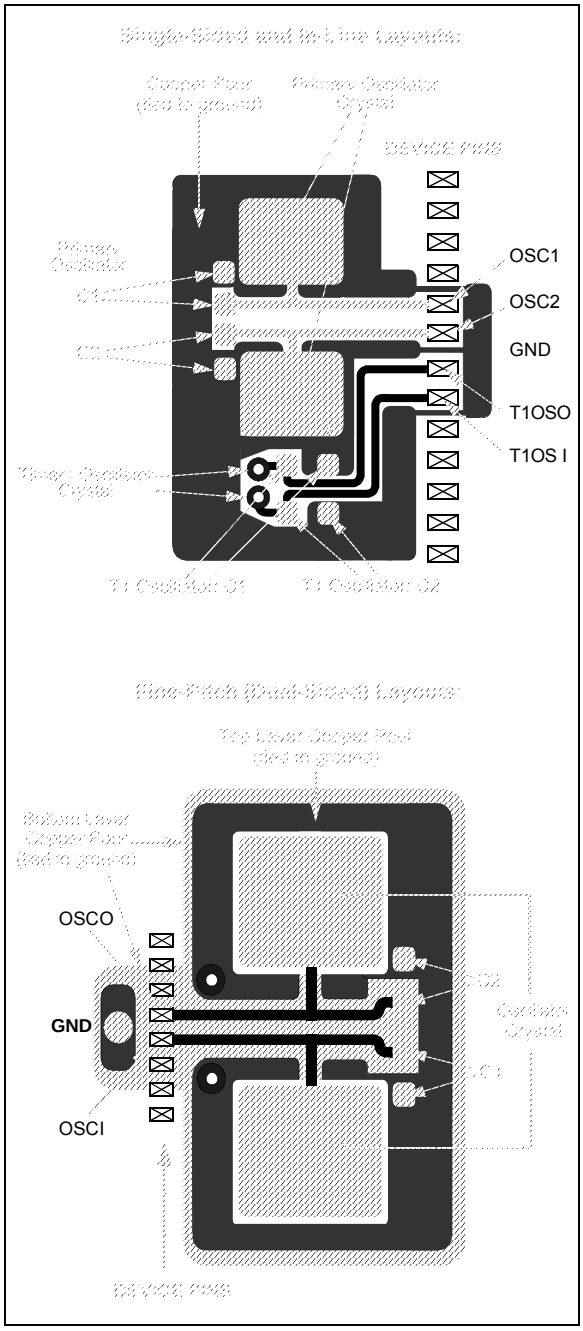
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- *AN849, "Basic PICmicro® Oscillator Design"*
- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output to logic low.

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



6.4.1.1 Data EEPROM Bulk Erase

To erase the entire data EEPROM (bulk erase), the address registers do not need to be configured because this operation affects the entire data EEPROM. The following sequence helps in performing bulk erase:

1. Configure NVMCON to Bulk Erase mode.
2. Clear NVMIF status bit and enable NVM interrupt (optional).
3. Write the key sequence to NVMKEY.
4. Set the WR bit to begin erase cycle.
5. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical bulk erase sequence is provided in Example 6-3.

6.4.2 SINGLE-WORD WRITE

To write a single word in the data EEPROM, the following sequence must be followed:

1. Erase one data EEPROM word (as mentioned in **Section 6.4.1 "Erase Data EEPROM"**) if the PGMONLY bit (NVMCON<12>) is set to '1'.
2. Write the data word into the data EEPROM latch.
3. Program the data word into the EEPROM:
   - Configure the NVMCON register to program one EEPROM word (NVMCON<5:0> = 0001xx).
   - Clear NVMIF status bit and enable NVM interrupt (optional).
   - Write the key sequence to NVMKEY.
   - Set the WR bit to begin erase cycle.
   - Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).
   - To get cleared, wait until NVMIF is set.

A typical single-word write sequence is provided in Example 6-4.

EXAMPLE 6-3: DATA EEPROM BULK ERASE

```
// Set up NVMCON to bulk erase the data EEPROM
NVMCON = 0x4050;

// Disable Interrupts For 5 Instructions
asm volatile ("disi #5");

// Issue Unlock Sequence and Start Erase Cycle
__builtin_write_NVM();
```

EXAMPLE 6-4: SINGLE-WORD WRITE TO DATA EEPROM

```
int __attribute__ ((space(eedata))) eeData = 0x1234;  // Variable located in EEPROM,declared as a
                                                         global variable.
   int newData;                                       // New data to write to EEPROM
   unsigned int offset;

   // Set up NVMCON to erase one word of data EEPROM
   NVMCON = 0x4004;

   // Set up a pointer to the EEPROM location to be erased
   TBLPAG = __builtin_tblpage(&eeData);               // Initialize EE Data page pointer
   offset = __builtin_tbloffset(&eeData);             // Initizlize lower word of address
   __builtin_tblwtl(offset, newData);                 // Write EEPROM data to write latch

   asm volatile ("disi #5");                          // Disable Interrupts For 5 Instructions
   __builtin_write_NVM();                             // Issue Unlock Sequence & Start Write Cycle
```

REGISTER 8-14: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	T2IP2	T2IP1	T2IP0	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

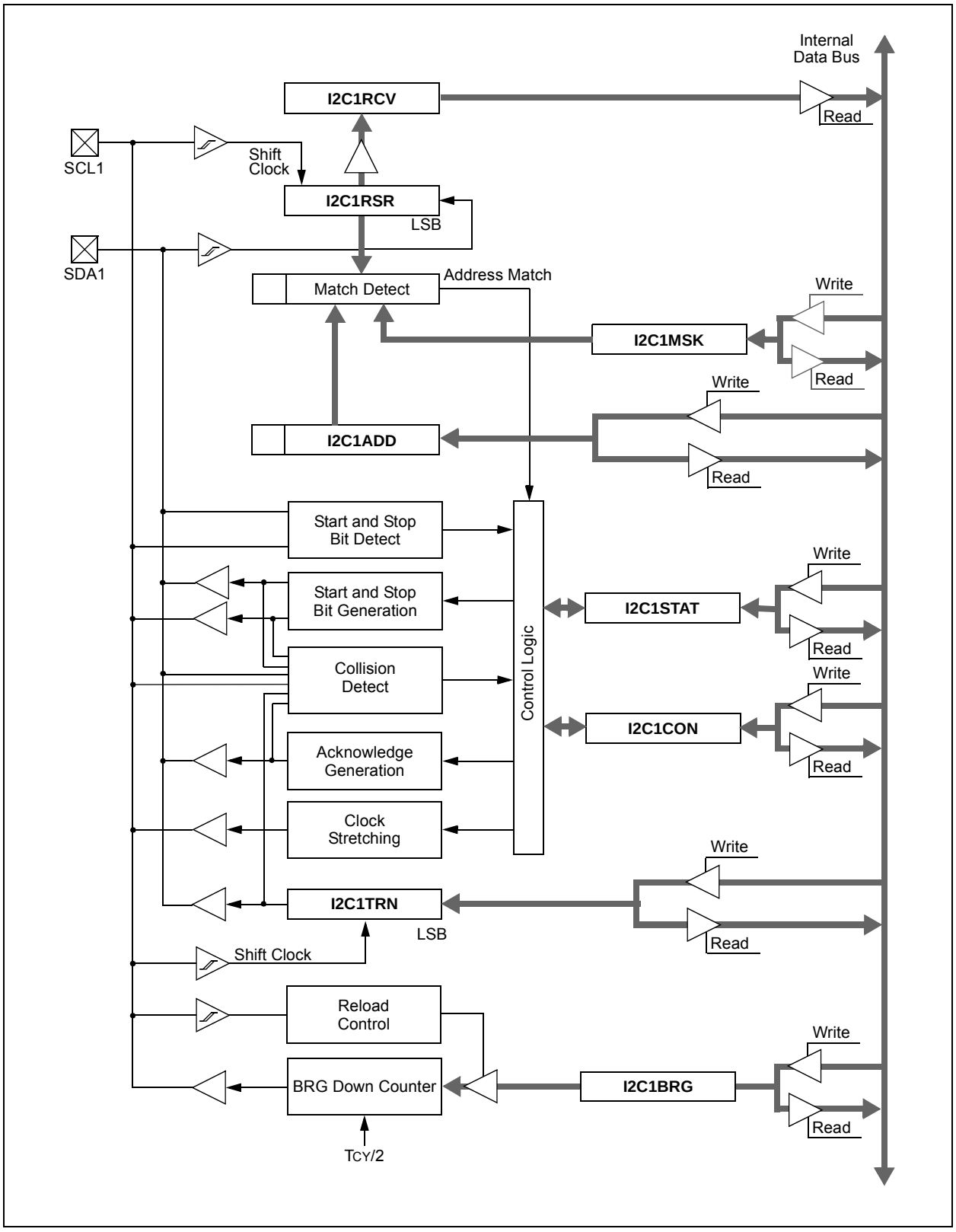
bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-0 **Unimplemented:** Read as '0'

NOTES:

FIGURE 17-1: I²C™ BLOCK DIAGRAM



19.2.4 RTCC CONTROL REGISTERS

REGISTER 19-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1)

R/W-0	U-0	R/W-0	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0
RTCEN(2)	—	RTCWREN	RTCSYNC	HALFSEC(3)	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVALH and RTCVALL registers can be written to by the user
0 = RTCVALH and RTCVALL registers are locked out from being written to by the user

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading due to a rollover ripple, resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = RTCVALH, RTCVALL or ALCFGRPT registers can be read without concern over a rollover ripple

bit 11 **HALFSEC:** Half Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
Points to the corresponding RTCC Value registers when reading the RTCVALH and RTCVALL registers. The RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'.
RTCVAL<15:8>:
00 = MINUTES
01 = WEEKDAY
10 = MONTH
11 = Reserved
RTCVAL<7:0>:
00 = SECONDS
01 = HOURS
10 = DAY
11 = YEAR

Note 1: The RCFGCAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

REGISTER 19-3: ALCFGRPT: ALARM CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 00h and CHIME = 0)

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 00h to FFh

0 = Chime is disabled; ARPT<7:0> bits stop once they reach 00h

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits

0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every 4 years)
101x = Reserved – do not use
11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers. The ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches '00'.

ALRMVAL<15:8>:
00 = ALRMMIN
01 = ALRMWD
10 = ALRMMNTH
11 = Unimplemented

ALRMVAL<7:0>:
00 = ALRMSEC
01 = ALRMHR
10 = ALRMDAY
11 = Unimplemented

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits

11111111 = Alarm will repeat 255 more times
.
.
.
00000000 = Alarm will not repeat

The counter decrements on any alarm event; it is prevented from rolling over from 00h to FFh unless CHIME = 1.

REGISTER 20-2: CRCXOR: CRC XOR POLYNOMIAL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X15	X14	X13	X12	X11	X10	X9	X8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X7	X6	X5	X4	X3	X2	X1	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **X<15:1>:** XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 21-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit
1 = HLVD is enabled
0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit
1 = Indicates that the band gap voltage is stable
0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Indicates that the internal reference voltage is stable and the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
0 = Indicates that the internal reference voltage is unstable and the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits
1111 = External analog input is used (input comes from the HLVDIN pin)
1110 = Trip Point 1(1)
1101 = Trip Point 2(1)
1100 = Trip Point 3(1)
.
.
.
0000 = Trip Point 15(1)

Note 1: For actual trip point, refer to **Section 29.0 "Electrical Characteristics"**.

TABLE 29-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE): Core Off, Clock on Base Current, PMD Bits are Set(2)						
DC50	2	18	μA	-40°C	1.8V	LPRC (31 kHz)
DC50a		18		+25°C		
DC50b		18		+60°C		
DC50c		18		+85°C		
DC50d	4	40		-40°C	3.3V	
DC50e		40		+25°C		
DC50f		40		+60°C		
DC50g		40		+85°C		
DC50h		60		+125°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:
- Core is off
- EC mode with the clock input driven with a square wave rail-to-rail
- I/Os are configured as outputs, driven low
- $\overline{MCLR}$ – VDD
- WDT FSCM are disabled
- SRAM, program and data memory are active
- All PMD bits are set except for the modules being measured

TABLE 29-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(4)**	—	—	—	—	
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		OSCI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSCI (HS mode)	VSS	—	0.2 VDD	V	
DI18		I/O Pins with I2C™ Buffer	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SMBus Buffer	VSS	—	0.8	V	SMBus enabled
	VIH(5)	**Input High Voltage(4)**	—	—	—	—	
DI20		I/O Pins:					
		with Analog Functions	0.8 VDD	—	VDD	V	
		Digital Only	0.8 VDD	—	VDD	V	
DI25		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI28		I/O Pins with I2C Buffer:					
		with Analog Functions	0.7 VDD	—	VDD	V	
		Digital Only	0.7 VDD	—	VDD	V	
DI29		I/O Pins with SMBus	2.1	—	VDD	V	2.5V ≤ VPIN ≤ VDD
DI30	ICNPU	**CNx Pull-up Current**	50	250	500	μA	VDD = 3.3V, VPIN = VSS
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Ports	—	0.050	±0.100	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		VREF+, VREF-, AN0, AN1	—	0.300	±0.500	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	—	±5.0	μA	VSS ≤ VPIN ≤ VDD
DI56		OSCI	—	—	±5.0	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-2 for I/O pin buffer types.

5: VIH requirements are met when internal pull-ups are enabled.

TABLE 29-22: AC SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Units
TLW	BCLKx High Time	20	TCY/2	—	ns
THW	BCLKx Low Time	20	(TCY * BRGx) + TCY/2	—	ns
TBLD	BCLKx Falling Edge Delay from UxTX	-50	—	50	ns
TBHD	BCLKx Rising Edge Delay from UxTX	TCY/2 – 50	—	TCY/2 + 50	ns
TWAK	Min. Low on UxRX Line to Cause Wake-up	—	1	—	µs
TCTS	Min. Low on $\overline{\text{UxCTS}}$ Line to Start Transmission	TCY	—	—	ns
TSETUP	Start bit Falling Edge to System Clock Rising Edge Setup Time	3	—	—	ns
TSTDELAY	Maximum Delay in the Detection of the Start bit Falling Edge	—	—	TCY + TSETUP	ns

TABLE 29-23: A/D CONVERSION TIMING REQUIREMENTS(1)

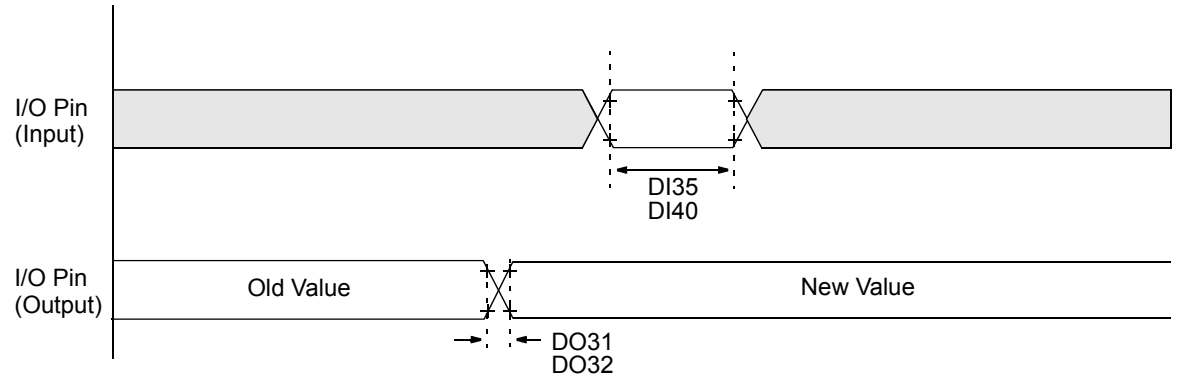
A/D CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	A/D Clock Period	75	—	—	ns	TCY = 75 ns, AD1CON3 is in the default state
AD51	TRC	A/D Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	TCONV	Conversion Time	—	12	—	TAD	
AD56	FCNV	Throughput Rate	—	—	500	ksps	AVDD ≥ 2.7V
AD57	TSAMP	Sample Time	—	1	—	TAD	
AD58	TACQ	Acquisition Time	750	—	—	ns	**(Note 2)**
AD59	TSWC	Switching Time from Convert to Sample	—	—	**(Note 3)**		
AD60	TDIS	Discharge Time	0.5	—	—	TAD	
Clock Parameters							
AD61	TPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

2: The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD).

3: On the following cycle of the device clock.

FIGURE 29-6: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 29-4 for load conditions.

TABLE 29-25: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx pin High or Low Time (output)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

FIGURE 29-20: SPIx MODULE SLAVE MODE TIMING CHARACTERISTICS (CKE = 1)

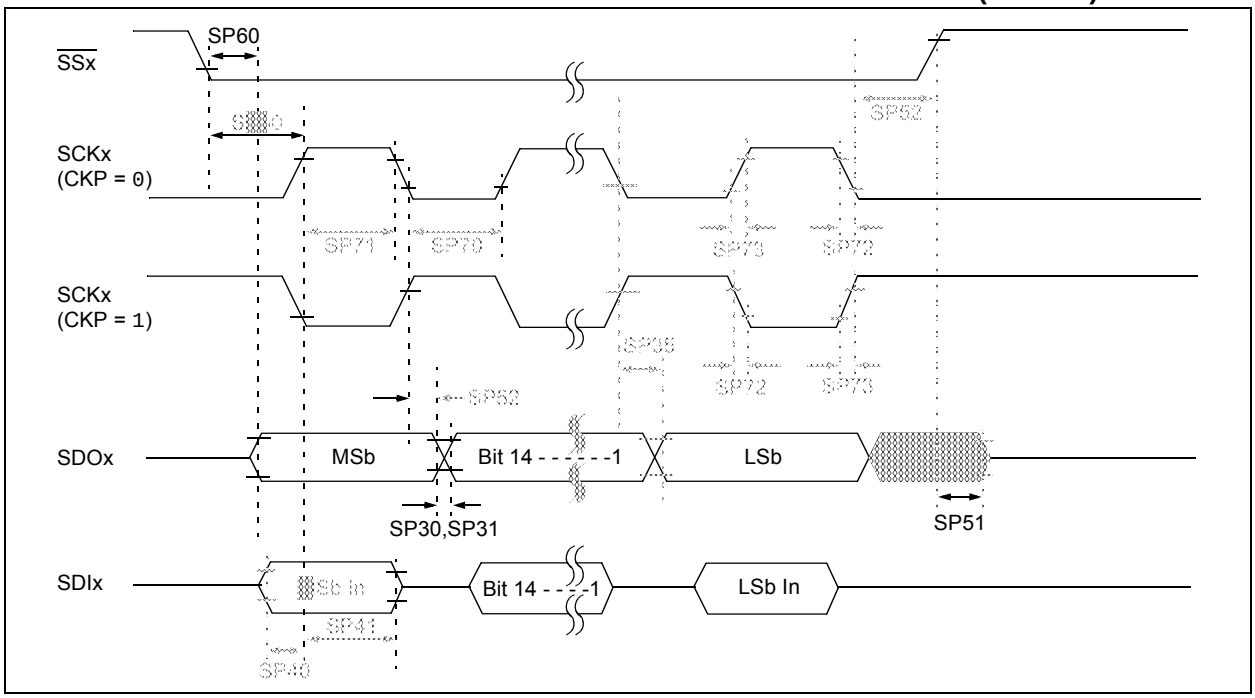


TABLE 29-39: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS (CKE = 1)

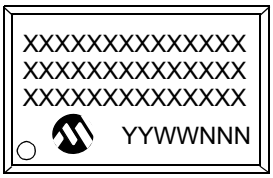
AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time(2)	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time(2)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(2)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(2)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	50	ns	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

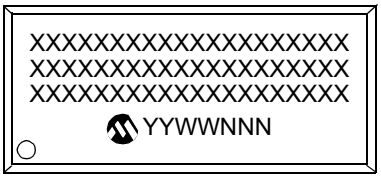
3: Assumes 50 pF load on all SPIx pins.

20-Lead SOIC (.300”)

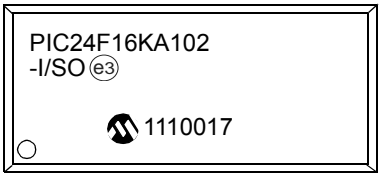


Example

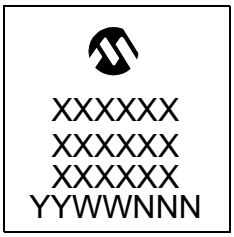
28-Lead SOIC (.300”)



Example

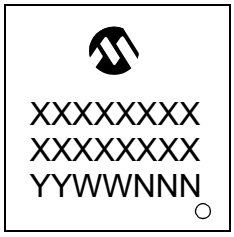


20-Lead QFN



Example

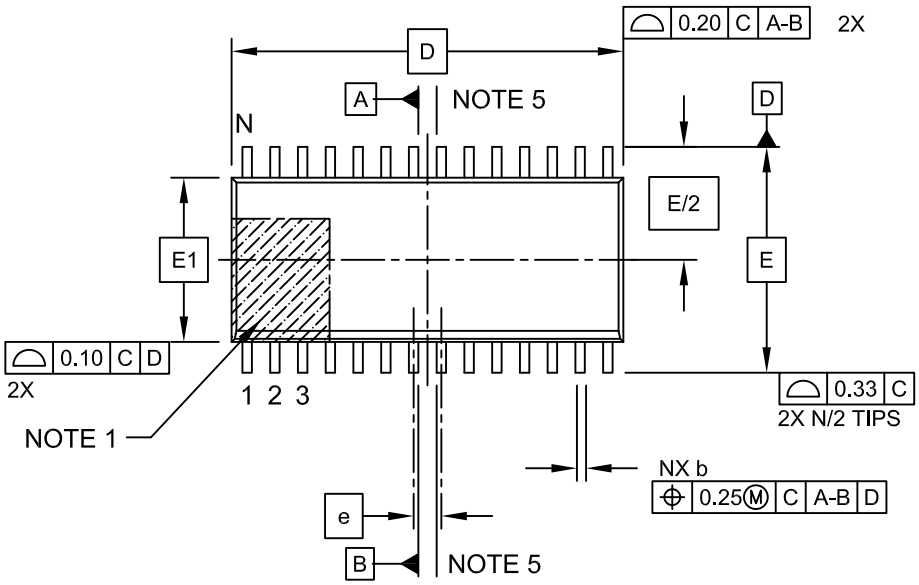
28-Lead QFN



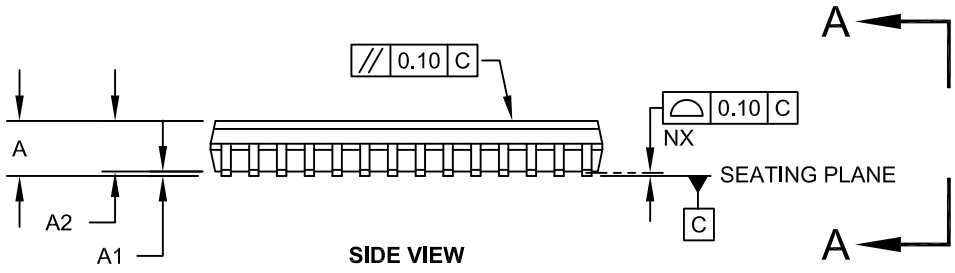
Example

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

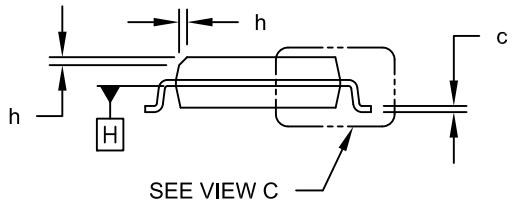
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

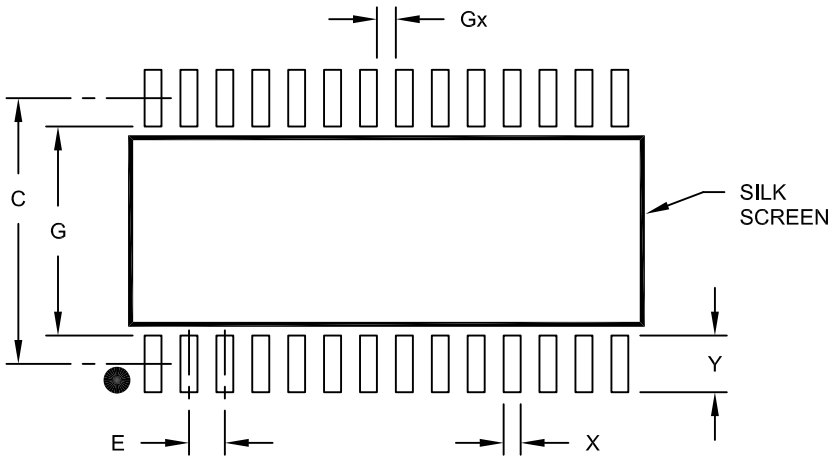


VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

APPENDIX A: REVISION HISTORY

Revision A (November 2008)

Original data sheet for the PIC24F16KA102 family of devices.

Revision B (March 2009)

Section 29.0 "Electrical Characteristics" was revised and minor text edits were made throughout the document.

Revision C (October 2011)

- Changed all instances of DSWSRC to DSWAKE.
- Corrected Example 5-2.
- Corrected Example 5-4.
- Corrected Example 6-1.
- Corrected Example 6-3.
- Added a comment to Example 6-5.
- Corrected Figure 9-1 to connect the SOSCI and SOSCO pins to the Schmitt trigger correctly.
- Added register descriptions for PMD1, PMD2, PMD3 and PMD4.
- Added note that RTCC will run in Reset.
- Corrected time values of ADCS (AD1CON3<5:0>).
- Corrected CH0SB and CH0SA (AD1CHS<11:8> and AD1CHS<3:0>) to correctly reference AVDD and AN3.
- Added description of PGCF15 and PGCF14 (AD1PCFG<15:14>).
- Edited Figure 22-2 to correctly reference RIC and the A/D capacitance.
- Changed all references from CTEDG1 to CTED1.
- Changed all references from CTEDG2 to CTED2.
- Changed description of CMIDL: it used to say it disables all comparators in Idle, now only disables interrupts in Idle mode.
- Changed all references of RTCCKSEL to RTCOSC.
- Changed all references of DSLPBOR to DSBOREN.
- Changed all references of DSWCKSEL to DSWDTOSC
- Imported Figure 40-9 from PIC24F FRM, Section 40.
- Added spec for BOR hysteresis.
- Edited Note 1 for Table 29-5 to further describe LPBOR.
- Edited max values of DC20d and DC20e on Table 29-6.
- Edited typical value for DC61-DC61c in Table 29-8.
- Edited Note 2 of Table 29-8.
- Added Note 5 to Table 29-9.
- Added Table 29-15.
- Added AD08 and AD09 in Table 29-26.
- Added Note 3 to Table 29-26.
- Imported Figure 40.10 from PIC24F FRM, Section 40.
- Deleted TVREG spec.
- Imported Figure 15-5 from PIC24F FRM, Section 15.
- Imported Table 15-4 from PIC24F FRM, Section 15.
- Imported Figure 16-22 from PIC24F FRM, Section 16.
- Imported Table 16-9 from PIC24F FRM, Section 16.
- Imported Figure 16-23 from PIC24F FRM, Section 16.
- Imported Table 16-10 from PIC24F FRM, Section 16.
- Imported Figure 21-24 from PIC24F FRM. Section 21.
- Imported Figure 21-25 from PIC24F FRM, Section 21.
- Imported Table 21-5 from PIC24F FRM, Section 21.
- Imported Figure 23-17 from PIC24F FRM, Section 23.
- Imported Table 23-3 from PIC24F FRM, Section 23.
- Imported Figure 23-18 from PIC24F FRM, Section 23.
- Imported Table 23-4 from PIC24F FRM, Section 23.
- Imported Figure 23-19 from PIC24F FRM, Section 23.
- Imported Table 23-5 from PIC24F FRM, Section 23.
- Imported Figure 23-20 from PIC24F FRM, Section 23.
- Imported Table 23-6 from PIC24F FRM, Section 23.
- Imported Figure 24-33 from PIC24F FRM, Section 24.
- Imported Table 24-6 from PIC24F FRM, Section 24.
- Imported Figure 24-34 from PIC24F FRM, Section 24.
- Imported Table 24-7 from PIC24F FRM, Section 24.
- Imported Figure 24-35 from PIC24F FRM, Section 24.
- Imported Table 24-8 from PIC24F FRM, Section 24.
- Imported Figure 24-36 from PIC24F FRM, Section 24.
- Imported Table 24-9 from PIC24F FRM, Section 24.

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