Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

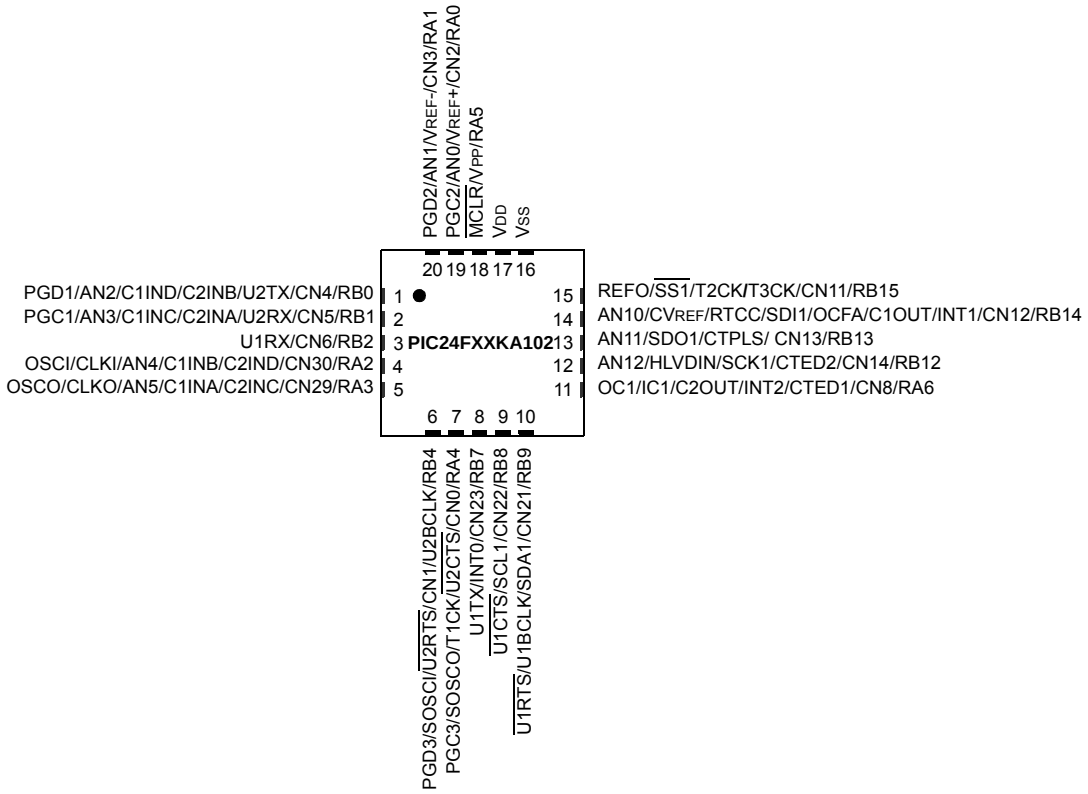
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08ka102t-i-ss

Pin Diagrams (Continued)

20-Pin QFN(1,2)



Note 1: The bottom pad of the QFN package should be connected to VSS.

2: All device pins have a maximum voltage of 3.6V and are not 5V tolerant.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24F16KA102 family family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 “Power Supply Pins”**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 “Power Supply Pins”**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 “Master Clear (MCLR) Pin”**)
- VCAP pins
  (see **Section 2.4 “Voltage Regulator Pin (VCAP)”**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 “ICSP Pins”**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.6 “External Oscillator Pins”**)

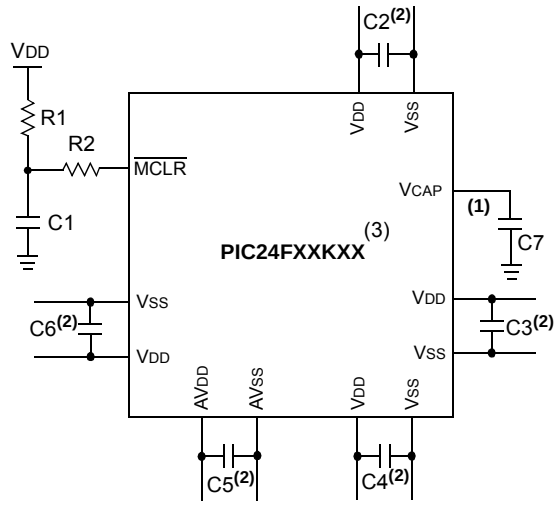
Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

Note:	The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 μF, 20V ceramic

C7: 10 μF, 16V tantalum or ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note 1: See **Section 2.4 “Voltage Regulator Pin (VCAP)”** for explanation of VCAP pin connections.

2: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

3: Some PIC24F K parts do not have a regulator.

3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the *"PIC24F Family Reference Manual"*, **Section 2. "CPU"** (DS39703).

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `REPEAT` instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K word boundary of either program memory or data EEPROM memory defined by the 8-bit Program Space Visibility Page Address (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct and three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (that is, A + B = C) to be executed in a single cycle.

A high-speed, 17-bit by 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit by 16-bit or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the `REPEAT` instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is illustrated in Figure 3-1.

3.1 Programmer's Model

Figure 3-2 displays the programmer's model for the PIC24F. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions.

Table 3-1 provides a description of each register. All registers associated with the programmer's model are memory mapped.

TABLE 4-3: CPU CORE REGISTERS MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0000	Working Register 0																0000
WREG1	0002	Working Register 1																0000
WREG2	0004	Working Register 2																0000
WREG3	0006	Working Register 3																0000
WREG4	0008	Working Register 4																0000
WREG5	000A	Working Register 5																0000
WREG6	000C	Working Register 6																0000
WREG7	000E	Working Register 7																0000
WREG8	0010	Working Register 8																0000
WREG9	0012	Working Register 9																0000
WREG10	0014	Working Register 10																0000
WREG11	0016	Working Register 11																0000
WREG12	0018	Working Register 12																0000
WREG13	001A	Working Register 13																0000
WREG14	001C	Working Register 14																0000
WREG15	001E	Working Register 15																0800
SPLIM	0020	Stack Pointer Limit Value Register																xxxx
PCL	002E	Program Counter Low Byte Register																0000
PCH	0030	—	—	—	—	—	—	—	—	Program Counter Register High Byte								0000
TBLPAG	0032	—	—	—	—	—	—	—	—	Table Memory Page Address Register								0000
PSVPAG	0034	—	—	—	—	—	—	—	—	Program Space Visibility Page Address Register								0000
RCOUNT	0036	REPEAT Loop Counter Register																xxxx
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	0044	—	—	—	—	—	—	—	—	—	—	—	—	IPL3	PSV	—	—	0000
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxx

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0, HC	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	PGMONLY(4)	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ERASE	NVMOP5(1)	NVMOP4(1)	NVMOP3(1)	NVMOP2(1)	NVMOP1(1)	NVMOP0(1)
bit 7							bit 0

Legend:	SO = Settable Only bit	HC = Hardware Clearable bit	
-n = Value at POR	'1' = Bit is set	R = Readable bit	W = Writable bit
'0' = Bit is cleared	x = Bit is unknown	U = Unimplemented bit, read as '0'	

bit 15 **WR:** Write Control bit
- 1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit
- 1 = Enable Flash program/erase operations
- 0 = Inhibit Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit
- 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **PGMONLY:** Program Only Enable bit(4)

bit 11-7 **Unimplemented:** Read as '0'

bit 6 **ERASE:** Erase/Program Enable bit
- 1 = Perform the erase operation specified by NVMOP<5:0> on the next WR command
- 0 = Perform the program operation specified by NVMOP<5:0> on the next WR command

bit 5-0 **NVMOP<5:0>:** Programming Operation Command Byte bits(1)

Erase Operations (when ERASE bit is '1'):
- 1010xx = Erase entire boot block (including code-protected boot block)(2)
- 1001xx = Erase entire memory (including boot block, configuration block, general block)(2)
- 011010 = Erase 4 rows of Flash memory(3)
- 011001 = Erase 2 rows of Flash memory(3)
- 011000 = Erase 1 row of Flash memory(3)
- 0101xx = Erase entire configuration block (except code protection bits)
- 0100xx = Erase entire data EEPROM(4)
- 0011xx = Erase entire general memory block programming operations
- 0001xx = Write 1 row of Flash memory (when ERASE bit is '0')(3)

Note 1: All other combinations of NVMOP<5:0> are no operation.

2: Available in ICSP™ mode only. Refer to device programming specification.

3: The address in the Table Pointer decides which rows will be erased.

4: This bit is used only while accessing data EEPROM.

EXAMPLE 5-5: INITIATING A PROGRAMMING SEQUENCE – ASSEMBLY LANGUAGE CODE

```
        DISI    #5                      ; Block all interrupts
                                          for next 5 instructions
        MOV     #0x55, W0
        MOV     W0, NVMKEY              ; Write the 55 key
        MOV     #0xAA, W1               ;
        MOV     W1, NVMKEY              ; Write the AA key
        BSET    NVMCON, #WR             ; Start the erase sequence
        NOP                             ; 2 NOPs required after setting WR
        NOP                             ;
        BTSC    NVMCON, #15             ; Wait for the sequence to be completed
        BRA     $-2                     ;
```

EXAMPLE 5-6: INITIATING A PROGRAMMING SEQUENCE – 'C' LANGUAGE CODE

```
// C example using MPLAB C30

asm("DISI #5");               // Block all interrupts for next 5 instructions

__builtin_write_NVM();        // Perform unlock sequence and set WR
```

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER2

R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Use Alternate Interrupt Vector Table
0 = Use standard (default) vector table

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as '0'

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 8-12: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
—	—	CTMUIE	—	—	—	—	HLVDIE
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
—	—	—	—	CRCIE	U2ERIE	U1ERIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3 **CRCIE:** CRC Generator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 8-19: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enabled bit
If FSCM is enabled (FCKSM1 = 1):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
If FSCM is disabled (FCKSM1 = 0):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **Unimplemented:** Read as '0'

bit 5 **LOCK:** PLL Lock Status bit(2)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** 32 kHz Secondary Oscillator (SOSC) Enable bit
1 = Enable secondary oscillator
0 = Disable secondary oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Initiate an oscillator switch to clock source specified by NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Reset values for these bits are determined by the FNOSC Configuration bits.
2: Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5(1)	TUN4(1)	TUN3(1)	TUN2(1)	TUN1(1)	TUN0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

011111 = Maximum frequency deviation
011110
.
.
.
000001
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111
.
.
.
100001
100000 = Minimum frequency deviation

Note 1: Increments or decrements of TUN<5:0> may not change the FRC frequency in equal steps over the FRC tuning range and may not be monotonic.

NOTES:

15.4 Output Compare Register

REGISTER 15-1: OC1CON: OUTPUT COMPARE 1 CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL	OCM2	OCM1	OCM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Stop Output Compare 1 in Idle Mode Control bit
1 = Output Compare 1 will halt in CPU Idle mode
0 = Output Compare 1 will continue to operate in CPU Idle mode

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **OCFLT:** PWM Fault Condition Status bit
1 = PWM Fault condition has occurred (cleared in HW only)
0 = No PWM Fault condition has occurred (this bit is only used when OCM<2:0> = 111)

bit 3 **OCTSEL:** Output Compare 1 Timer Select bit
1 = Timer3 is the clock source for Output Compare 1
0 = Timer2 is the clock source for Output Compare 1
Refer to the device data sheet for specific time bases available to the output compare module.

bit 2-0 **OCM<2:0>:** Output Compare 1 Mode Select bits
111 = PWM mode on OC1, Fault pin; OCF1 enabled(1)
110 = PWM mode on OC1, Fault pin; OCF1 disabled(1)
101 = Initialize OC1 pin low, generate continuous output pulses on OC1 pin
100 = Initialize OC1 pin low, generate single output pulse on OC1 pin
011 = Compare event toggles OC1 pin
010 = Initialize OC1 pin high, compare event forces OC1 pin low
001 = Initialize OC1 pin low, compare event forces OC1 pin high
000 = Output compare channel is disabled

Note 1: The OCFA pin controls the OC1 channel.

23.0 COMPARATOR MODULE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator module, refer to the *"PIC24F Family Reference Manual"*, **Section 46. "Scalable Comparator Module"** (DS39734).

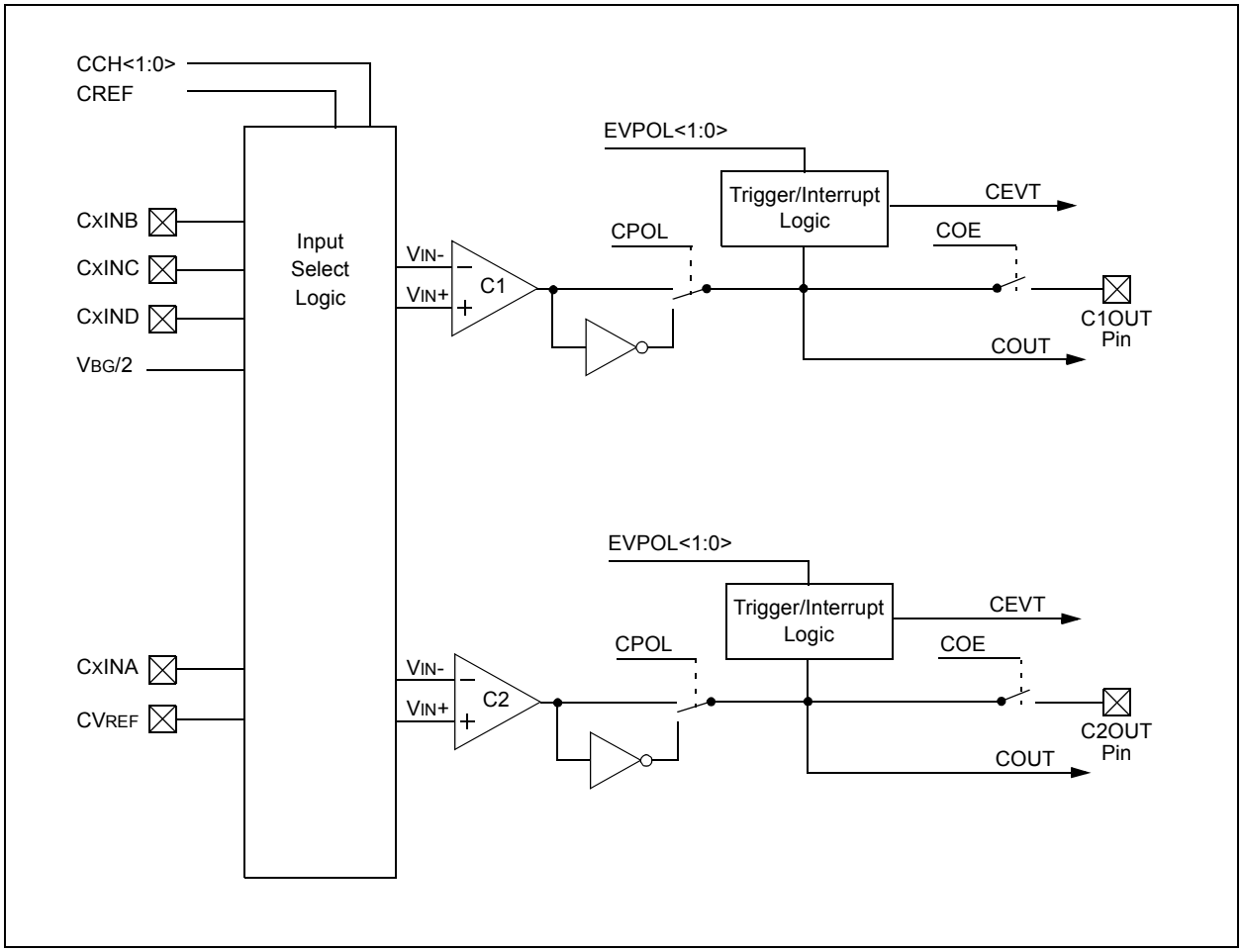
The comparator module provides two dual input comparators. The inputs to the comparator can be configured to use any one of four external analog inputs, as well as a voltage reference input from either the internal band gap reference, divided by 2 ($V_{BG}/2$), or the comparator voltage reference generator.

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is displayed in Figure 23-1. Diagrams of the possible individual comparator configurations are displayed in Figure 23-2.

Each comparator has its own control register, CMxCON (Register 23-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 23-2).

FIGURE 23-1: COMPARATOR MODULE BLOCK DIAGRAM



REGISTER 23-1: CMxCON: COMPARATOR x CONTROL REGISTERS (CONTINUED)

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)
1 = Non-inverting input connects to the internal CV_{REF} voltage
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = Inverting input of comparator connects to $V_{BG}/2$
10 = Inverting input of comparator connects to CxIND pin
01 = Inverting input of comparator connects to CxINC pin
00 = Inverting input of comparator connects to CxINB pin

REGISTER 23-2: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	—	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
—	—	—	—	—	—	C2OUT	C1OUT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL:** Comparator Stop in Idle Mode bit
1 = Disable comparator interrupts when the device enters Idle mode; the module is still enabled
0 = Continue operation of all enabled comparators in Idle mode

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 8 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

REGISTER 26-8: FDS: DEEP SLEEP CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
DSWDTEN	DSBOREN	RTCOSC	DSWDTOSC	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
1 = DSWDT is enabled
0 = DSWDT is disabled

bit 6 **DSBOREN:** Deep Sleep/Low-Power BOR Enable bit (does not affect operation in non Deep Sleep modes)
1 = Deep Sleep BOR is enabled in Deep Sleep
0 = Deep Sleep BOR is disabled in Deep Sleep

bit 5 **RTCOSC:** RTCC Reference Clock Select bit
1 = RTCC uses SOSC as a reference clock
0 = RTCC uses LPRC as a reference clock

bit 4 **DSWDTOSC:** DSWDT Reference Clock Select bit
1 = DSWDT uses LPRC as a reference clock
0 = DSWDT uses SOSC as a reference clock

bit 3-0 **DSWDTPS<3:0>:** Deep Sleep Watchdog Timer Postscale Select bits
The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms.
1111 = 1:2,147,483,648 (25.7 days) nominal
1110 = 1:536,870,912 (6.4 days) nominal
1101 = 1:134,217,728 (38.5 hours) nominal
1100 = 1:33,554,432 (9.6 hours) nominal
1011 = 1:8,388,608 (2.4 hours) nominal
1010 = 1:2,097,152 (36 minutes) nominal
1001 = 1:524,288 (9 minutes) nominal
1000 = 1:131,072 (135 seconds) nominal
0111 = 1:32,768 (34 seconds) nominal
0110 = 1:8,192 (8.5 seconds) nominal
0101 = 1:2,048 (2.1 seconds) nominal
0100 = 1:512 (528 ms) nominal
0011 = 1:128 (132 ms) nominal
0010 = 1:32 (33 ms) nominal
0001 = 1:8 (8.3 ms) nominal
0000 = 1:2 (2.1 ms) nominal

TABLE 29-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**	
IDD Current(2)					
DC31	8	28	μA	-40°C	1.8V, LPRC (31 kHz)
DC31a		28		+25°C	
DC31b		28		+60°C	
DC31c		28		+85°C	
DC31d	15	55	μA	-40°C	3.3V, LPRC (31 kHz)
DC31e		55		+25°C	
DC31f		55		+60°C	
DC31g		55		+85°C	
DC31h		250		+125°C	

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:
- EC mode with clock input driven with a square wave rail-to-rail
- I/Os are configured as outputs, driven low
- $\overline{MCLR}$ – VDD
- WDT FSCM is disabled
- SRAM, program and data memory are active
- All PMD bits are set except for modules being measured

TABLE 29-24: A/D MODULE SPECIFICATIONS

A/D CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 1.8	—	Lesser of VDD + 0.3 or 3.6	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.7	—	AVDD	V	
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 1.7	V	
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD08	IVREF	Reference Voltage Input Current	—	—	200	μA	VREF+ = 3.3V; sampling
			—	—	1.0	mA	VREF+ = 3.3V; converting
AD09	ZVREF	Reference Input Impedance	—	10K	—	Ω	**(Note 3)**
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	**(Note 2)**
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3		AVDD/2	V	
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	2.5K	Ω	10-bit
A/D Accuracy							
AD20b	NR	Resolution	—	10	—	bits	
AD21b	INL	Integral Nonlinearity	—	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD22b	DNL	Differential Nonlinearity	—	±1	-1 +1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD23b	GERR	Gain Error	—	±1	±3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD24b	EOFF	Offset Error	—	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD25b		Monotonicity	—	—	—	—	**(Note 1)**

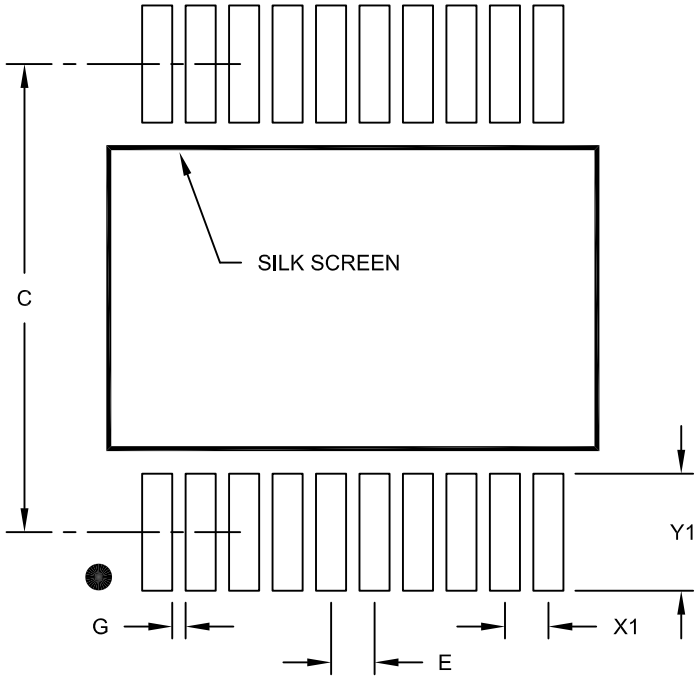
Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: Measurements are taken with external VREF+ and VREF- used as the A/D voltage reference.

3: Impedance during sampling is at 3.3V, 25°C. This parameter is for design guidance only and is not tested.

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

IPC2 (Interrupt Priority Control 2) 81
IPC3 (Interrupt Priority Control 3) 82
IPC4 (Interrupt Priority Control 4) 83
IPC5 (Interrupt Priority Control 5) 84
IPC7 (Interrupt Priority Control 7) 85
MINSEC (RTCC Minutes and Seconds Value) 161
MTHDY (RTCC Month and Day Value) 160
NVMCON (Flash Memory Control) 47
NVMCON (Nonvolatile Memory Control) 52
OC1CON (Output Compare 1 Control) 129
OSCCON (Oscillator Control) 93
OSCTUN (FRC Oscillator Tune) 96
PADCFG1 (Pad Configuration Control) 130, 146, 158
PMD1 (Peripheral Module Disable 1) 108
PMD2 (Peripheral Module Disable 2) 109
PMD3 (Peripheral Module Disable 3) 110
PMD4 (Peripheral Module Disable 4) 111
RCFGCAL (RTCC Calibration and Configuration) 157
RCON (Reset Control) 58
REFOCON (Reference Oscillator Control) 99
SPI1CON1 (SPI1 Control 1) 136
SPI1CON2 (SPI1 Control 2) 137
SPI1STAT (SPI1 Status and Control) 134
SR (ALU STATUS) 26, 67
T1CON (Timer1 Control) 116
T2CON (Timer2 Control) 120
T3CON (Timer3 Control) 121
UxMODE (UARTx Mode) 150
UxRXREG (UARTx Receive) 154
UxSTA (UARTx Status and Control) 152
UxTXREG (UARTx Transmit) 154
WKDYHR (RTCC Weekday and Hours Value) 161
YEAR (RTCC Year Value) 160

Resets
Clock Source Selection 60
Delay Times for Various Device Resets 60
Device Times 60
RCON Flags Operation 59
SFR States 61
Revision History 269
RTCC 155
Alarm Configuration 164
Alarm Mask Settings (figure) 165
Calibration 164
Register Mapping 156
Source Clock 155
Selection 156
Write Lock 156

S

Selective Peripheral Power Control 107
Serial Peripheral Interface. *See* SPI.
SFR Space 32
Software Simulator (MPLAB SIM) 205
Software Stack 41

T

Timer1 115
Timer2/3 117
Timing Diagrams
Baud Rate Generator Output 239, 240
Brown-out Reset Characteristics 219
CLKO and I/O Timing 236
External Clock 232
I^2C Bus Data (Master Mode) 240
I^2C Bus Data (Slave Mode) 242
I^2C Bus Start/Stop Bits (Master Mode) 240
I^2C Bus Start/Stop Bits (Slave Mode) 242
Input Capture 244
Output Compare 244
PWM Requirements 245
Reset, Watchdog Timer. Oscillator Start-up Timer, Power-up Timer Characteristics 238
SPIx Master Mode (CKE = 0) 246
SPIx Master Mode (CKE = 1) 247
SPIx Slave Mode (CKE = 0) 248
SPIx Slave Mode (CKE = 1) 249
Start Bit Edge Detection 243
Timing Requirements
CLKO and I/O 236
External Clock 232
I^2C Bus Data (Master Mode) 240, 241
I^2C Bus Data (Slave Mode) 243
I^2C Bus Start/Stop Bit (Slave Mode) 242
PLL Clock Specifications 233
PWM 245
SPIx Master Mode (CKE = 0) 246
SPIx Master Mode (CKE = 1) 247
SPIx Slave Mode (CKE = 0) 248
SPIx Slave Mode (CKE = 1) 249

U

UART 147
Baud Rate Generator (BRG) 148
Break and Sync Transmit Sequence 149
IrDA Support 149
Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins 149
Receiving in 8-Bit or 9-Bit Data Mode 149
Transmitting in 8-Bit Data Mode 149
Transmitting in 9-Bit Data Mode 149

W

Watchdog Timer
Deep Sleep (DSWDT) 202
Watchdog Timer (WDT) 201
Windowed Operation 201
WWW Address 275
WWW, On-Line Support 8