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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1.5K × 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16ka102-e-so

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Read	ler Kesponse	
Prod	uct Identification System	

20-Pin PDIP/SSOP/SOIC/QFN 28-Pin SPDIP/SSOP/SOIC/QFN

TABLE 1-1:       DEVICE FEATURES FOR THE PIC24F16KA102 FAMILY							
Features	PIC24F08KA101	PIC24F16KA101	PIC24F08KA102	PIC24F16KA102			
Operating Frequency		DC – 3	32 MHz				
Program Memory (bytes)	8K	16K	8K	16K			
Program Memory (instructions)	2816	5632	2816	5632			
Data Memory (bytes)		15	36				
Data EEPROM Memory (bytes)		5	12				
Interrupt Sources (soft vectors/NMI traps)		30 (2	26/4)				
I/O Ports	PORT/ PORTB<15:1	A<6:0> 2, 9:7, 4, 2:0>	PORTA<7:0> PORTB<15:0>				
Total I/O Pins	18 24						
Timers: Total Number (16-bit) 32-Bit (from paired 16-bit timers)			3 1				
Input Capture Channels			1				
Output Compare/PWM Channels			1				
Input Change Notification Interrupt	17 23						
Serial Communications: UART SPI (3-wire/4-wire) I <sup>2</sup> C™		-	2 1 1				
10-Bit Analog-to-Digital Module (input channels)	9						
Analog Comparators			2				
Resets (and delays)	POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)						
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations						

Packages

### 2.2 Power Supply Pins

### 2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1  $\mu$ F (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu$ F to 0.001  $\mu$ F. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1  $\mu$ F in parallel with 0.001  $\mu$ F).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

### 2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7  $\mu$ F to 47  $\mu$ F.

# 2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the  $\overline{\text{MCLR}}$  pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the  $\overline{\text{MCLR}}$  pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the  $\overline{\text{MCLR}}$  pin should be placed within 0.25 inch (6 mm) of the pin.

### FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Overstress (EOS). Ensure that the MCLR pin

VIH and VIL specifications are met.

### REGISTER 8-15: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	<u>U-0</u>	R/W-1	R/W-0	R/W-0
	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	SPF1IP2	SPF1IP1	SPF1IP0		T3IP2	T3IP1	T3IP0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value a	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	כ'				
bit 14-12	U1RXIP<2:0>	-: UART1 Rece	iver Interrupt I	Priority bits			
	111 = Interru	pt is Priority 7(	highest priority	v interrupt)			
	•						
	•						
	001 = Interru	pt is Priority 1					
	000 = Interru	pt source is dis	abled				
bit 11	Unimplemen	ted: Read as '	כי				
bit 10-8	SPI1IP<2:0>:	SPI1 Event In	terrupt Priority	bits			
	111 = Interru	pt is Priority 7 (	highest priority	/ interrupt)			
	•						
	•						
	001 = Interru	pt is Priority 1					
	000 = Interru	pt source is dis	abled				
bit 7	Unimplemen	ted: Read as '	כ'				
bit 6-4	SPF1IP<2:0>	: SPI1 Fault In	terrupt Priority	bits			
	111 = Interru	pt is Priority 7 (	highest priority	interrupt)			
	•						
	•						
	001 = Interru	pt is Priority 1					
	000 = Interru	pt source is dis	abled				
bit 3	Unimplemen	ted: Read as '	כי				
bit 2-0	T3IP<2:0>: ⊺	imer3 Interrupt	Priority bits				
	111 = Interru	pt is Priority 7 (	highest priority	interrupt)			
	•						
	•						
	001 = Interru	pt is Prioritv 1					
	000 = Interru	pt source is dis	abled				

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0	
_	—	_	_	—	RTCIP2	RTCIP1	RTCIP0	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	—	—	—		—	—	
bit 7							bit 0	
Legend:								
R = Readab	le bit	W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-11	Unimplemen	ted: Read as '	0'					
bit 10-8	RTCIP<2:0>:	Real-Time Clo	ck and Calend	lar Interrupt Prie	ority bits			
	111 = Interru	pt is Priority 7 (	highest priority	interrupt)				
	•							
	•							
•								
	001 = Interru	pt is Priority 1						
	000 = Interru	pt source is dis	abled					
bit 7-0	Unimplemen	ted: Read as '	0'					

### REGISTER 8-20: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15

### 9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMDx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

### 9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 26.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled; this is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

#### 9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

- 1. If desired, read the COSCx bits (OSCCON<14:12>), to determine the current oscillator source.
- 2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
- 3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
- 4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
- 5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

- 1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
- If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
- The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
- 4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
- 5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
- The old clock source is turned off at this time, with the exception of LPRC (if WDT, FSCM or RTCC with LPRC as clock source are enabled) or SOSC (if SOSCEN remains enabled).

Note 1: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

# 10.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not								
	intended to be a comprehensive reference								
	source. For more information, refer to the								
	"PIC24F Family Reference Manual",								
	"Section 39. Power-Saving Features								
	with Deep Sleep" (DS39727).								

The PIC24F16KA102 family of devices provides the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. All PIC24F devices manage power consumption in four different ways:

- Clock frequency
- Instruction-based Sleep, Idle and Deep Sleep modes
- Software controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical application features, such as timing-sensitive communications.

### 10.1 Clock Frequency and Clock Switching

PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0** "Oscillator Configuration".

### 10.2 Instruction-Based Power-Saving Modes

PIC24F devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution; Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. Deep Sleep mode stops clock operation, code execution and all peripherals except RTCC and DSWDT. It also freezes I/O states and removes power to SRAM and Flash memory. The assembly syntax of the PWRSAV instruction is shown in Example 10-1.

**Note:** SLEEP\_MODE and IDLE\_MODE are constants, defined in the assembler include file, for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

### 10.2.1 SLEEP MODE

Sleep mode includes these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The I/O pin directions and states are frozen.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT or RTCC, with LPRC as the clock source, is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the input change notification on the I/O ports, or peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- On any interrupt source that is individually enabled
- · On any form of device Reset
- · On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered.

#### EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV	#SLEEP_MODE	; Put the device into SLEEP mode
PWRSAV	#IDLE_MODE	; Put the device into IDLE mode
BSET	DSCON, #DSEN	; Enable Deep Sleep
PWRSAV	#SLEEP_MODE	; Put the device into Deep SLEEP mode

# 14.1 Input Capture Registers

### REGISTER 14-1: IC1CON: INPUT CAPTURE 1 CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
_	—	ICSIDL	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture 1 Module Stop in Idle Control bit
	<ul> <li>1 = Input capture module will halt in CPU Idle mode</li> <li>0 = Input capture module will continue to operate in CPU Idle mode</li> </ul>
bit 12-8	Unimplemented: Read as '0'
bit 7	ICTMR: Input Capture 1 Timer Select bit
	<ul> <li>1 = TMR2 contents are captured on capture event</li> <li>0 = TMR3 contents are captured on capture event</li> </ul>
bit 6-5	ICI<1:0>: Select Number of Captures per Interrupt bits
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	00 = Interrupt on every capture event
bit 4	ICOV: Input Capture 1 Overflow Status Flag bit (read-only)
	1 = Input capture overflow occurred
	0 = No input capture overflow occurred
bit 3	ICBNE: Input Capture 1 Buffer Empty Status bit (read-only)
	<ul> <li>1 = Input capture buffer is not empty, at least one more capture value can be read</li> <li>0 = Input capture buffer is empty</li> </ul>
bit 2-0	ICM<2:0>: Input Capture 1 Mode Select bits
	<ul> <li>111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (rising edge detect only, all other control bits are not applicable)</li> <li>110 = Upused (medule is disabled)</li> </ul>
	101 = Capture mode, every 16th rising edge
	100 = Capture mode, every 4th rising edge
	011 = Capture mode, every rising edge
	010 = Capture mode, every failing edge
	for this mode
	000 = Input capture module is turned off



### FIGURE 16-1: SPI1 MODULE BLOCK DIAGRAM (STANDARD BUFFER MODE)

## 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to the *"PIC24F Family Reference Manual"*, Section 21. "UART" (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA<sup>®</sup> encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS pins

- Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- · 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9<sup>th</sup> bit = 1)
- Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UART is displayed in Figure 18-1. The UART module consists of these important hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- · Asynchronous Receiver

### FIGURE 18-1: UART SIMPLIFIED BLOCK DIAGRAM



### REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit				
C = Clearable bit	HS = Hardware Settable bit	it HSC = Hardware Settable/Clearable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15,13 UTXISEL<1:0>: Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 UTXINV: IrDA<sup>®</sup> Encoder Transmit Polarity Inversion bit

	,
	<u>If IREN = 0:</u>
	1 = UxTX Idle '0'
	0 = UxTX Idle '1'
	<u>If IREN = 1:</u>
	1 = UxTX Idle '1'
	0 = UxTX Idle '0'
bit 12	Unimplemented: Read as '0'
bit 11	UTXBRK: Transmit Break bit
	1 = Send Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
	0 = Sync Break transmission is disabled or completed
bit 10	UTXEN: Transmit Enable bit
	1 = Transmit is enabled, UxTX pin is controlled by UARTx
	0 = Transmit is disabled, any pending transmission is aborted and buffer is reset. UxTX pin is controlled by the PORT register.
bit 9	UTXBF: Transmit Buffer Full Status bit (read-only)
	1 = Transmit buffer is full
	0 = Transmit buffer is not full, at least one more character can be written
bit 8	TRMT: Transmit Shift Register Empty bit (read-only)
	<ul> <li>1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)</li> <li>0 = Transmit Shift Register is not empty, a transmission is in progress or queued</li> </ul>
bit 7-6	URXISEL<1:0>: Receive Interrupt Mode Selection bits
	<ul> <li>11 = Interrupt is set on RSR transfer, making the receive buffer full (i.e., has 4 data characters)</li> <li>10 = Interrupt is set on RSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)</li> <li>0x = Interrupt is set when any character is received and transferred from the RSR to the receive buffer;</li> </ul>

REGISTER	19-3. ALUI	GREI. ALAN			GISTER		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARP17	ARP16	ARP15	ARP14	ARP13	ARP12	ARP11	ARPIO
bit 7							bit 0
Legend:							]
R = Readable	e bit	W = Writable I	oit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	ALRMEN: Al	arm Enable bit					
	1 = Alarm is	enabled (clear	ed automatica	illy after an ala	arm event whe	never ARPT<7	:0> = 00h and
	CHIME =	= 0) dia alcha d					
hit 14		uisabled					
DIL 14				allowed to roll	over from 00h	to EEb	
	1 = Chime is 0 = Chime is	disabled: ARP	<7.0> bits are $<7.0>$ bits atc	once they re	ach 00h		
bit 13-10	AMASK<3:0	>: Alarm Mask (	Configuration b	pits			
	0000 = Eve	ry half second	0				
	0001 = Eve	ry second					
	0010 = Eve	ry 10 seconds					
	0011 = Even	ry minute					
	0100 = Eve	ry hour					
	0110 = Onc	e a day					
	0111 = Onc	e a week					
	1000 = Onc	e a month	tubon configu	une d feur Debuije	m ooth anaa a		
	1001 = Onc 101x = Res	e a year (excep erved – do not i	t when conligt ise	ired for Februa	iry 29 <sup>th</sup> , once e	very 4 years)	
	11xx = Res	erved – do not u	ise				
bit 9-8	ALRMPTR<1	:0>: Alarm Valu	ie Register Wi	ndow Pointer b	oits		
	Points to the c	corresponding Al	arm Value regis	sters when read	ing the ALRMV	ALH and ALRM	VALL registers.
	The ALRMPT	R<1:0> value de	ecrements on e	every read or wr	rite of ALRMVA	LH until it reach	<b>es</b> '00'.
	ALRMVAL<1	<u>5:8&gt;:</u>					
	00 = ALRIMM	IIIN D					
	10 = ALRMM	INTH					
	11 = Unimple	emented					
	ALRMVAL<7	:0>:					
	00 = ALRMS	EC					
	01 = ALRMH	R AV					
	11 = Unimple	emented					
bit 7-0	ARPT<7:0>:	Alarm Repeat C	Counter Value	bits			
	11111111 =	Alarm will repe	eat 255 more t	imes			
	0000000 -	Alarm will not	reneat				
	The counter of	decrements on a	any alarm eve	nt; it is prevent	ted from rolling	over from 00h	to FFh unless
	CHIME = 1.		-	·	0		

### REGISTER 19-3: ALCFGRPT: ALARM CONFIGURATION REGISTER

## 20.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Programmable Cyclic Redundancy Check, refer to the "PIC24F Family Reference Manual", Section 30. "Programmable Cyclic Redundancy Check (CRC)" (DS39714).

The programmable Cyclic Redundancy Check (CRC) module in PIC24F devices is a software-configurable CRC checksum generator. The CRC algorithm treats a message as a binary bit stream and divides it by a fixed binary number.

The remainder from this division is considered the checksum. As in division, the CRC calculation is also an iterative process. The only difference is that these operations are done on modulo arithmetic based on mod2. For example, division is replaced with the XOR operation (i.e., subtraction without carry). The CRC algorithm uses the term, polynomial, to perform all of its calculations.

The divisor, dividend and remainder that are represented by numbers are termed as polynomials with binary coefficients.

The programmable CRC generator offers the following features:

- · User-programmable polynomial CRC equation
- Interrupt output
- Data FIFO

The module implements a software-configurable CRC generator. The terms of the polynomial and its length can be programmed using the CRCXOR (X<15:1>) bits and the CRCCON (PLEN<3:0>) bits, respectively. Consider the CRC equation:

### EQUATION 20-1: CRC

$$x^{16} + x^{12} + x^5 + 1 \\$$

To program this polynomial into the CRC generator, the CRC register bits should be set as provided in Table 20-1.

#### TABLE 20-1: EXAMPLE CRC SETUP

Bit Name	Bit Value
PLEN<3:0>	1111
X<15:1>	00010000010000

The value of X<15:1>, the 12<sup>th</sup> bit and the 5<sup>th</sup> bit are set to '1', as required by the equation. The 0 bit required by the equation is always XORed. For a 16-bit polynomial, the 16<sup>th</sup> bit is also always assumed to be XORed; therefore, the X<15:1> bits do not have the 0 bit or the 16<sup>th</sup> bit.

The topology of a standard CRC generator is displayed in Figure 20-2.



### FIGURE 20-1: CRC SHIFTER DETAILS

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### TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0000h1FFFh}
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal $\in \{031\}$
lit8	8-bit unsigned literal $\in \{0255\}$
lit10	10-bit unsigned literal $\in$ {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal $\in \{016384\}$
lit16	16-bit unsigned literal $\in \{065535\}$
lit23	23-bit unsigned literal $\in$ {08388608}; LSB must be '0'
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal ∈ {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }

### TABLE 29-1:THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
Operating Junction Temperature Range	TJ	-40	_	+175	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $PI/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD	Pint + Pi/o			W
Maximum Allowed Power Dissipation	Рдмах (Тј – Та)/θја				W

### TABLE 29-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit	Notes
Package Thermal Resistance, 20-Pin PDIP	θJA	62.4	_	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60		°C/W	1
Package Thermal Resistance, 20-Pin SSOP	θJA	108	-	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θJA	71	_	°C/W	1
Package Thermal Resistance, 20-Pin SOIC	θJA	75	_	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	80.2	-	°C/W	1
Package Thermal Resistance, 20-Pin QFN	θJA	43	_	°C/W	1
Package Thermal Resistance, 28-Pin QFN	θJA	32	_	°C/W	1

**Note 1:** Junction to ambient thermal resistance, Theta-JA ( $\theta$ JA) numbers are achieved by package simulations.





### TABLE 29-25: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Sym	Characteristic	Min	Conditions				
DO31	TIOR	Port Output Rise Time	—	10	25	ns		
DO32	TIOF	Port Output Fall Time	—	10	25	ns		
DI35	Tinp	INTx pin High or Low Time (output)	20	—	—	ns		
DI40	Trbp	CNx High or Low Time (input)	2	—	—	Тсү		

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.



### TABLE 29-29: I<sup>2</sup>C<sup>™</sup> BUS START/STOP BIT TIMING REQUIREMENTS (MASTER MODE)

АС СНА	RACTER	ISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 2.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial)} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Charac	teristic	Min <sup>(1)</sup> Max Units Conditions				
IM30	TSU:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)		μs	Only relevant for	
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)	_	μs	Repeated Start	
			1 MHz mode <sup>(2)</sup>	Tcy/2 (BRG + 1)	_	μs	condition	
IM31	Thd:sta	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	After this period, the	
		ŀ	Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	_	μs	first clock pulse is
			1 MHz mode <sup>(2)</sup>	Tcy/2 (BRG + 1)	—	μS	generated	
IM33	Tsu:sto	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	μS		
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)	—	μS		
			1 MHz mode <sup>(2)</sup>	Tcy/2 (BRG + 1)	—	μS		
IM34	THD:STO	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	ns		
		Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	—	ns		
			1 MHz mode <sup>(2)</sup>	Tcy/2 (BRG + 1)	_	ns		

Note 1: BRG is the value of the l<sup>2</sup>C<sup>™</sup> Baud Rate Generator. Refer to Section 17.3 "Setting Baud Rate When Operating as a Bus Master" for details.

2: Maximum pin capacitance = 10 pF for all I<sup>2</sup>C pins (for 1 MHz mode only).

### FIGURE 29-10: I<sup>2</sup>C<sup>™</sup> BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



### FIGURE 29-14: INPUT CAPTURE TIMINGS



### TABLE 29-33: INPUT CAPTURE

Param. No.	Symbol	Characteristic		Min	Мах	Units	Conditions
IC10	TccL	ICx Input Low Time –	No Prescaler	Tcy + 20	_	ns	Must also meet
		Synchronous Timer	With Prescaler	20	—	ns	Parameter IC15
IC11	ТссН	ICx Input Low Time –	No Prescaler	Tcy + 20	—	ns	Must also meet
		Synchronous Timer	With Prescaler	20	—	ns	Parameter IC15
IC15	TccP	ICx Input Period – Synchronous Timer		<u>2 * Tcy + 40</u> N	_	ns	N = prescale value (1, 4, 16)

### TABLE 29-34: OUTPUT CAPTURE

Param. No.	Symbol	Characteristic	Min	Мах	Units	Conditions
OC11	TccR	OC1 Output Rise Time		10	ns	
			—	—	ns	
OC10	TCCF	OC1 Output Fall Time	—	10	ns	
			—	—	ns	

### FIGURE 29-15: OUTPUT COMPARE TIMINGS



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