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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 75264 |
| Total RAM Bits | 516096 |
| Number of I/O | 620 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 896-BGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/agle3000v2-fgg896 |

**Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard)**

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option[1] (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{PYS}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.12 | 0.18 | 1.08 | 1.34 | 0.66 | 2.17 | 1.69 | 2.71 | 3.08 | 5.76 | 5.28 | ns |
| 3.3 V LVCMOS Wide Range[1, 2] | 100 µA | 12 | High | 5 | – | 0.97 | 2.96 | 0.18 | 1.42 | 1.84 | 0.66 | 2.98 | 2.28 | 3.86 | 4.36 | 6.58 | 5.87 | ns |
| 2.5 V LVCMOS | 12 | 12 | High | 5 | – | .097 | 2.15 | 0.18 | 1.31 | 1.41 | 0.66 | 2.20 | 1.85 | 2.78 | 2.98 | 5.80 | 5.45 | ns |
| 1.8 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.37 | 0.18 | 1.27 | 1.59 | 0.66 | 2.42 | 2.03 | 3.07 | 3.57 | 6.02 | 5.62 | ns |
| 1.5 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.69 | 0.18 | 1.47 | 1.77 | 0.66 | 2.75 | 2.30 | 3.24 | 3.67 | 6.35 | 5.89 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 [3] | 0.97 | 2.38 | 0.18 | 0.96 | 1.42 | 0.66 | 2.43 | 1.80 | 2.72 | 3.08 | 6.03 | 5.39 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 [3] | 0.97 | 2.38 | 0.19 | 0.92 | 1.34 | 0.66 | 2.43 | 1.80 | 2.72 | 3.08 | 6.03 | 5.39 | ns |
| 3.3 V GTL | 20[4] | – | High | 10 | 25 | 0.97 | 1.78 | 0.19 | 2.35 | – | 0.66 | 1.80 | 1.78 | – | – | 5.39 | 5.38 | ns |
| 2.5 V GTL | 20[4] | – | High | 10 | 25 | 0.97 | 1.85 | 0.19 | 1.98 | – | 0.66 | 1.89 | 1.82 | – | – | 5.49 | 5.42 | ns |
| 3.3 V GTL+ | 35 | – | High | 10 | 25 | 0.97 | 1.80 | 0.19 | 1.32 | – | 0.66 | 1.84 | 1.77 | – | – | 5.44 | 5.36 | ns |
| 2.5 V GTL+ | 33 | – | High | 10 | 25 | 0.97 | 1.92 | 0.19 | 1.26 | – | 0.66 | 1.96 | 1.80 | – | – | 5.56 | 5.40 | ns |
| HSTL (I) | 8 | – | High | 20 | 50 | 0.97 | 2.67 | 0.18 | 1.72 | – | 0.66 | 2.72 | 2.67 | – | – | 6.32 | 6.26 | ns |
| HSTL (II) | 15 | – | High | 20 | 25 | 0.97 | 2.55 | 0.18 | 1.72 | – | 0.66 | 2.60 | 2.34 | – | – | 6.20 | 5.93 | ns |
| SSTL2 (I) | 15 | – | High | 30 | 50 | 0.97 | 1.86 | 0.19 | 1.12 | – | 0.66 | 1.90 | 1.68 | – | – | 5.50 | 5.28 | ns |
| SSTL2 (II) | 18 | – | High | 30 | 25 | 0.97 | 1.89 | 0.19 | 1.12 | – | 0.66 | 1.93 | 1.62 | – | – | 5.53 | 5.22 | ns |
| SSTL3 (I) | 14 | – | High | 30 | 50 | 0.97 | 2.00 | 0.19 | 1.06 | – | 0.66 | 2.04 | 1.67 | – | – | 5.64 | 5.27 | ns |
| SSTL3 (II) | 21 | – | High | 30 | 25 | 0.97 | 1.81 | 0.19 | 1.06 | – | 0.66 | 1.85 | 1.55 | – | – | 5.45 | 5.14 | ns |
| LVDS | 24 | – | High | – | – | 0.97 | 1.73 | 0.19 | 1.62 | – | – | – | – | – | – | – | – | ns |
| LVPECL | 24 | – | High | – | – | 0.97 | 1.65 | 0.18 | 1.42 | – | – | – | – | – | – | – | – | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI Specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Detailed I/O DC Characteristics

**Table 2-27 • Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

**Table 2-28 • I/O Output Buffer Maximum Resistances[1]**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 1.2 V LVCMOS[4] | 2 mA | 158 | 164 |
| 1.2 V LVCMOS Wide Range[4] | 100 µA | Same as regular 1.2 V LVCMOS | Same as regular 1.2 V LVCMOS |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Applicable to IGLOOe V2 devices operating in the 1.2 V core range ONLY.*
5. *Output drive strength is below JEDEC specification.*

### 1.2 V DC Core Voltage

**Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 1.55 | 5.54 | 0.26 | 1.31 | 1.58 | 1.10 | 5.63 | 4.53 | 2.79 | 2.87 | 11.42 | 10.32 | ns |
| 8 mA | Std. | 1.55 | 4.60 | 0.26 | 1.31 | 1.58 | 1.10 | 4.67 | 3.94 | 3.09 | 3.45 | 10.45 | 9.73 | ns |
| 12 mA | Std. | 1.55 | 3.93 | 0.26 | 1.31 | 1.58 | 1.10 | 3.99 | 3.51 | 3.28 | 3.82 | 9.77 | 9.29 | ns |
| 16 mA | Std. | 1.55 | 3.74 | 0.26 | 1.31 | 1.58 | 1.10 | 3.79 | 3.41 | 3.32 | 3.92 | 9.58 | 9.20 | ns |
| 24 mA | Std. | 1.55 | 3.64 | 0.26 | 1.31 | 1.58 | 1.10 | 3.69 | 3.42 | 3.38 | 4.30 | 9.48 | 9.21 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

**Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 1.55 | 3.26 | 0.26 | 1.31 | 1.58 | 1.10 | 3.33 | 2.67 | 2.79 | 3.01 | 9.12 | 8.46 | ns |
| 8 mA | Std. | 1.55 | 2.77 | 0.26 | 1.31 | 1.58 | 1.10 | 2.80 | 2.24 | 3.09 | 3.59 | 8.59 | 8.03 | ns |
| 12 mA | Std. | 1.55 | 2.47 | 0.26 | 1.31 | 1.58 | 1.10 | 2.51 | 2.04 | 3.28 | 3.97 | 8.29 | 7.82 | ns |
| 16 mA | Std. | 1.55 | 2.42 | 0.26 | 1.31 | 1.58 | 1.10 | 2.46 | 2.00 | 3.33 | 4.08 | 8.24 | 7.79 | ns |
| 24 mA | Std. | 1.55 | 2.45 | 0.26 | 1.31 | 1.58 | 1.10 | 2.48 | 1.95 | 3.38 | 4.46 | 8.26 | 7.73 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### Timing Characteristics

#### 1.2 V DC Core Voltage

**Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 9.92 | 0.26 | 2.09 | 2.95 | 1.10 | 9.53 | 7.48 | 4.02 | 3.67 | 15.31 | 13.26 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

**Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 4.06 | 0.26 | 2.09 | 2.95 | 1.10 | 3.92 | 3.46 | 4.01 | 3.79 | 9.71 | 9.24 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

## 1.2 V LVCMOS Wide Range

**Table 2-68 • Minimum and Maximum DC Input and Output Levels**

| 1.2 V LVCMOS Wide Range[1] | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[4] | Min. (V) | Max. (V) | Min. (V) | Max (V) | Max. (V) | Min. (V) | µA | µA | Max. (mA)[5] | Max. (mA)[5] | µA[6] | µA[6] |
| 100 µA | 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 100 | 100 | 20 | 26 | 10 | 10 |

*Notes:*

1. *Applicable to V2 devices ONLY.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI . Input current is larger when operating outside recommended ranges.*
4. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

### Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-48 for worst-case timing.

### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

**Table 2-69 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min., V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-12.

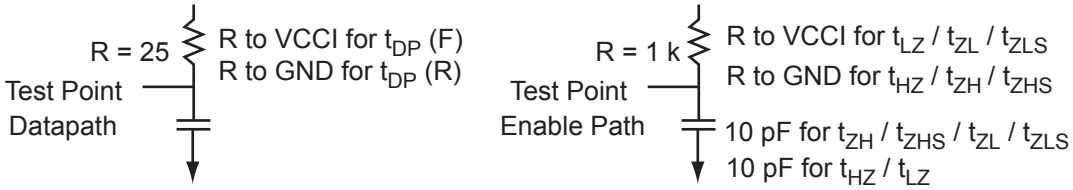



**Figure 2-12 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-70.

**Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$<br>0.615 * VCCI for $t_{DP(F)}$ | – | 10 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

### SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-101 • Minimum and Maximum DC Input and Output Levels**

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 18 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI – 0.43 | 18 | 18 | 169 | 124 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

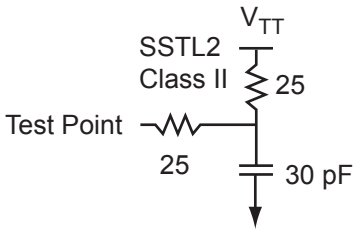



**Figure 2-20 • AC Loading**

**Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input HIGH (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 2.3 V VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.98 | 1.94 | 0.19 | 1.15 | 0.67 | 1.97 | 1.66 | | | 5.60 | 5.29 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,**
**Worst-Case VCCI = 2.3 V VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 1.55 | 2.20 | 0.26 | 1.39 | 1.10 | 2.24 | 1.97 | | | 8.05 | 7.78 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

**Table 2-113 • Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL[1] | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH[1] | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIH[2,3] | Input High Leakage Current | | | 10 | µA |
| IIL[2,4] | Input Low Leakage Current | | | 10 | µA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

*Notes:*

1. *IOL/IOH is defined by VODIFF/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*

**Table 2-114 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---|---|---|---|
| 1.075 | 1.325 | Cross point | – |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-115 • LVDS – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.98 | 1.77 | 0.19 | 1.62 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-116 • LVDS – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 1.55 | 2.19 | 0.26 | 1.88 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

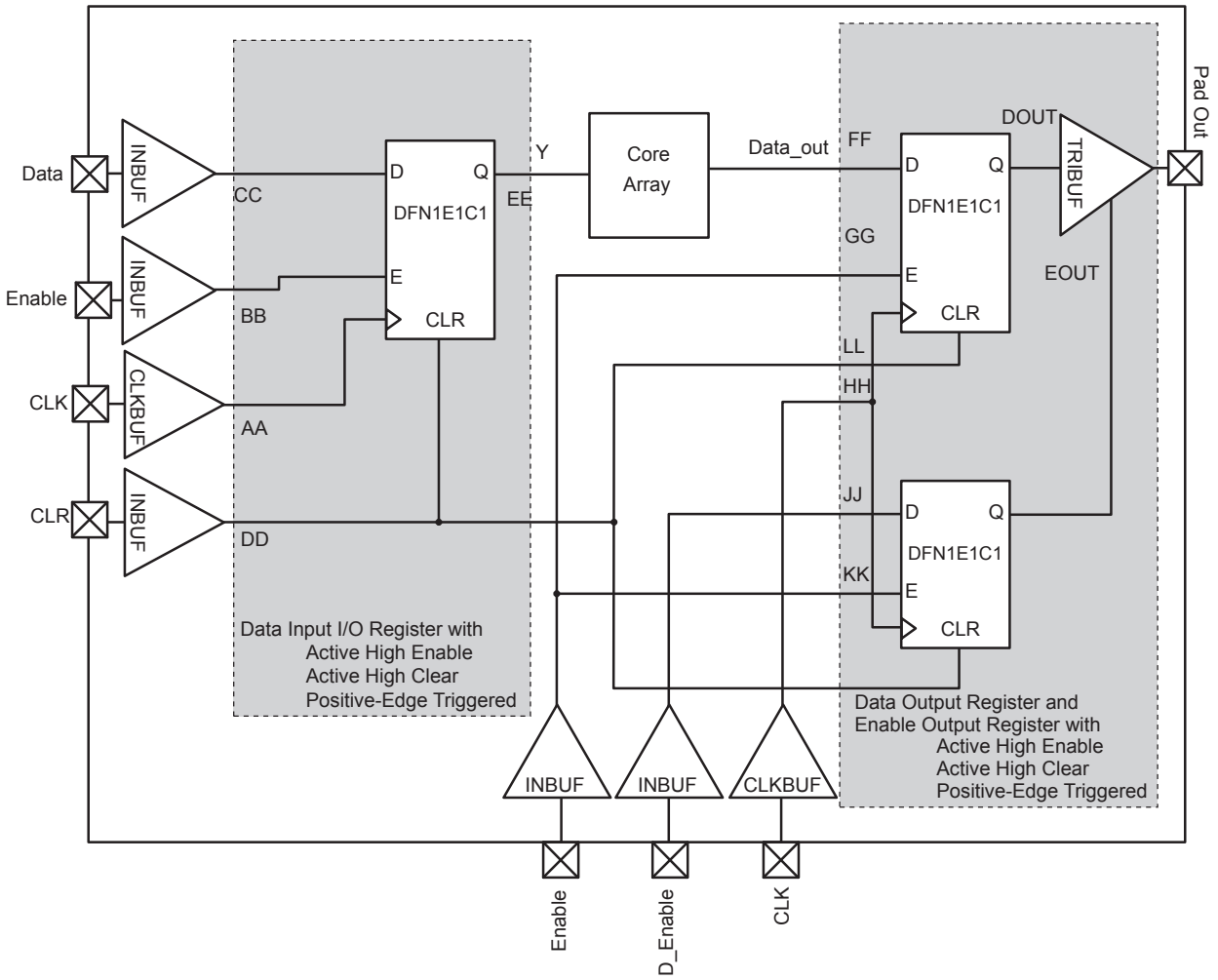



***Figure 2-27 •*** **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

## DDR Module Specifications

### *Input DDR Module*

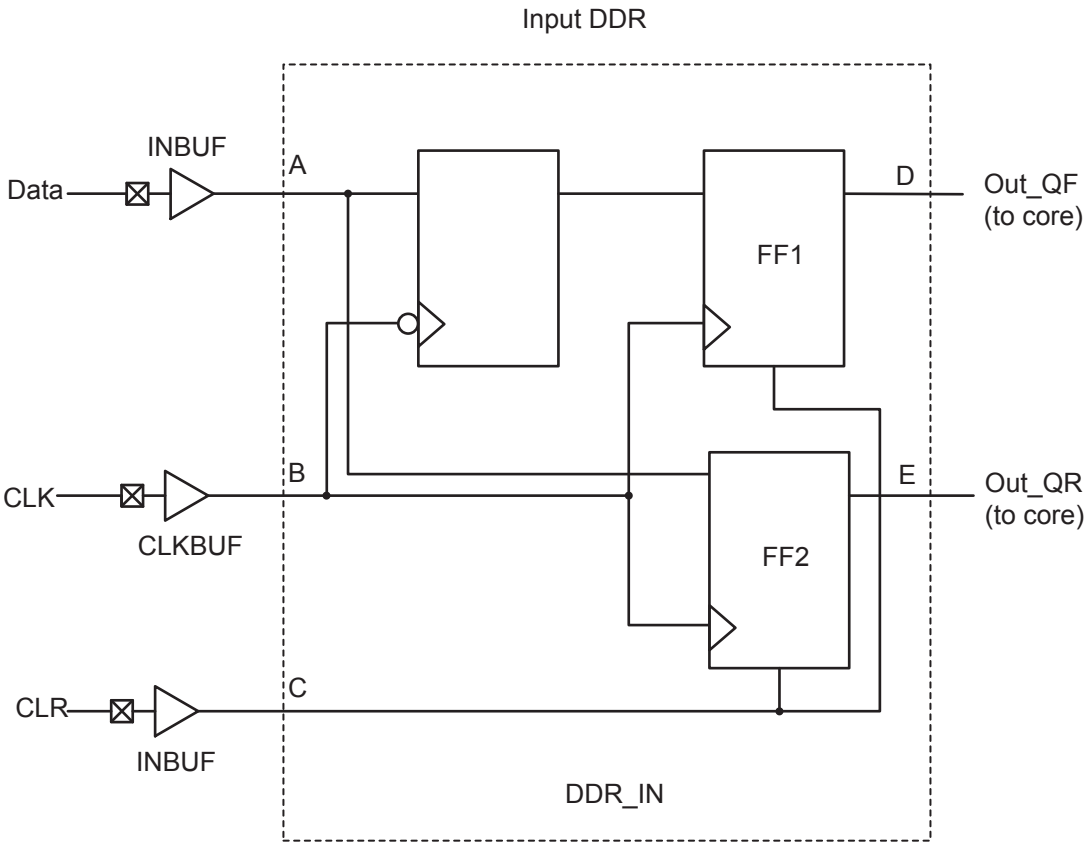



***Figure 2-31 •*** **Input DDR Timing Model**

***Table 2-129 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

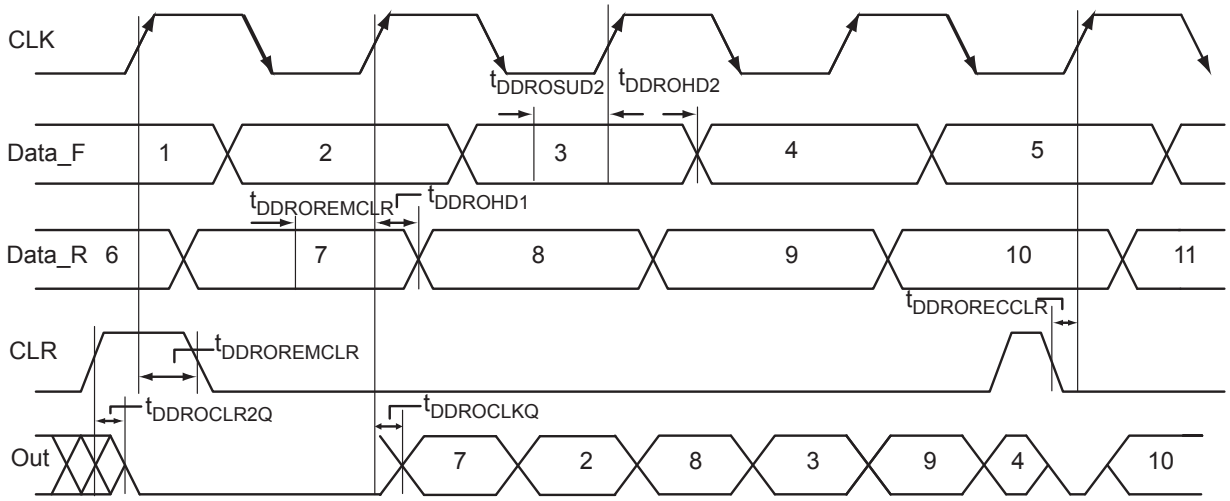



***Figure 2-34 •*** **Output DDR Timing Diagram**

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-133 • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.07 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.38 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.23 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 250.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-134 • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 1.09 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 1.16 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 160.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

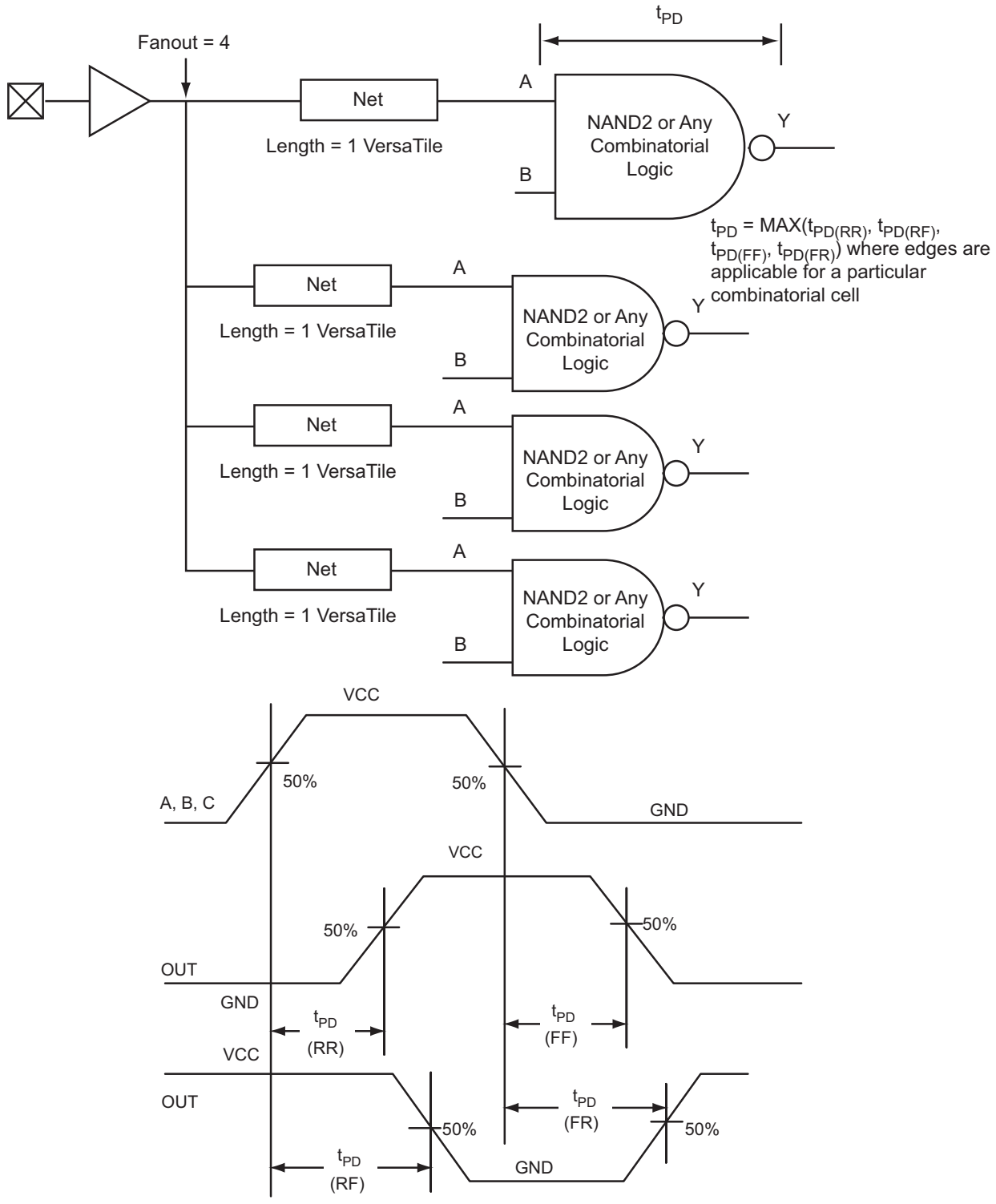



***Figure 2-36 •*** **Timing Model and Waveforms**

## VersaTile Specifications as a Sequential Module

The IGLOOe library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

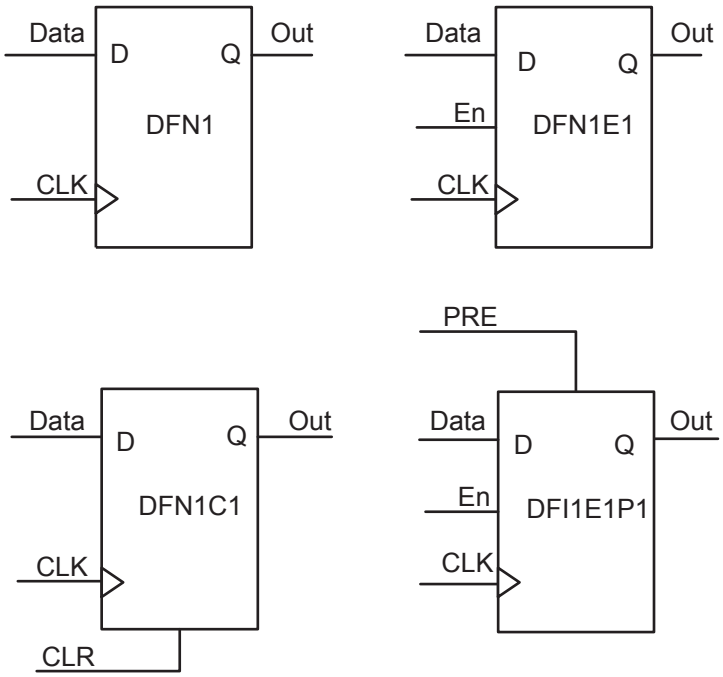
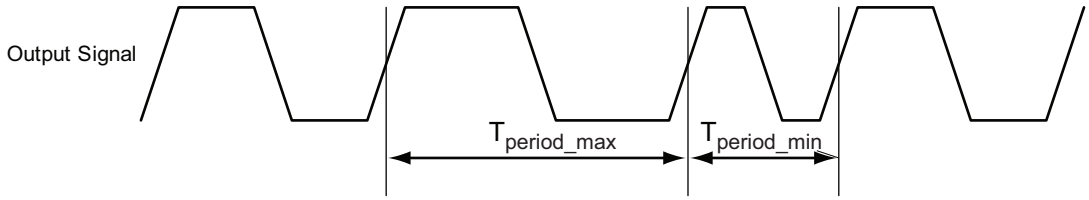



***Figure 2-37 •*** **Sample of Sequential Cells**




*Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.*

***Figure 2-40 •*** **Peak-to-Peak Jitter Definition**

## Timing Waveforms

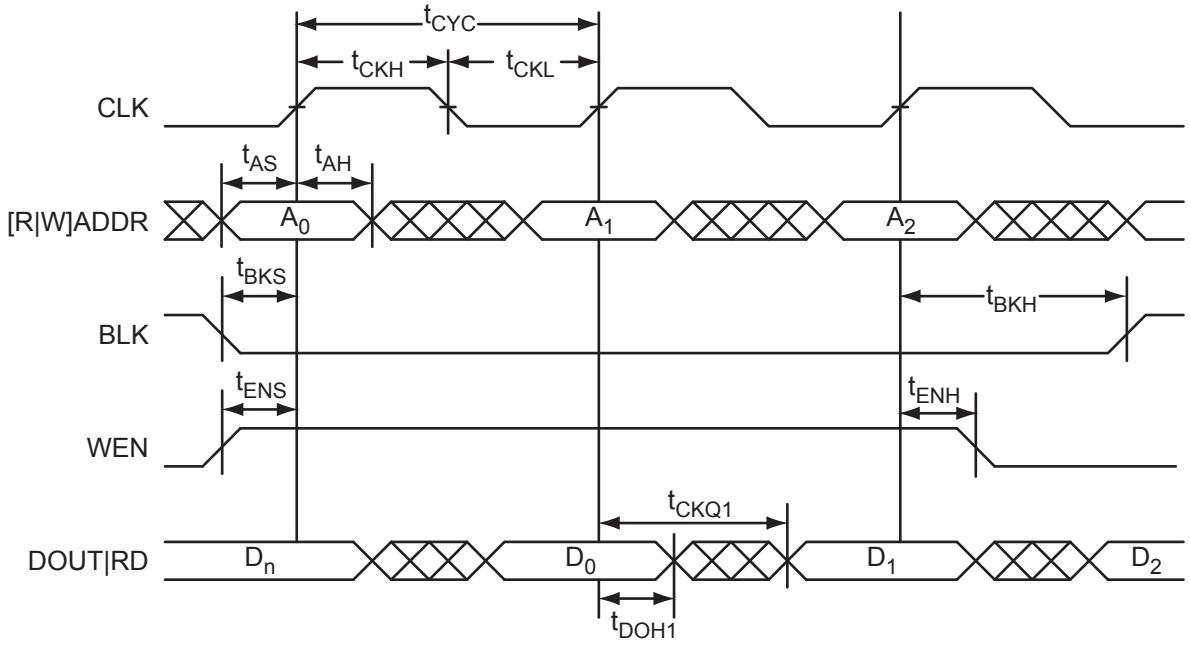



***Figure 2-42 •*** **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512X18.**

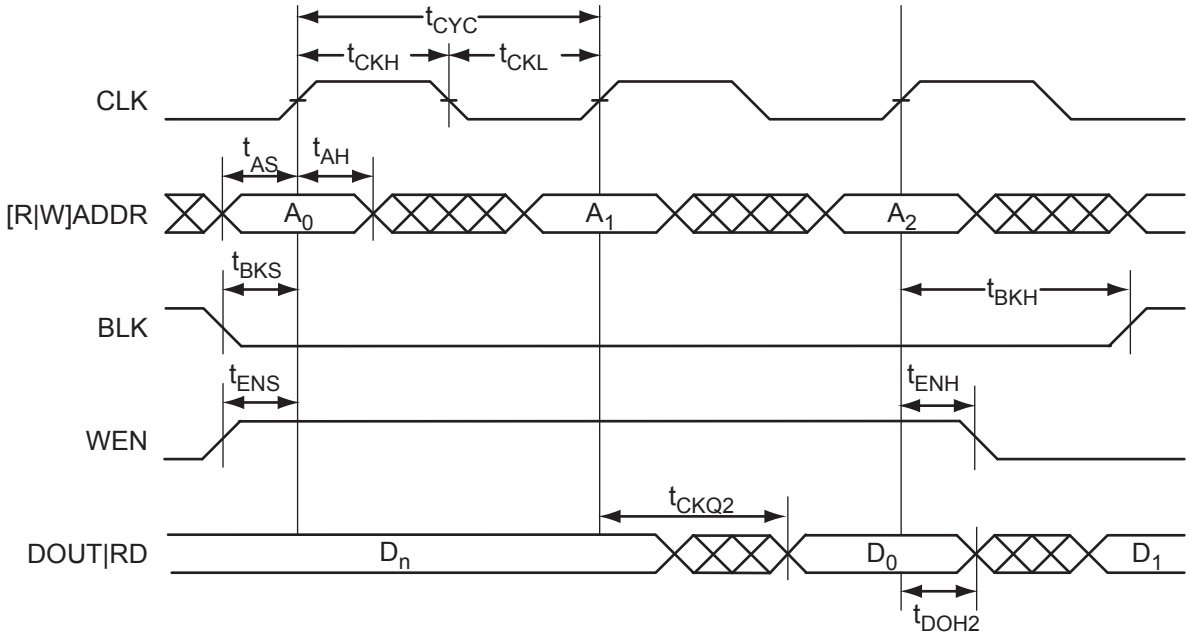



***Figure 2-43 •*** **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512X18.**

# Embedded FlashROM Characteristics

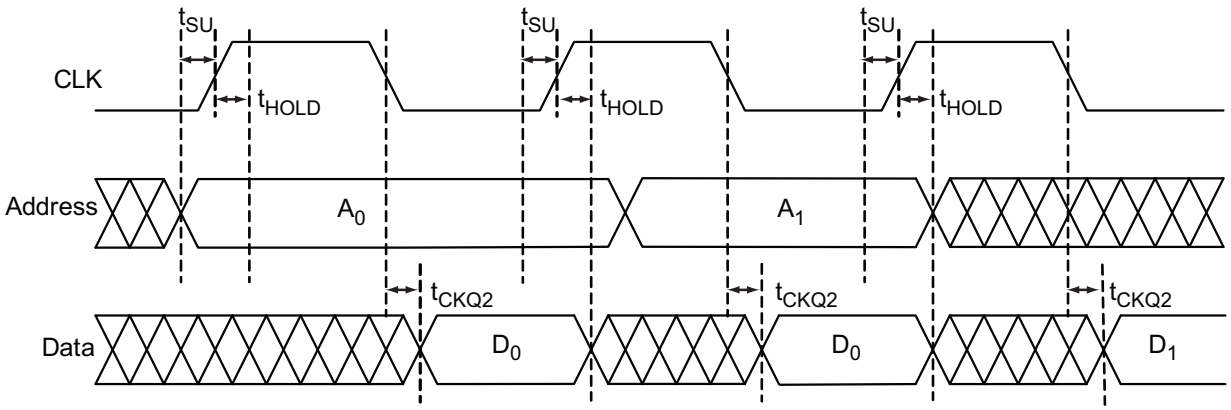



***Figure 2-55 •*** **Timing Diagram**

## *Timing Characteristics*

### *Applies to 1.5 V DC Core Voltage*

***Table 2-151 •*** **Embedded FlashROM Access Time**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{SU}$ | Address Setup Time | 0.58 | ns |
| $t_{HOLD}$ | Address Hold Time | 0.00 | ns |
| $t_{CK2Q}$ | Clock-to-Out | 34.14 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | 15 | MHz |

### *Applies to 1.2 V DC Core Voltage*

***Table 2-152 •*** **Embedded FlashROM Access Time**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{SU}$ | Address Setup Time | 0.59 | ns |
| $t_{HOLD}$ | Address Hold Time | 0.00 | ns |
| $t_{CK2Q}$ | Clock-to-Out | 52.90 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | 10 | MHz |

# User Pins

**I/O** **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

**GL** **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOOe FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the *IGLOOe FPGA Fabric User's Guide* for an explanation of the naming of global pins.

**FF** **Flash*Freeze Mode Activation Pin**

Flash*Freeze mode is available on IGLOOe devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O. The FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

***Table 3-3* • TRST and TCK Pull-Down Recommendations**

| VJTAG | Tie-Off Resistance* |
|---|---|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

*Note: Equivalent parallel resistance if more than one device is on the JTAG chain*

**TDI Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

**TDO Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

**TMS Test Mode Select**

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

**TRST Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

# Special Function Pins

**NC No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

**DC Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

# Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

| Revision | Changes | Page |
|---|---|---|
| **Revision 8 (Nov 2009)** | The version changed to v2.0 for IGLOOe datasheet chapters, indicating the datasheet contains information based on final characterization. | N/A |
| Product Brief v2.0 | The "Pro (Professional) I/O" section was revised to add "Hot-swappable and cold-sparing I/Os." | I |
| | The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance." | I |
| | Definitions of hot-swap and cold-sparing were added to the "Pro I/Os with Advanced I/O Standards" section. | 1-7 |
| DC and Switching Characteristics v2.0 | 3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data. | N/A |
| | IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables. | N/A |
| | Values for 1.2 V wide range DC core supply voltage were added to Table 2-2 • Recommended Operating Conditions 1. Table notes regarding 3.3 V wide range and the core voltage required for programming were added to the table. | 2-2 |
| | The data in Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (1.5 V DC core supply voltage) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (1.2 V DC core supply voltage) was revised. | 2-6 |
| | 3.3 V LVCMOS wide range data was included in Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1. Table notes were added in connection with this data. | 2-9, 2-10 |
| | The temperature was revised from 110ºC to 100ºC in Table 2-31 • Duration of Short Circuit Event before Failure and Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*. | 2-31, 2-31 |
| | The tables in the "Overview of I/O Performance" section and "Detailed I/O DC Characteristics" sectionwere revised to include 3.3 V LVCMOS and 1.2 V LVCMOS wide range. | 2-20, 2-28 |
| | Most tables were updated in the following sections, revising existing values and adding information for 3.3 V and 1.2 V wide range:<br>"Single-Ended I/O Characteristics"<br>"Voltage-Referenced I/O Characteristics"<br>"Differential I/O Characteristics" | 2-32, 2-51, 2-62 |
| | The value for "Delay range in block: fixed delay" was revised in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification. | 2-91, 2-92 |
| | The timing characteristics tables for RAM4K9 and RAM512X18 were updated, including renaming of the address collision parameters. | 2-98 – 2-101 |
| **Revision 7 (Apr 2009)**<br>Product Brief v1.4<br>DC and Switching Characteristics Advance v0.4 | The –F speed grade is no longer offered for IGLOOe devices and was removed from the documentation. The speed grade column and note regarding –F speed grade were removed from "IGLOOe Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed. | III, IV |

# Datasheet Categories

### Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOOe Device Status" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Production

This version contains information that is considered to be final.

## Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

# Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group’s products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.