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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	620
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agle3000v5-fgg896

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings (continued)Std. Speed Grade, Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V,Worst-Case VCCI (per standard)

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option <sup>1</sup> (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	έρουτ (ns)	(su) dQ	(su) <sup>NIC;</sup>	i <sub>PΥ</sub> (ns)	(su) Skd	Eour (ns)	<sup>;51</sup> (us)	(su) <sup>HZ</sup>	ירz (su)	(su) <sup>ZH</sup>	; <sub>ZLS</sub> (ns)	(su) <sup>SHZ;</sup>	Jnits
LVDS	24	-	High	-	_	1.55	2.26	0.25	1.95	_	_	_	-	_	_	_	-	ns
LVPECL	24	-	High	-	-	1.55	2.17	0.25	1.70	-	-	-		-	-	-	-	ns

Notes:

 The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.

5. Output drive strength is below JEDEC specification.

6. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

### static Microsemi.

IGLOOe DC and Switching Characteristics

### Single-Ended I/O Characteristics

### 3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

3.3 V LVTTL / 3.3 V LVCMOS	v	ΊL	v	IH	VOL	VOH	IOL	юн	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

 Table 2-34 •
 Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-7 • AC Loading

### Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)
0	3.3	1.4	-	5

Note: \*Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

### 3.3 V LVCMOS Wide Range

3.3 V LVC	MOS Wide Range	V	L	۱ ۱	/IH	VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>3</sup>	Min. (V)	Max. (V)	Min. (V)	Max (V)	Max. (V)	Min. (V)	μA	μΑ	Max. (mA) <sup>4</sup>	Max. (mA) <sup>4</sup>	μA⁵	μA <sup>5</sup>
100 µA	2 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	132	127	10	10
100 µA	24 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	268	181	10	10

#### Table 2-40 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

 The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

4. Currents are measured at 85°C junction temperature.

5. All LVCMOS 3.3 V software macros supports LVCMOS 3.3 V wide range as specified in the JDEC8a specification.

6. Software default selection highlighted in gray.

#### Table 2-41 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)
0	3.3	1.4	_	5

Note: \*Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

### Timing Characteristics

### 1.5 V DC Core Voltage

Table 2-48 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

	Speed													Unit
Drive Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	S
4 mA	Std.	0.97	5.55	0.18	1.31	1.41	0.66	5.66	4.75	2.28	1.96	9.26	8.34	ns
8 mA	Std.	0.97	4.58	0.18	1.31	1.41	0.66	4.67	4.07	2.58	2.53	8.27	7.66	ns
12 mA	Std.	0.97	3.89	0.18	1.31	1.41	0.66	3.97	3.58	2.78	2.91	7.56	7.17	ns
16 mA	Std.	0.97	3.68	0.18	1.31	1.41	0.66	3.75	3.47	2.82	3.01	7.35	7.06	ns
24 mA	Std.	0.97	3.59	0.18	1.31	1.41	0.66	3.66	3.48	2.88	3.37	7.26	7.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

#### Table 2-49 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Unit s
4 mA	Std.	0.97	2.94	0.18	1.31	1.41	0.66	3.00	2.68	2.28	2.03	6.60	6.27	ns
8 mA	Std.	0.97	2.45	0.18	1.31	1.41	0.66	2.50	2.12	2.58	2.62	6.10	5.72	ns
12 mA	Std.	0.97	2.15	0.18	1.31	1.41	0.66	2.20	1.85	2.78	2.98	5.80	5.45	ns
16 mA	Std.	0.97	2.10	0.18	1.31	1.41	0.66	2.15	1.80	2.82	3.08	5.75	5.40	ns
24 mA	Std.	0.97	2.11	0.18	1.31	1.41	0.66	2.16	1.74	2.88	3.47	5.75	5.33	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

IGLOOe DC and Switching Characteristics

### 1.2 V DC Core Voltage

### Table 2-50 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

	Speed													
Drive Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	1.55	6.25	0.26	1.55	1.77	1.10	6.36	5.34	2.81	2.63	12.14	11.13	ns
8 mA	Std.	1.55	5.18	0.26	1.55	1.77	1.10	5.26	4.61	3.13	3.32	11.05	10.39	ns
12 mA	Std.	1.55	4.42	0.26	1.55	1.77	1.10	4.49	4.08	3.36	3.76	10.28	9.86	ns
16 mA	Std.	1.55	4.19	0.26	1.55	1.77	1.10	4.25	3.96	3.40	3.89	10.04	9.75	ns
24 mA	Std.	1.55	4.09	0.26	1.55	1.76	1.10	4.15	3.97	3.47	4.32	9.94	9.76	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

## Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	1.55	3.38	0.26	1.55	1.77	1.10	3.42	3.11	2.81	2.72	9.21	8.89	ns
8 mA	Std.	1.55	2.83	0.26	1.55	1.77	1.10	2.87	2.51	3.13	3.42	8.66	8.30	ns
12 mA	Std.	1.55	2.51	0.26	1.55	1.77	1.10	2.54	2.22	3.36	3.85	8.33	8.00	ns
16 mA	Std.	1.55	2.45	0.26	1.55	1.77	1.10	2.48	2.16	3.40	3.97	8.27	7.95	ns
24 mA	Std.	1.55	2.46	0.26	1.55	1.77	1.10	2.49	2.09	3.47	4.44	8.28	7.88	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

#### 1.2 V DC Core Voltage

 Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

 Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

	Speed													
Drive Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	tzhs	Units
2 mA	Std.	1.55	8.21	0.26	1.53	1.96	1.10	8.35	6.88	2.87	1.70	14.14	12.67	ns
4 mA	Std.	1.55	6.83	0.26	1.53	1.96	1.10	6.94	5.88	3.27	3.18	12.73	11.67	ns
6 mA	Std.	1.55	5.85	0.26	1.53	1.96	1.10	5.94	5.19	3.53	3.37	11.73	10.98	ns
8 mA	Std.	1.55	5.52	0.26	1.53	1.96	1.10	5.61	5.06	3.59	3.88	11.39	10.84	ns
12 mA	Std.	1.55	5.42	0.26	1.53	1.96	1.10	5.51	5.06	3.68	4.44	11.30	10.85	ns
16 mA	Std.	1.55	5.42	0.26	1.53	1.96	1.10	5.51	5.06	3.68	4.44	11.30	10.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

### Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

	Speed													
Drive Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
2 mA	Std.	1.55	3.82	0.26	1.53	1.96	1.10	3.98	3.87	2.86	1.72	9.76	9.66	ns
4 mA	Std.	1.55	3.25	0.26	1.53	1.96	1.10	3.30	3.01	3.26	3.26	9.08	8.79	ns
6 mA	Std.	1.55	2.84	0.26	1.53	1.96	1.10	2.88	2.58	3.53	3.81	8.66	8.37	ns
8 mA	Std.	1.55	2.76	0.26	1.53	1.96	1.10	2.80	2.50	3.58	3.97	8.58	8.29	ns
12 mA	Std.	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns
16 mA	Std.	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

3.3 V PCI/PCI-X	VIL		v	IH	VOL	VOH	IOL	ЮН	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min., V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
Per PCI specification	Per PCI curves								10	10		

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-12.



### Figure 2-12 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-70.

#### Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)
0	3.3	0.285 * VCCI for t <sub>DP(R)</sub>	-	10
		0.615 * VCCI for t <sub>DP(F)</sub>		

Note: \*Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

IGLOOe DC and Switching Characteristics

### HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 •	Minimum and Maximum DC	Input and Output Levels
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HSTL Class I		VIL	VIH		VOL	VOH	IOL	юн	IOSH	IOSL	IIL¹	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
8 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI-0.4	8	8	32	39	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



#### Figure 2-17 • AC Loading

#### Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)	
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20	

Note: \*Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

### Timing Characteristics

#### 1.5 V DC Core Voltage

Table 2-91 •HSTL Class I – Applies to 1.5 V DC Core Voltage<br/>Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V,<br/>Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
Std.	0.98	2.74	0.19	1.77	0.67	2.79	2.73			6.42	6.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

#### 1.2 V DC Core Voltage

# Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
Std.	1.55	3.10	0.26	1.94	1.10	3.12	3.10			8.93	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

IGLOOe DC and Switching Characteristics

### **Output Register**





### **Timing Characteristics**

1.5 V DC Core Voltage

Table 2-125 • Output Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units				
t <sub>OCLKQ</sub>	Clock-to-Q of the Output Data Register	1.00	ns				
t <sub>OSUD</sub>	Data Setup Time for the Output Data Register						
t <sub>OHD</sub>	Data Hold Time for the Output Data Register						
t <sub>OSUE</sub>	Enable Setup Time for the Output Data Register						
t <sub>OHE</sub>	Enable Hold Time for the Output Data Register	0.00	ns				
t <sub>OCLR2Q</sub>	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns				
t <sub>OPRE2Q</sub>	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns				
t <sub>OREMCLR</sub>	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns				
t <sub>ORECCLR</sub>	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns				
t <sub>OREMPRE</sub>	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns				
t <sub>ORECPRE</sub>	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns				
t <sub>OWCLR</sub>	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns				
t <sub>OWPRE</sub>	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns				
t <sub>OCKMPWH</sub>	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns				
t <sub>OCKMPWL</sub>	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns				

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### 1.2 V DC Core Voltage

# Table 2-126 • Output Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units				
t <sub>OCLKQ</sub>	Clock-to-Q of the Output Data Register	1.52	ns				
t <sub>OSUD</sub>	Data Setup Time for the Output Data Register	1.15	ns				
t <sub>OHD</sub>	Data Hold Time for the Output Data Register						
t <sub>OSUE</sub>	Enable Setup Time for the Output Data Register						
t <sub>OHE</sub>	Enable Hold Time for the Output Data Register						
t <sub>OCLR2Q</sub>	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns				
t <sub>OPRE2Q</sub>	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns				
t <sub>OREMCLR</sub>	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns				
t <sub>ORECCLR</sub>	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns				
t <sub>OREMPRE</sub>	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns				
t <sub>ORECPRE</sub>	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns				
t <sub>OWCLR</sub>	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns				
t <sub>OWPRE</sub>	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns				
t <sub>OCKMPWH</sub>	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns				
t <sub>OCKMPWL</sub>	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns				

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

### 1.2 V DC Core Voltage

# Table 2-128 • Output Enable Register Propagation Delays Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units				
t <sub>OECLKQ</sub>	Clock-to-Q of the Output Enable Register	1.10	ns				
t <sub>OESUD</sub>	Data Setup Time for the Output Enable Register						
t <sub>OEHD</sub>	Data Hold Time for the Output Enable Register						
t <sub>OESUE</sub>	Enable Setup Time for the Output Enable Register						
t <sub>OEHE</sub>	Enable Hold Time for the Output Enable Register						
t <sub>OECLR2Q</sub>	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns				
t <sub>OEPRE2Q</sub>	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns				
t <sub>OEREMCLR</sub>	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns				
t <sub>OERECCLR</sub>	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns				
t <sub>OEREMPRE</sub>	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns				
t <sub>OERECPRE</sub>	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns				
t <sub>OEWCLR</sub>	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns				
t <sub>OEWPRE</sub>	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns				
t <sub>OECKMPWH</sub>	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns				
t <sub>OECKMPWL</sub>	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns				

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.



### **DDR Module Specifications**

### Input DDR Module



Figure 2-31 • Input DDR Timing Model

Table 2-12	9•	Parameter	Definitions
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Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t <sub>DDRICLKQ1</sub>	Clock-to-Out Out_QR	B, D
t <sub>DDRICLKQ2</sub>	Clock-to-Out Out_QF	B, E
t <sub>DDRISUD</sub>	Data Setup Time of DDR input	A, B
t <sub>DDRIHD</sub>	Data Hold Time of DDR input	A, B
t <sub>DDRICLR2Q1</sub>	Clear-to-Out Out_QR	C, D
t <sub>DDRICLR2Q2</sub>	Clear-to-Out Out_QF	C, E
t <sub>DDRIREMCLR</sub>	Clear Removal	С, В
t <sub>DDRIRECCLR</sub>	Clear Recovery	С, В

### VersaTile Specifications as a Sequential Module

The IGLOOe library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO*, *Fusion*, *and ProASIC3 Macro Library Guide*.



Figure 2-37 • Sample of Sequential Cells

### Timing Waveforms



Figure 2-48 • FIFO Read



Figure 2-49 • FIFO Write

IGLOOe DC and Switching Characteristics

### **Timing Characteristics**

### Applies to 1.5 V DC Core Voltage

Table 2-149 • FIFO

### Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t <sub>ENS</sub>	REN, WEN Setup Time	1.99	ns
t <sub>ENH</sub>	REN, WEN Hold Time	0.16	ns
t <sub>BKS</sub>	BLK Setup Time	0.30	ns
t <sub>BKH</sub>	BLK Hold Time	0.00	ns
t <sub>DS</sub>	Input Data (WD) Setup Time	0.76	ns
t <sub>DH</sub>	Input Data (WD) Hold Time	0.25	ns
t <sub>CKQ1</sub>	Clock HIGH to New Data Valid on RD (pass-through)	3.33	ns
t <sub>CKQ2</sub>	Clock HIGH to New Data Valid on RD (pipelined)	1.80	ns
t <sub>RCKEF</sub>	RCLK HIGH to Empty Flag Valid	3.53	ns
t <sub>WCKFF</sub>	WCLK HIGH to Full Flag Valid	3.35	ns
t <sub>CKAF</sub>	Clock HIGH to Almost Empty/Full Flag Valid	12.85	ns
t <sub>RSTFG</sub>	RESET LOW to Empty/Full Flag Valid	3.48	ns
t <sub>RSTAF</sub>	RESET LOW to Almost Empty/Full Flag Valid	12.72	ns
t <sub>RSTBQ</sub>	RESET LOW to Data Out LOW on RD (pass-through)	2.02	ns
	RESET LOW to Data Out LOW on RD (pipelined)	2.02	ns
t <sub>REMRSTB</sub>	RESET Removal	0.61	ns
t <sub>RECRSTB</sub>	RESET Recovery	3.21	ns
t <sub>MPWRSTB</sub>	RESET Minimum Pulse Width	0.68	ns
t <sub>CYC</sub>	Clock Cycle Time	6.24	ns
F <sub>MAX</sub>	Maximum Frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

### **JTAG 1532 Characteristics**

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-16 for more details.

### **Timing Characteristics**

Applies to 1.2 V DC Core Voltage

### Table 2-153 • JTAG 1532

Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t <sub>DISU</sub>	Test Data Input Setup Time	1.50	ns
t <sub>DIHD</sub>	Test Data Input Hold Time	3.00	ns
t <sub>TMSSU</sub>	Test Mode Select Setup Time	1.50	ns
t <sub>TMDHD</sub>	Test Mode Select Hold Time	3.00	ns
t <sub>TCK2Q</sub>	Clock to Q (data out)	11.00	ns
t <sub>RSTB2Q</sub>	Reset to Q (data out)	30.00	ns
F <sub>TCKMAX</sub>	TCK Maximum Frequency	9.00	MHz
t <sub>TRSTREM</sub>	ResetB Removal Time	1.18	ns
t <sub>TRSTREC</sub>	ResetB Recovery Time	0.00	ns
t <sub>TRSTMPW</sub>	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

### Applies to 1.5 V DC Core Voltage

### Table 2-154 • JTAG 1532

### Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t <sub>DISU</sub>	Test Data Input Setup Time	1.00	ns
t <sub>DIHD</sub>	Test Data Input Hold Time	2.00	ns
t <sub>TMSSU</sub>	Test Mode Select Setup Time	1.00	ns
t <sub>TMDHD</sub>	Test Mode Select Hold Time	2.00	ns
t <sub>TCK2Q</sub>	Clock to Q (data out)	8.00	ns
t <sub>RSTB2Q</sub>	Reset to Q (data out)	25.00	ns
F <sub>TCKMAX</sub>	TCK Maximum Frequency	15.00	MHz
t <sub>TRSTREM</sub>	ResetB Removal Time	0.58	ns
t <sub>TRSTREC</sub>	ResetB Recovery Time	0.00	ns
t <sub>TRSTMPW</sub>	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



## 3 – Pin Descriptions and Packaging

### **Supply Pins**

### GND

### Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

### GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

#### VCC

#### **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOOe V5 devices, and 1.2 V or 1.5 V for IGLOOe V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOOe V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

### VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOOe devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

#### VMVx

### I/O Supply Voltage (quiet)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

### VCCPLA/B/C/D/E/F PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device.

- 1.5 V for IGLOOe devices
- 1.2 V or 1.5 V for IGLOOe V2 devices

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section in the "Clock Conditioning Circuits in Low Power Flash FPGAs and Mixed Signal FPGAs" chapter in the *IGLOOe FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on IGLOOe devices.



Package Pin Assignments

	FG484		FG484
Pin Number	AGLE600 Function	Pin Number	AGLE600 Function
V3	GND	W16	IO68NDB4V0
V4	GEA1/IO102PDB6V0	W17	GDA2/IO68PDB4V0
V5	GEA0/IO102NDB6V0	W18	TMS
V6	GNDQ	W19	GND
V7	GEC2/IO99PDB5V2	W20	NC
V8	IO95NPB5V1	W21	NC
V9	IO91NDB5V1	W22	NC
V10	IO91PDB5V1	Y1	VCCIB6
V11	IO83NDB5V0	Y2	NC
V12	IO83PDB5V0	Y3	NC
V13	IO77NDB4V1	Y4	IO98NDB5V2
V14	IO77PDB4V1	Y5	GND
V15	IO69NDB4V0	Y6	IO94NDB5V1
V16	GDB2/IO69PDB4V0	Y7	IO94PDB5V1
V17	TDI	Y8	VCC
V18	GNDQ	Y9	VCC
V19	TDO	Y10	IO89PDB5V0
V20	GND	Y11	IO80PDB4V1
V21	NC	Y12	IO78NPB4V1
V22	IO63NDB3V1	Y13	NC
W1	NC	Y14	VCC
W2	NC	Y15	VCC
W3	NC	Y16	NC
W4	GND	Y17	NC
W5	IO100NDB5V2	Y18	GND
W6	FF/GEB2/IO100PDB5V2	Y19	NC
W7	IO99NDB5V2	Y20	NC
W8	IO88NDB5V0	Y21	NC
W9	IO88PDB5V0	Y22	VCCIB3
W10	IO89NDB5V0		
W11	IO80NDB4V1		
W12	IO81NDB4V1		
W13	IO81PDB4V1		
W14	IO70NDB4V0		

W15

GDC2/IO70PDB4V0

Revision	Changes	Page
Advance v0.4 (December 2007)	The Table 1 • IGLOOe Product Family table was updated to change the maximum number of user I/Os for AGLE3000.	
	The "IGLOOe FPGAs Package Sizes Dimensions" table table is new. Package dimensions were removed from the "I/Os Per Package <sup>1</sup> " table. The number of I/Os was updated for FG896.	II
	A note regarding marking information was added to the "IGLOOe Ordering Information" table.	
	Table 2-4 • IGLOOe CCC/PLL Specification and Table 2-5 • IGLOOe CCC/PLL         Specification were updated.	2-18, 2-19
	The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core.	2-60
	Figure 2-38 • Flash*Freeze Mode Type 1 – Timing Diagram was updated to modify the LSICC signal.	2-56
	Table 2-32 • Flash*Freeze Pin Location in IGLOOe Family Packages (device-independent) was updated for the FG896 package.	2-64
	Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal.	2-58
	Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section.	3-6
	Table 3-8 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode† was updated.	3-6
	Table 3-9 • Quiescent Supply Current (IDD), IGLOOe Sleep Mode (VCC = 0 V)† was updated.	3-6
	Table 3-11 • Quiescent Supply Current, No IGLOOe Flash*Freeze Mode1 was updated.	3-6
	Table 3-99 • Minimum and Maximum DC Input and Output Levels was updated.	3-51
	Table 3-136 • JTAG 1532 and Table 3-135 • JTAG 1532 were updated.	3-95
	The "484-Pin FBGA" table for AGLE3000 is new.	4-11
	The "896-Pin FBGA" package and table for AGLE3000 is new.	4-16
Advance v0.3 (September 2007)	Cortex-M1 device information was added to the Table 1 • IGLOOe Product Family table, the "I/Os Per Package 1" table, "IGLOOe Ordering Information", and "Temperature Grade Offerings".	I, II, III, IV
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOOe Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections.	III, IV
	The T <sub>J</sub> parameter in Table 3-2 $\bullet$ Recommended Operating Conditions was changed to T <sub>A</sub> , ambient temperature, and table notes 6–8 were added.	3-2



### **Datasheet Categories**

### Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOOe Device Status" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Production

This version contains information that is considered to be final.

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