Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agle3000v5-fgg896i

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

IGLOOe Ordering Information

AGLE3000 V2 – FG G 896 Y I

Application (Temperature Range)
- Blank = Commercial (0°C to +70°C Ambient Temperature)
- I = Industrial (–40°C to +85°C Ambient Temperature)
- PP = Pre-Production
- ES = Engineering Sample (Room Temperature Only)

Security Feature
- Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
- Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Package Lead Count

Lead-Free Packaging
- Blank = Standard Packaging
- G = RoHS-Compliant Packaging

Package Type
- FG = Fine Pitch Ball Grid Array (1.0 mm pitch)

Supply Voltage
- 2 = 1.2 V to 1.5 V
- 5 = 1.5 V only

Part Number

IGLOOe Devices
- AGLE600 = 600,000 System Gates
- AGLE3000 = 3,000,000 System Gates

IGLOOe Devices with Cortex-M1
- M1AGLE3000 = 3,000,000 System Gates

Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.

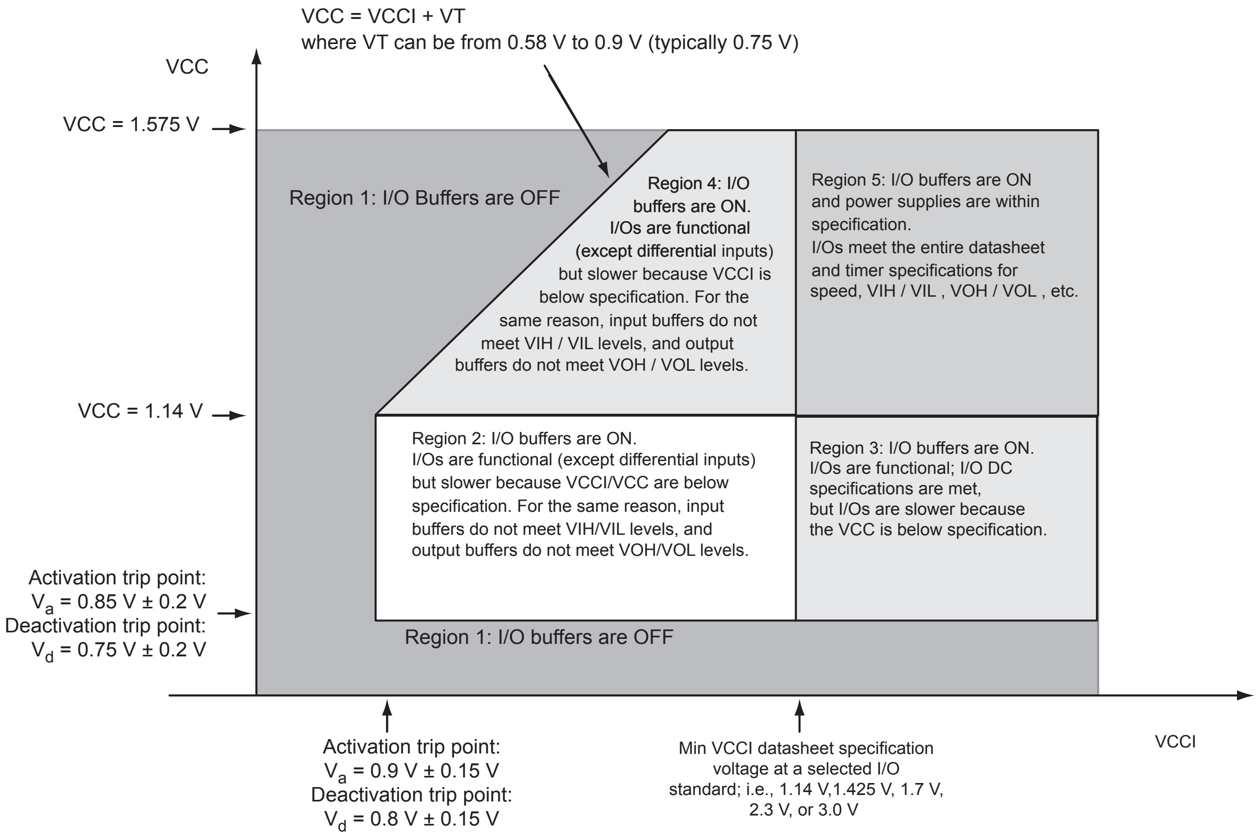


Figure 2-2 • **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels (continued) Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
HSTL (II)	15 mA[5]	15 mA[5]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
5. *Output drive strength is below JEDEC specification.*
6. *Output Slew Rates can be extracted from IBIS Models, http://www.microsemi.com/soc/download/ibis/default.aspx.*

Table 2-22 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[5]	10	10	15	15
1.2 V LVCOMS Wide Range[5]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Applicable to V2 devices operating at VCCI ≥ VCC.*

Timing Characteristics

1.5 V DC Core Voltage

**Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	7.33	0.18	1.27	1.59	0.66	7.47	6.18	2.34	1.18	11.07	9.77	ns
4 mA	Std.	0.97	6.07	0.18	1.27	1.59	0.66	6.20	5.25	2.69	2.42	9.79	8.84	ns
6 mA	Std.	0.97	5.18	0.18	1.27	1.59	0.66	5.29	4.61	2.93	2.88	8.88	8.21	ns
8 mA	Std.	0.97	4.88	0.18	1.27	1.59	0.66	4.98	4.48	2.99	3.01	8.58	8.08	ns
12 mA	Std.	0.97	4.80	0.18	1.27	1.59	0.66	4.89	4.49	3.07	3.47	8.49	8.09	ns
16 mA	Std.	0.97	4.80	0.18	1.27	1.59	0.66	4.89	4.49	3.07	3.47	8.49	8.09	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.43	0.18	1.27	1.59	0.66	3.51	3.39	2.33	1.19	7.10	6.98	ns
4 mA	Std.	0.97	2.83	0.18	1.27	1.59	0.66	2.89	2.59	2.69	2.49	6.48	6.18	ns
6 mA	Std.	0.97	2.45	0.18	1.27	1.59	0.66	2.51	2.19	2.93	2.95	6.10	5.79	ns
8 mA	Std.	0.97	2.38	0.18	1.27	1.59	0.66	2.43	2.12	2.98	3.08	6.03	5.71	ns
12 mA	Std.	0.97	2.37	0.18	1.27	1.59	0.66	2.42	2.03	3.07	3.57	6.02	5.62	ns
16 mA	Std.	0.97	2.37	0.18	1.27	1.59	0.66	2.42	2.03	3.07	3.57	6.02	5.62	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	7.61	0.18	1.47	1.77	0.66	7.76	6.33	2.81	2.34	11.36	9.92	ns
4 mA	Std.	0.97	6.54	0.18	1.47	1.77	0.66	6.67	5.56	3.09	2.88	10.26	9.16	ns
6 mA	Std.	0.97	6.15	0.18	1.47	1.77	0.66	6.27	5.42	3.15	3.02	9.87	9.02	ns
8 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns
12 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.47	1.77	0.66	3.32	3.00	2.80	2.43	6.92	6.59	ns
4 mA	Std.	0.97	2.81	0.18	1.47	1.77	0.66	2.87	2.51	3.08	2.97	6.46	6.10	ns
6 mA	Std.	0.97	2.72	0.18	1.47	1.77	0.66	2.78	2.41	3.14	3.12	6.37	6.01	ns
8 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns
12 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-122* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note: *See Figure 2-27 on page 2-68 for more information.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-135 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y = !(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	Y = A ⊕ B	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.33	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-136 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.35	ns
AND2	Y = A · B	t_{PD}	1.42	ns
NAND2	Y = !(A · B)	t_{PD}	1.58	ns
OR2	Y = A + B	t_{PD}	2.10	ns
NOR2	Y = !(A + B)	t_{PD}	1.94	ns
XOR2	Y = A ⊕ B	t_{PD}	2.33	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.34	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.05	ns
MUX2	Y = A !S + B S	t_{PD}	2.64	ns
AND3	Y = A · B · C	t_{PD}	2.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

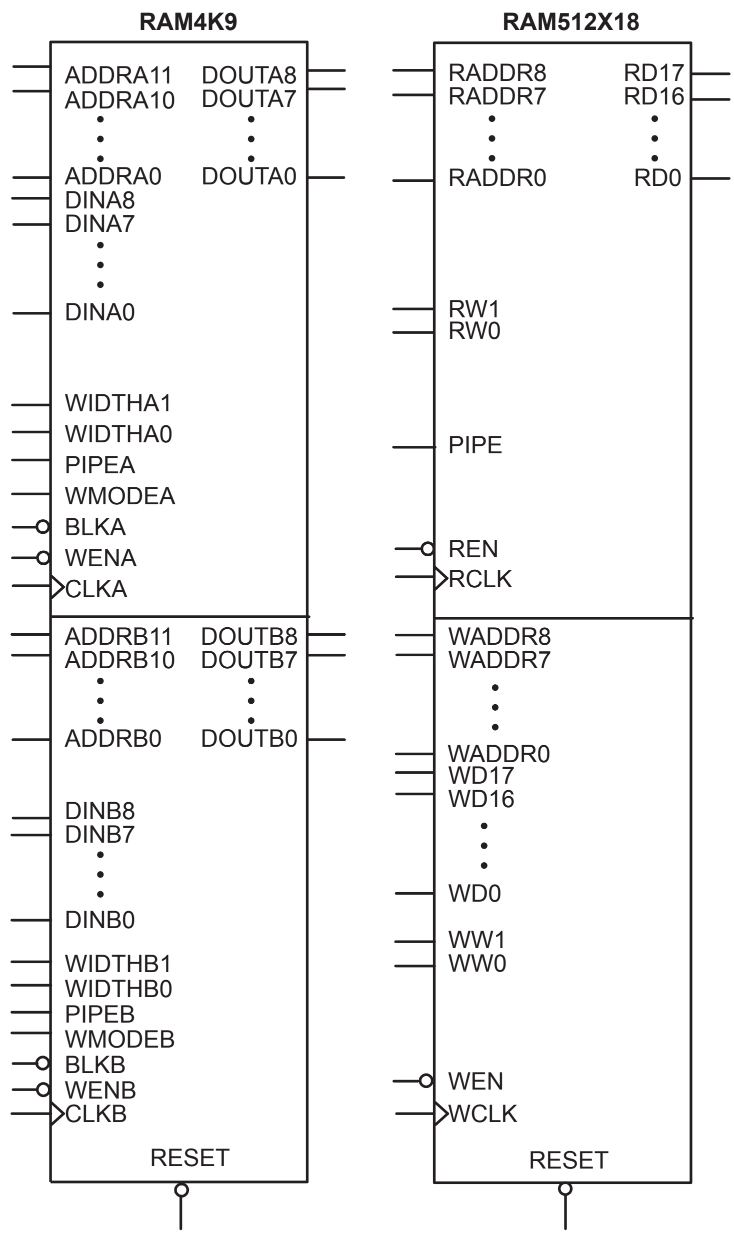


***Figure 2-41* • RAM Models**

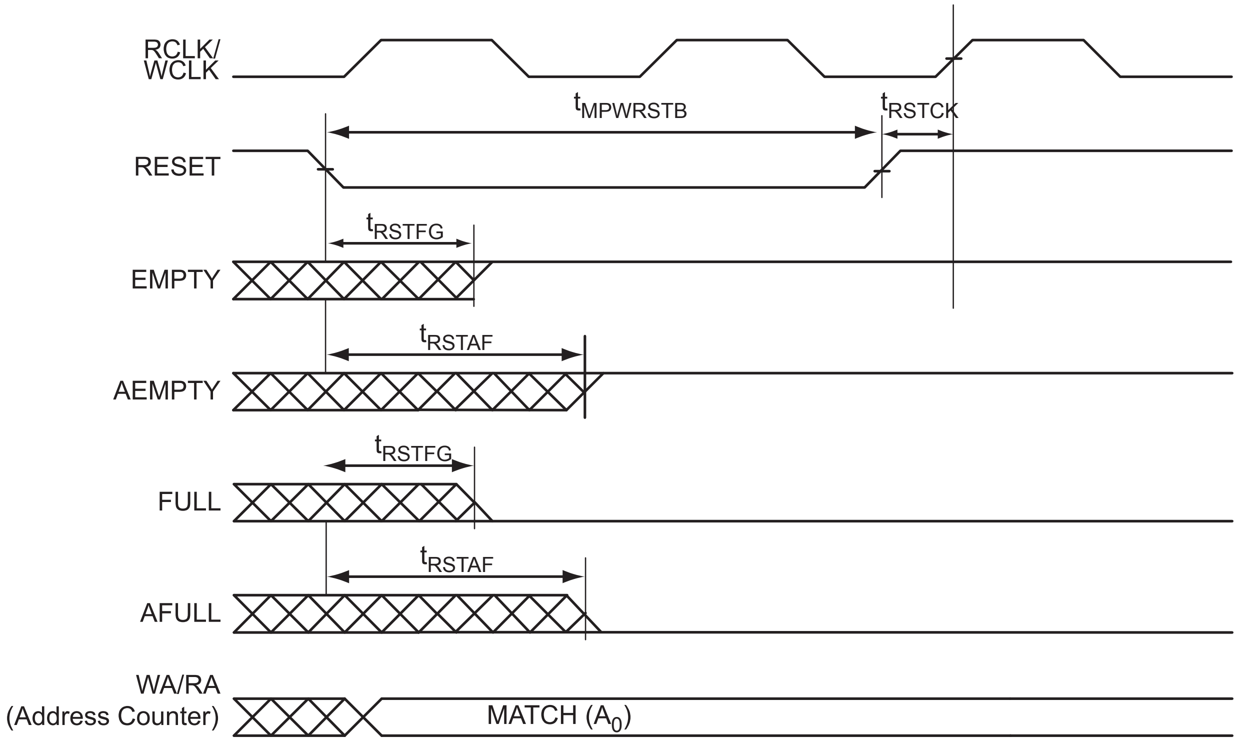


Figure 2-50 **• FIFO Reset**

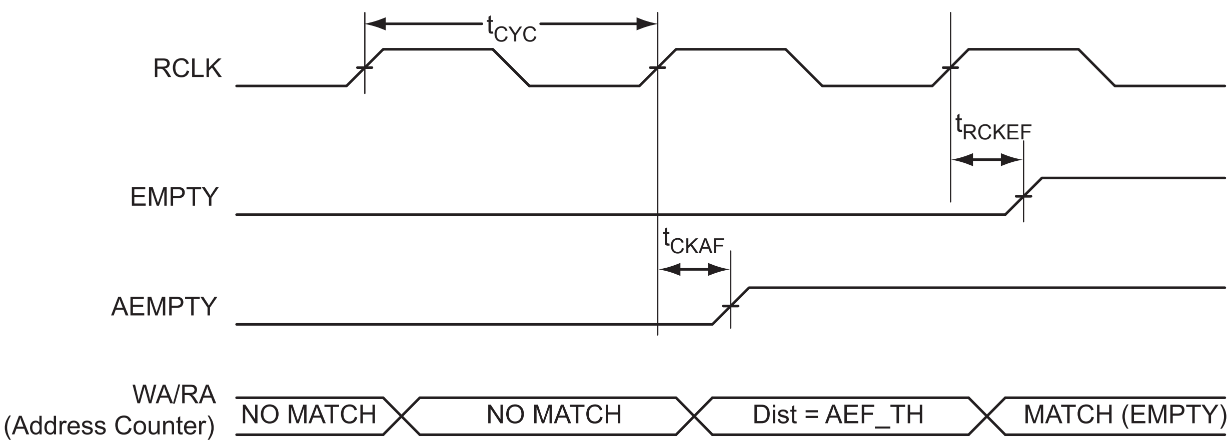


Figure 2-51 **• FIFO EMPTY Flag and AEMPTY Flag Assertion**

Embedded FlashROM Characteristics

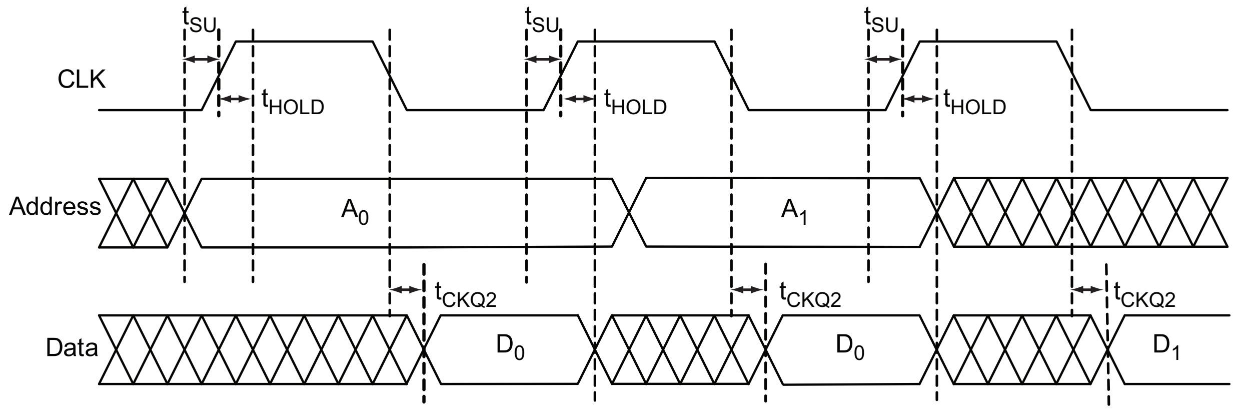


Figure 2-55 • **Timing Diagram**

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-151 • **Embedded FlashROM Access Time**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.58	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock-to-Out	34.14	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

Applies to 1.2 V DC Core Voltage

Table 2-152 • **Embedded FlashROM Access Time**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock-to-Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOOe FPGA Fabric User’s Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the *IGLOOe FPGA Fabric User’s Guide* for an explanation of the naming of global pins.

FF **Flash*Freeze Mode Activation Pin**

Flash*Freeze mode is available on IGLOOe devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O. The FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-3 • **TRST and TCK Pull-Down Recommendations**

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

FG256	
Pin Number	**AGLE600 Function**
A1	GND
A2	GAA0/IO00NDB0V0
A3	GAA1/IO00PDB0V0
A4	GAB0/IO01NDB0V0
A5	IO05PDB0V0
A6	IO10PDB0V1
A7	IO12PDB0V2
A8	IO16NDB0V2
A9	IO23NDB1V0
A10	IO23PDB1V0
A11	IO28NDB1V1
A12	IO28PDB1V1
A13	GBB1/IO34PDB1V1
A14	GBA0/IO35NDB1V1
A15	GBA1/IO35PDB1V1
A16	GND
B1	GAB2/IO133PDB7V1
B2	GAA2/IO134PDB7V1
B3	GNDQ
B4	GAB1/IO01PDB0V0
B5	IO05NDB0V0
B6	IO10NDB0V1
B7	IO12NDB0V2
B8	IO16PDB0V2
B9	IO20NDB1V0
B10	IO24NDB1V0
B11	IO24PDB1V0
B12	GBC1/IO33PDB1V1
B13	GBB0/IO34NDB1V1
B14	GNDQ
B15	GBA2/IO36PDB2V0
B16	IO42NDB2V0
C1	IO133NDB7V1
C2	IO134NDB7V1
C3	VMV7
C4	VCCPLA

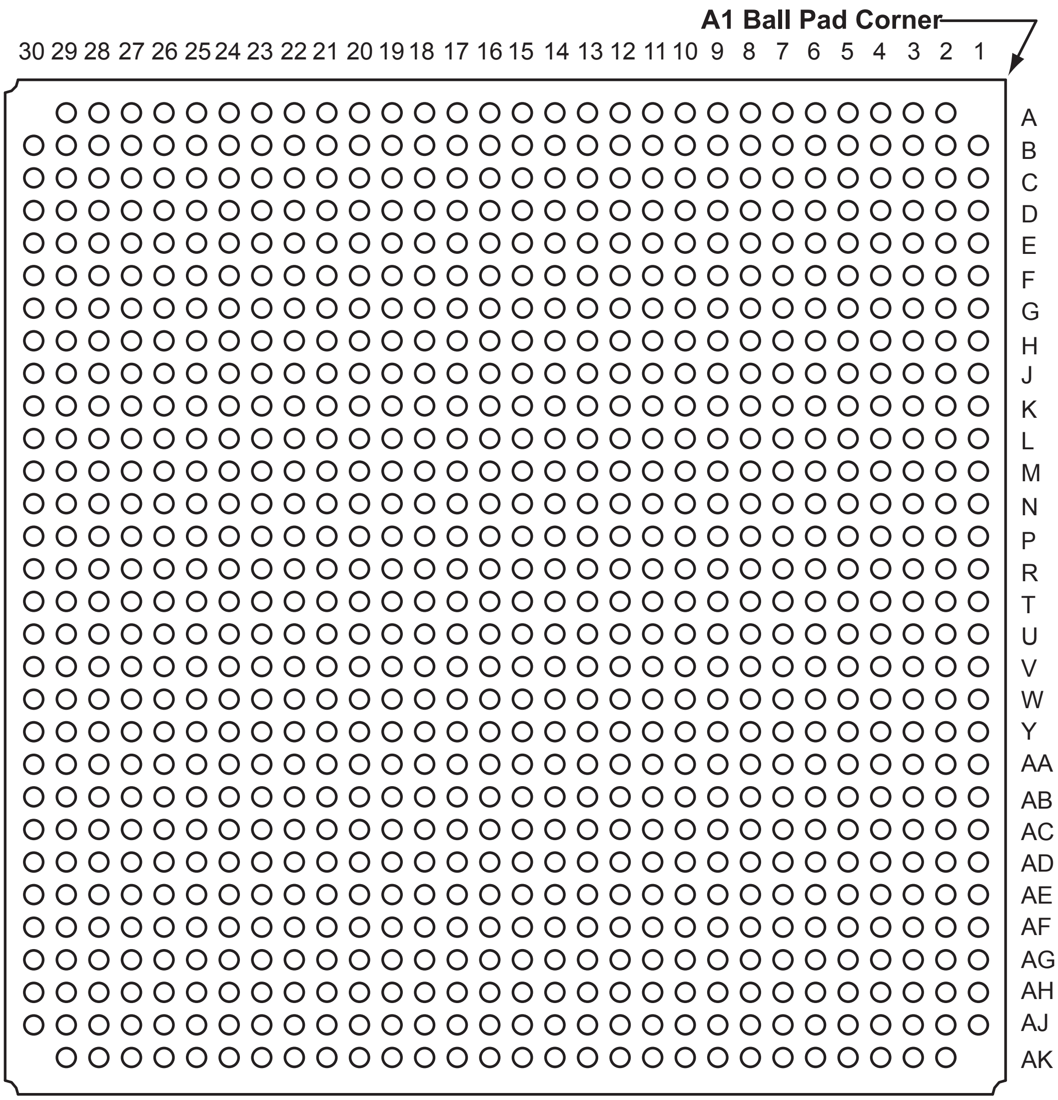
FG256	
Pin Number	**AGLE600 Function**
C5	GAC0/IO02NDB0V0
C6	GAC1/IO02PDB0V0
C7	IO15NDB0V2
C8	IO15PDB0V2
C9	IO20PDB1V0
C10	IO25NDB1V0
C11	IO27PDB1V0
C12	GBC0/IO33NDB1V1
C13	VCCPLB
C14	VMV2
C15	IO36NDB2V0
C16	IO42PDB2V0
D1	IO128PDB7V1
D2	IO129PDB7V1
D3	GAC2/IO132PDB7V1
D4	VCOMPLA
D5	GNDQ
D6	IO09NDB0V1
D7	IO09PDB0V1
D8	IO13PDB0V2
D9	IO21PDB1V0
D10	IO25PDB1V0
D11	IO27NDB1V0
D12	GNDQ
D13	VCOMPLB
D14	GBB2/IO37PDB2V0
D15	IO39PDB2V0
D16	IO39NDB2V0
E1	IO128NDB7V1
E2	IO129NDB7V1
E3	IO132NDB7V1
E4	IO130PDB7V1
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO13NDB0V2

FG256	
Pin Number	**AGLE600 Function**
E9	IO21NDB1V0
E10	VCCIB1
E11	VCCIB1
E12	VMV1
E13	GBC2/IO38PDB2V0
E14	IO37NDB2V0
E15	IO41NDB2V0
E16	IO41PDB2V0
F1	IO124PDB7V0
F2	IO125PDB7V0
F3	IO126PDB7V0
F4	IO130NDB7V1
F5	VCCIB7
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB2
F13	IO38NDB2V0
F14	IO40NDB2V0
F15	IO40PDB2V0
F16	IO45PSB2V1
G1	IO124NDB7V0
G2	IO125NDB7V0
G3	IO126NDB7V0
G4	GFC1/IO120PPB7V0
G5	VCCIB7
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB2

FG484	
Pin Number	AGLE3000 Function
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0

FG484	
Pin Number	AGLE3000 Function
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	VCCIB6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	VCC
Y9	VCC
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	VCC
Y15	VCC
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	VCCIB3

FG896



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG896	
Pin Number	AGLE3000 Function
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1

FG896	
Pin Number	AGLE3000 Function
AD22	VCCIB4
AD23	TCK
AD24	VCC
AD25	TRST
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND

FG896	
Pin Number	AGLE3000 Function
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	VCC
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ

FG896	
Pin Number	AGLE3000 Function
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	VCC
B5	IO14PPB0V1
B6	VCC
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2

FG896	
Pin Number	AGLE3000 Function
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	VCC
B26	GBC0/IO79NPB1V4
B27	VCC
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	VCC
C4	GAA0/IO00NPB0V0
C5	VCCIB0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4

FG896	
Pin Number	AGLE3000 Function
C25	IO75PDB1V4
C26	VCCIB1
C27	IO64PPB1V2
C28	VCC
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	VCC
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	VCC

FG896	
Pin Number	AGLE3000 Function
R11	VCC
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	VCC
R21	VCCIB2
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	VCOMPLC
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4
T2	VCCPLF
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	VCCIB6
T11	VCC
T12	GND
T13	GND
T14	GND
T15	GND

FG896	
Pin Number	AGLE3000 Function
T16	GND
T17	GND
T18	GND
T19	GND
T20	VCC
T21	VCCIB3
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	VCCPLC
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC

FG896	
Pin Number	AGLE3000 Function
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	VCC
V21	VCCIB3
V22	IO120NDB3V0
V23	IO128NDB3V1
V24	IO132PDB3V2
V25	IO130PPB3V2