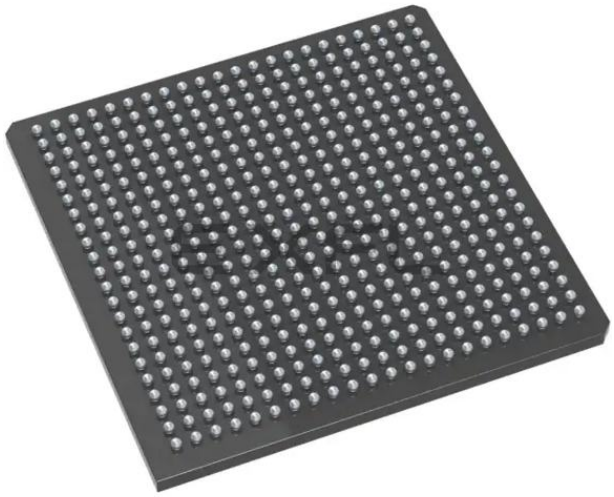

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	270
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agle600v2-fg484i

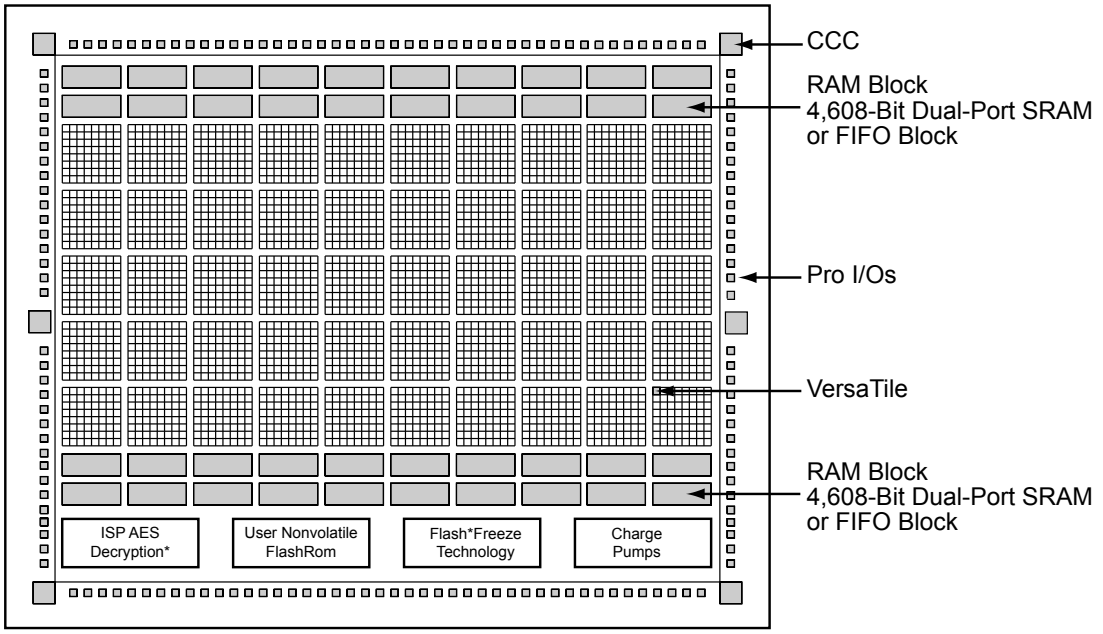

Figure 1-1 • **IGLOOe Device Architecture Overview**

*Flash*Freeze Technology*

The IGLOOe device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static and dynamic capabilities of the IGLOOe device. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode.

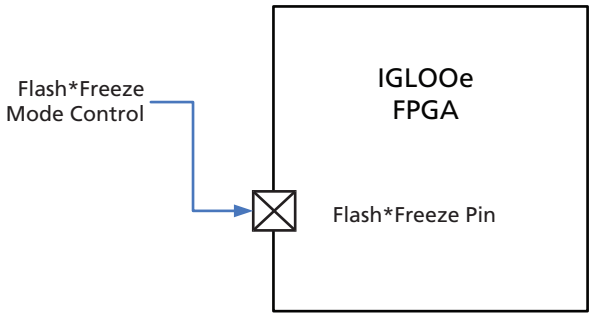

Figure 1-2 • **IGLOOe Flash*Freeze Mode**

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient Temperature		0 to +70	–40 to +85	°C
T_J	Junction Temperature[2]		0 to + 85	–40 to +100	°C
VCC [3]	1.5 V DC core supply voltage[4]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core voltage[5, 6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage[6]	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[4]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V DC core supply voltage[5]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV[9]	1.2 V DC supply voltage[5]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V wide range DC supply voltage[5]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage[10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-20. VCCI should be at the same voltage within a given I/O bank.*
4. *For IGLOOe V5 devices*
5. *For IGLOOe V2 devices only, operating at VCCI ≥ VCC*
6. *All IGLOOe devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "VCCPLA/B/C/D/E/F PLL Supply Voltage" section for further information.*
9. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section for further information.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{13.6\text{°C/W}} = 2.206\ \text{W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C,VCC = 1.425 V) For IGLOOe V2 or V5 devices, 1.5 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.945	0.965	0.978	1.000	1.008	1.013
1.500	0.876	0.893	0.906	0.927	0.934	0.940
1.575	0.824	0.840	0.852	0.872	0.879	0.884

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.14 V) For IGLOOe V2, 1.2 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.968	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.873	0.885	0.893	0.898	0.902
1.26	0.793	0.803	0.813	0.821	0.826	0.829

Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1]

	Core Voltage	AGLE600	AGLE3000	Units
ICCA Current[2]				
Typical (25°C)	1.2 V	28	89	µA
	1.5 V	82	320	µA
ICCI or IJTAG Current[3]				
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI/VJTAG= 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

Notes:

1. *IDD = N_{BANKS} × ICCI + ICCA. JTAG counts as one bank when powered.*
2. *Includes VCC and VPUMP and VCCPLL currents.*
3. *Values do not include I/O static contribution (PDC6 and PDC7).*

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-15.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-20 on page 2-15.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-20 on page 2-15.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-20 on page 2-15.

PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

1.2 V DC Core Voltage

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.54	0.26	1.31	1.58	1.10	5.63	4.53	2.79	2.87	11.42	10.32	ns
8 mA	Std.	1.55	4.60	0.26	1.31	1.58	1.10	4.67	3.94	3.09	3.45	10.45	9.73	ns
12 mA	Std.	1.55	3.93	0.26	1.31	1.58	1.10	3.99	3.51	3.28	3.82	9.77	9.29	ns
16 mA	Std.	1.55	3.74	0.26	1.31	1.58	1.10	3.79	3.41	3.32	3.92	9.58	9.20	ns
24 mA	Std.	1.55	3.64	0.26	1.31	1.58	1.10	3.69	3.42	3.38	4.30	9.48	9.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.26	0.26	1.31	1.58	1.10	3.33	2.67	2.79	3.01	9.12	8.46	ns
8 mA	Std.	1.55	2.77	0.26	1.31	1.58	1.10	2.80	2.24	3.09	3.59	8.59	8.03	ns
12 mA	Std.	1.55	2.47	0.26	1.31	1.58	1.10	2.51	2.04	3.28	3.97	8.29	7.82	ns
16 mA	Std.	1.55	2.42	0.26	1.31	1.58	1.10	2.46	2.00	3.33	4.08	8.24	7.79	ns
24 mA	Std.	1.55	2.45	0.26	1.31	1.58	1.10	2.48	1.95	3.38	4.46	8.26	7.73	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-48 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	5.55	0.18	1.31	1.41	0.66	5.66	4.75	2.28	1.96	9.26	8.34	ns
8 mA	Std.	0.97	4.58	0.18	1.31	1.41	0.66	4.67	4.07	2.58	2.53	8.27	7.66	ns
12 mA	Std.	0.97	3.89	0.18	1.31	1.41	0.66	3.97	3.58	2.78	2.91	7.56	7.17	ns
16 mA	Std.	0.97	3.68	0.18	1.31	1.41	0.66	3.75	3.47	2.82	3.01	7.35	7.06	ns
24 mA	Std.	0.97	3.59	0.18	1.31	1.41	0.66	3.66	3.48	2.88	3.37	7.26	7.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-49 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.94	0.18	1.31	1.41	0.66	3.00	2.68	2.28	2.03	6.60	6.27	ns
8 mA	Std.	0.97	2.45	0.18	1.31	1.41	0.66	2.50	2.12	2.58	2.62	6.10	5.72	ns
12 mA	Std.	0.97	2.15	0.18	1.31	1.41	0.66	2.20	1.85	2.78	2.98	5.80	5.45	ns
16 mA	Std.	0.97	2.10	0.18	1.31	1.41	0.66	2.15	1.80	2.82	3.08	5.75	5.40	ns
24 mA	Std.	0.97	2.11	0.18	1.31	1.41	0.66	2.16	1.74	2.88	3.47	5.75	5.33	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	9.92	0.26	2.09	2.95	1.10	9.53	7.48	4.02	3.67	15.31	13.26	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range[1]		VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[4]	Min. (V)	Max. (V)	Min. (V)	Max (V)	Max. (V)	Min. (V)	µA	µA	Max. (mA)[5]	Max. (mA)[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. *Applicable to V2 devices ONLY.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI . Input current is larger when operating outside recommended ranges.*
4. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-48 for worst-case timing.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-105 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
14 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14	51	54	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

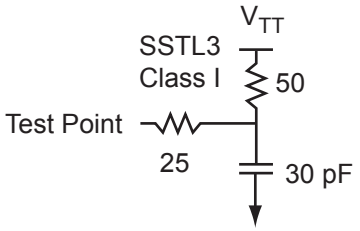

Figure 2-21 • AC Loading

Table 2-106 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-107 • SSTL 3 Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.05	0.19	1.09	0.67	2.09	1.71			5.72	5.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-108 • SSTL 3 Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.32	0.26	1.32	1.10	2.37	2.02			8.17	7.83	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

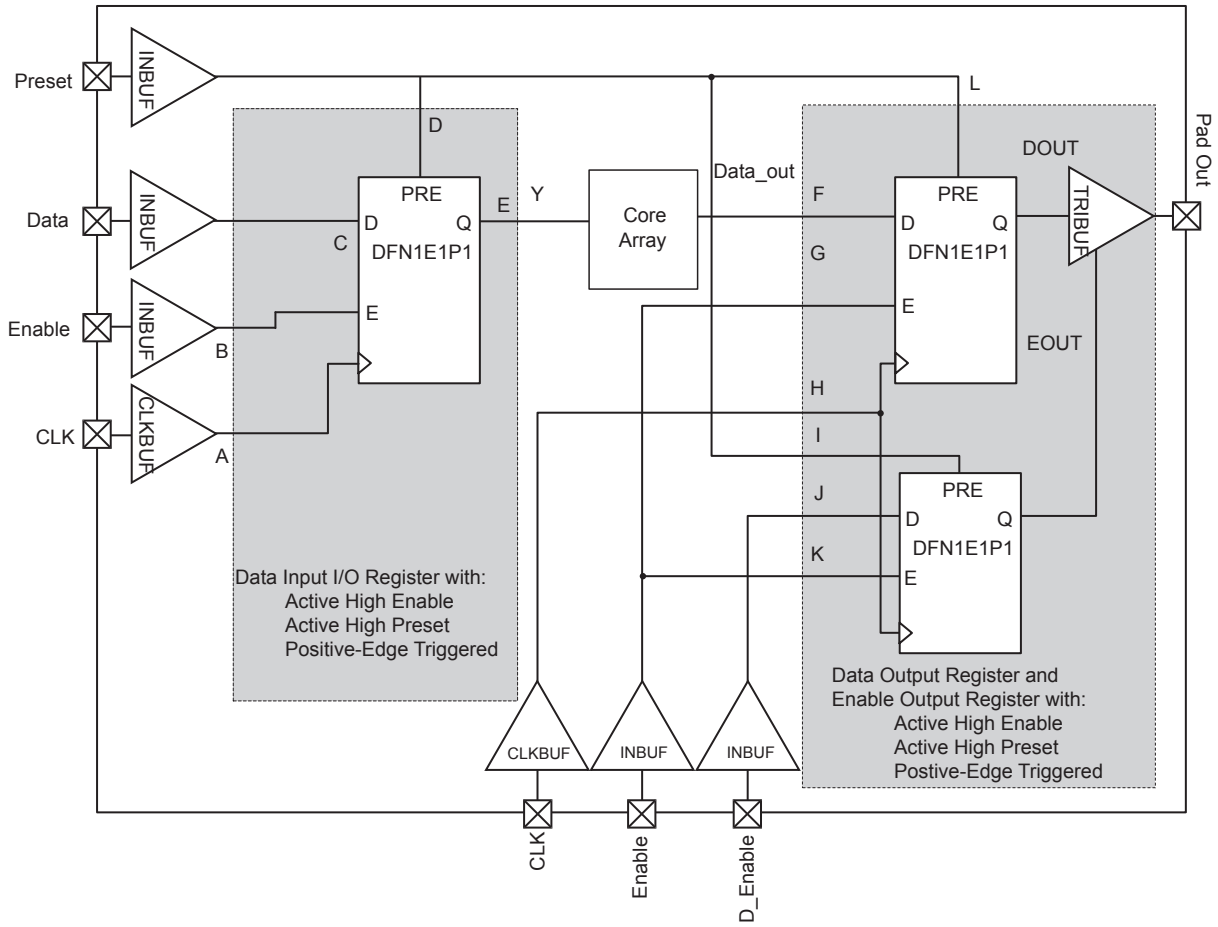

Figure 2-26 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Output Enable Register

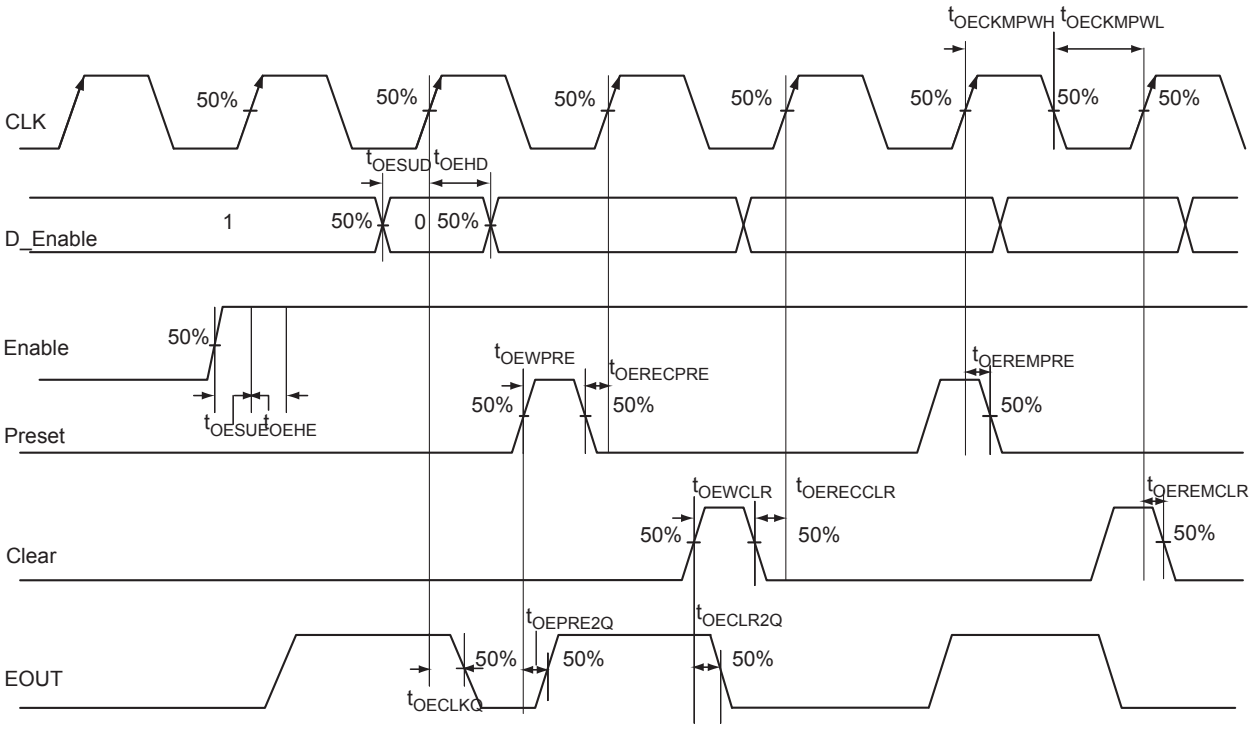

Figure 2-30 • **Output Enable Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-127 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.73	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output DDR Module

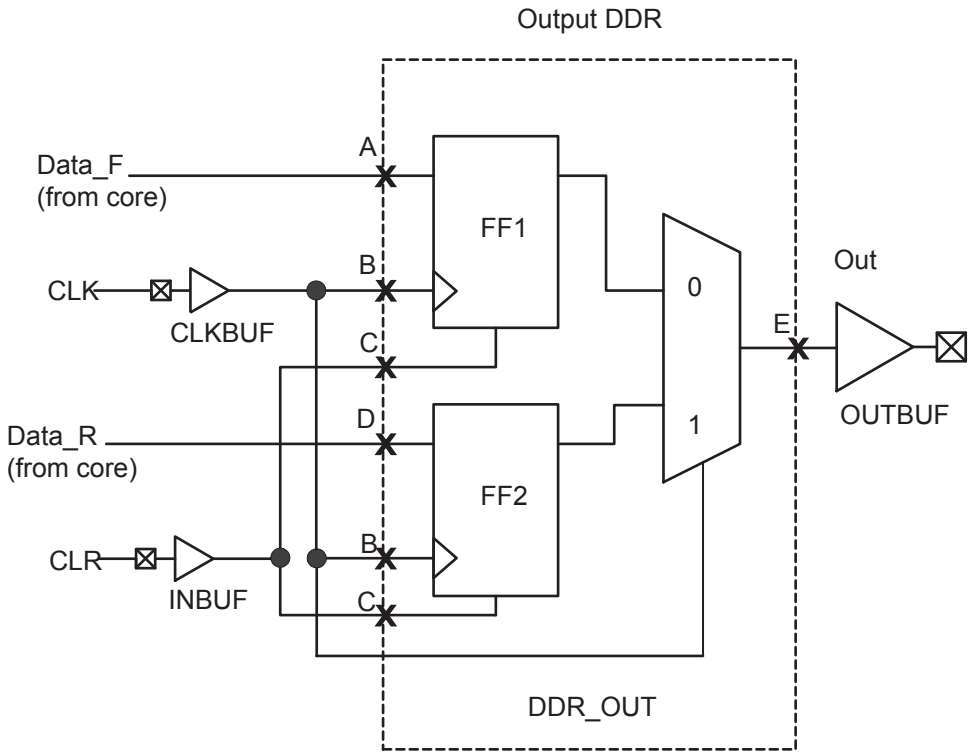

Figure 2-33 • **Output DDR Timing Model**

Table 2-132 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Global Resource Characteristics

AGLE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-39 is an example of a global tree used for clock routing. The global tree presented in Figure 2-39 is driven by a CCC located on the west side of the AGLE600 device. It is used to drive all D-flip-flops in the device.

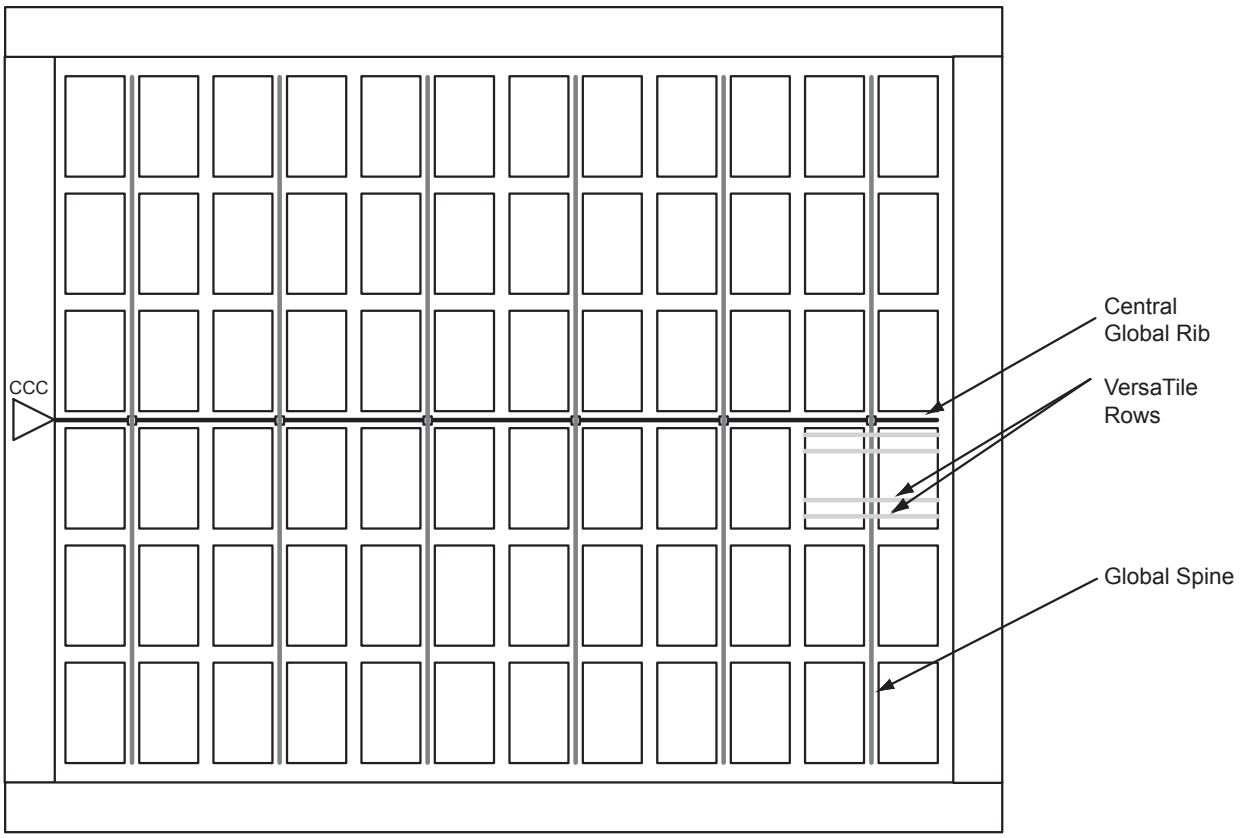

Figure 2-39 • **Example of Global Tree Use in an AGLE600 Device for Clock Routing**

Embedded SRAM and FIFO Characteristics

SRAM

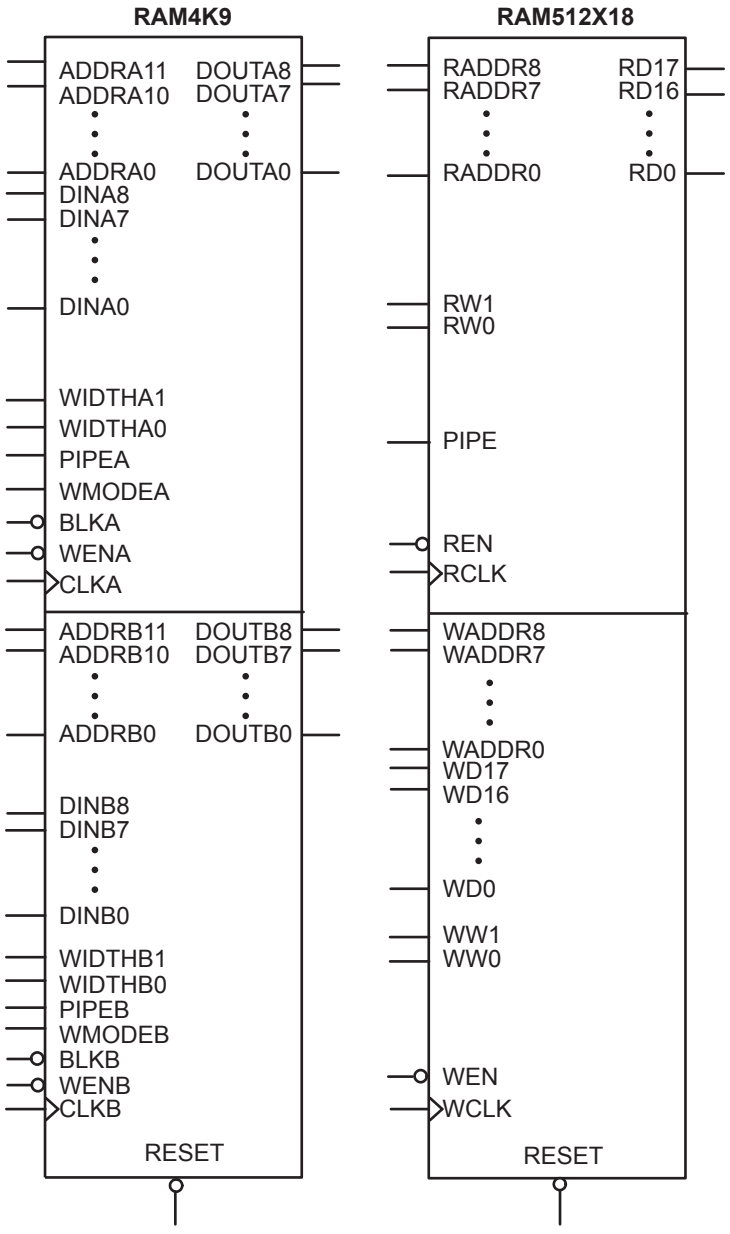

Figure 2-41 • **RAM Models**

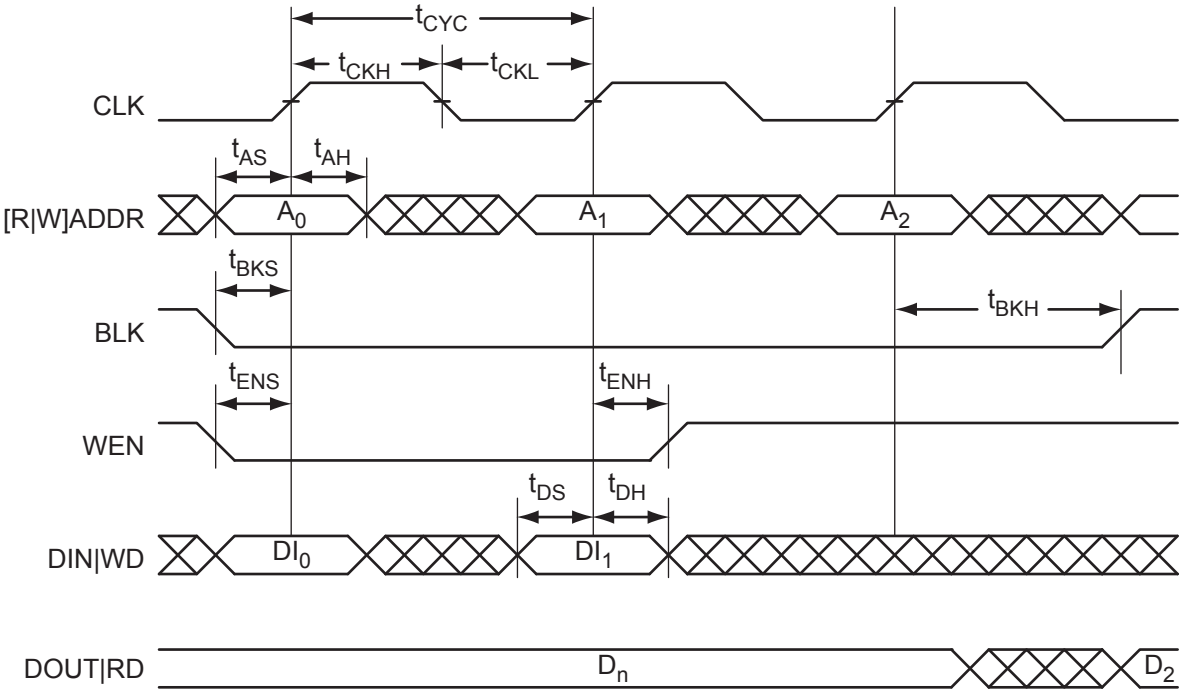

Figure 2-44 • **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512X18.**

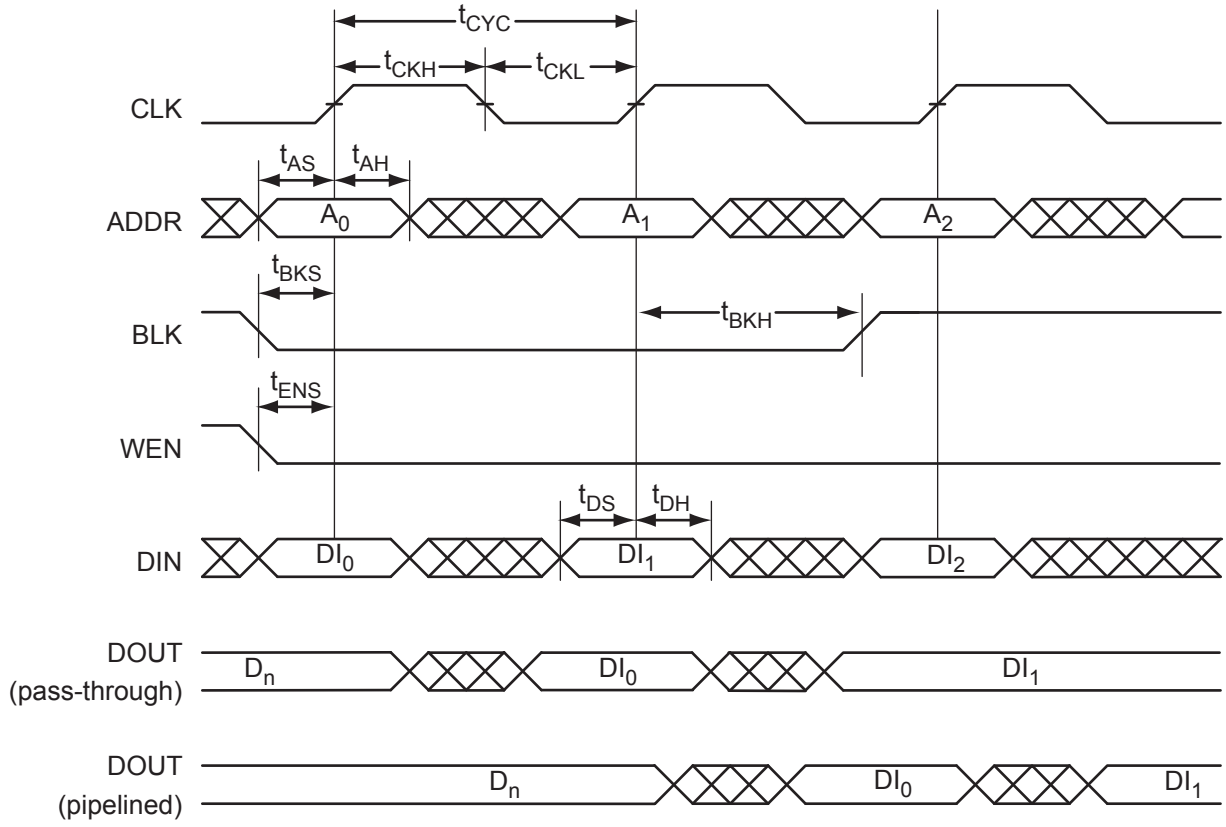

Figure 2-45 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOOe V5 devices, and 1.2 V or 1.5 V for IGLOOe V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOOe V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOOe devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device.

- 1.5 V for IGLOOe devices
- 1.2 V or 1.5 V for IGLOOe V2 devices

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section in the "Clock Conditioning Circuits in Low Power Flash FPGAs and Mixed Signal FPGAs" chapter in the *IGLOOe FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on IGLOOe devices.

Related Documents

User's Guides

IGLOOe FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/IGLOOe_UG.pdf

Packaging Documents

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: http://www.microsemi.com/soc/products/solutions/package/docs.aspx.