Microsemi Corporation - AGLE600V2-FGG484 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	270
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agle600v2-fgg484

Table of Contents

1 – IGLOOe Device Family Overview

General Description

The IGLOOe family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOOe devices enables entering and exiting an ultra-low power mode while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOOe device is completely functional in the system. This allows the IGLOOe device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOOe devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOOe is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOOe devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on 6 integrated phase-locked loops (PLLs). IGLOOe devices have up to 3 million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

M1 IGLOOe devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOOe device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Microsemi for use in M1 IGLOOe FPGAs.

The ARM-enabled devices have Microsemi ordering numbers that begin with M1AGLE and do not support AES decryption.

Flash*Freeze Technology

The IGLOOe device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOOe devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOOe V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOOe device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOOe devices the best fit for portable electronics.

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{100°C - 70°C}{13.6°C/W} = 2.206\ \text{W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C,VCC = 1.425 V) For IGLOOe V2 or V5 devices, 1.5 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.945	0.965	0.978	1.000	1.008	1.013
1.500	0.876	0.893	0.906	0.927	0.934	0.940
1.575	0.824	0.840	0.852	0.872	0.879	0.884

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.14 V) For IGLOOe V2, 1.2 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.968	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.873	0.885	0.893	0.898	0.902
1.26	0.793	0.803	0.813	0.821	0.826	0.829

Table 2-17 • Different Components Contributing to the Dynamic Power Consumption in IGLOOe Devices For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)	
		AGLE600	AGLE3000
PAC1	Clock contribution of a Global Rib	12.61	8.17
PAC2	Clock contribution of a Global Spine	2.66	1.18
PAC3	Clock contribution of a VersaTile row	0.56	
PAC4	Clock contribution of a VersaTile used as a sequential module	0.071	
PAC5	First contribution of a VersaTile used as a sequential module	0.045	
PAC6	Second contribution of a VersaTile used as a sequential module	0.186	
PAC7	Contribution of a VersaTile used as a combinatorial module	0.109	
PAC8	Average contribution of a routing net	0.449	
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-9 on page 2-7.	
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-10 on page 2-7 and Table 2-11 on page 2-7.	
PAC11	Average contribution of a RAM block during a read operation	25.00	
PAC12	Average contribution of a RAM block during a write operation	30.00	
PAC13	Dynamic PLL contribution	2.10	

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC software.

Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Definition	Device Specific Static Power (mW)	
		AGLE600	AGLE3000
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8.	
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-7.	
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7.	
PDC4	Static PLL contribution	0.90	
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8.	
PDC6	I/O input pin static power (standard-dependent)	See Table 2-13 on page 2-9.	
PDC7	I/O output pin static power (standard-dependent)	See Table 2-14 on page 2-10.	

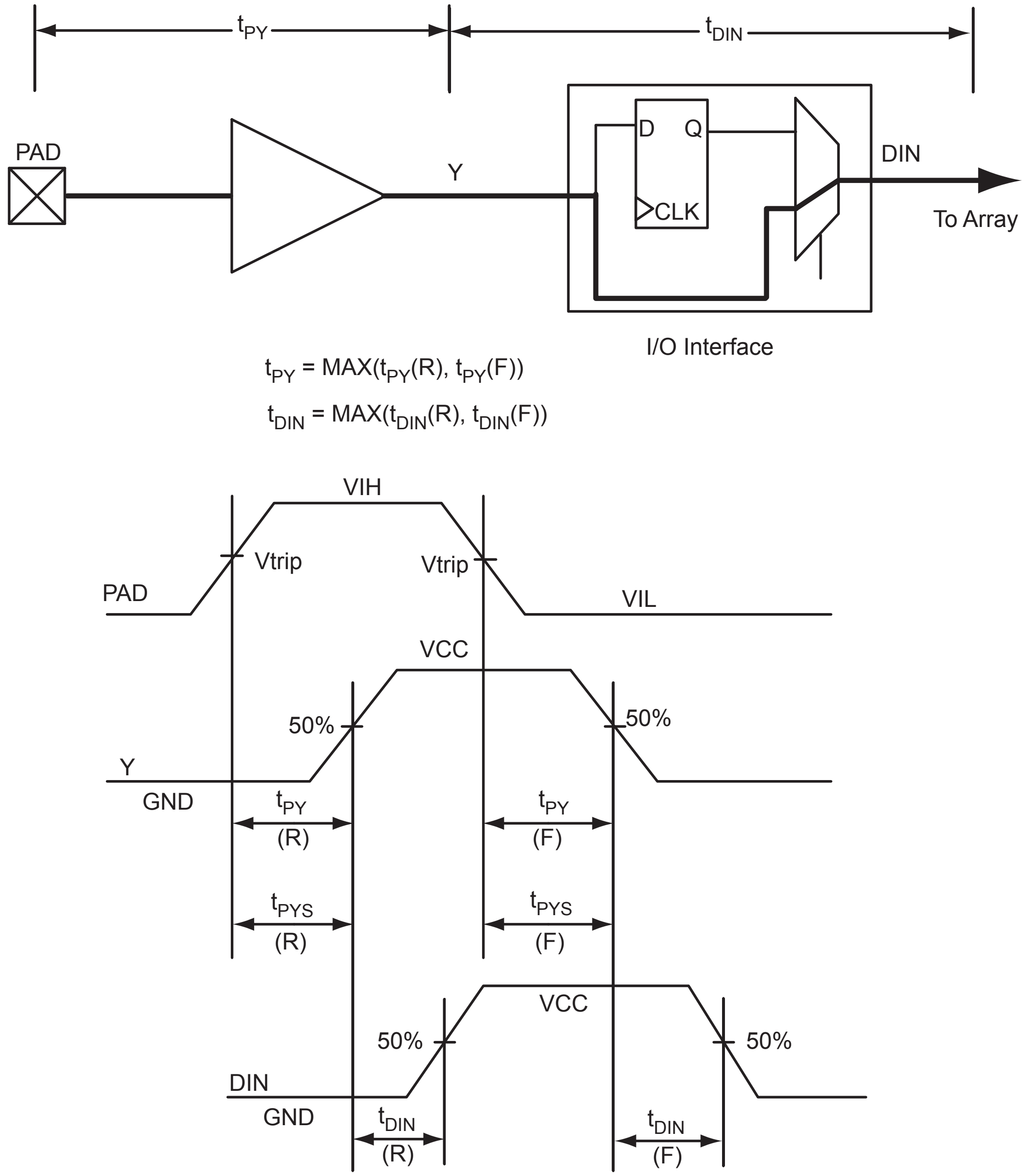

Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

Table 2-22 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
DC I/O Standards	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[5]	10	10	15	15
1.2 V LVCOMS Wide Range[5]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Applicable to V2 devices operating at VCCI ≥ VCC.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
3.3 V LVCMOS Wide Range	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
1.2 V LVCMOS*	–	–	0.6 V
1.2 V LVCMOS – Wide Range*	–	–	0.6 V
3.3 V PCI	–	–	0.285 * VCCI (RR)
	–	–	0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR)
	–	–	0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

*Note: *Applicable to V2 devices ONLY operating in the 1.2 V core range.*

1.2 V DC Core Voltage

Table 2-44 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	1.55	8.14	0.26	1.66	2.14	1.10	8.14	6.46	3.80	3.79	13.93	12.25	ns
100 µA	8 mA	Std.	1.55	6.68	0.26	1.66	2.14	1.10	6.68	5.57	4.25	4.69	12.47	11.36	ns
100 µA	12 mA	Std.	1.55	5.65	0.26	1.66	2.14	1.10	5.65	4.91	4.55	5.25	11.44	10.69	ns
100 µA	16 mA	Std.	1.55	5.36	0.26	1.66	2.14	1.10	5.36	4.76	4.61	5.41	11.14	10.55	ns
100 µA	24 mA	Std.	1.55	5.20	0.26	1.66	2.14	1.10	5.20	4.78	4.69	6.00	10.99	10.56	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-45 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	1.55	4.65	0.26	1.66	2.14	110	4.65	3.64	3.80	4.00	10.44	9.43	ns
100 µA	8 mA	Std.	1.55	3.85	0.26	1.66	2.14	1.10	3.85	2.99	4.25	4.91	9.64	8.77	ns
100 µA	12 mA	Std.	1.55	3.40	0.26	1.66	2.14	1.10	3.40	2.68	4.55	5.49	9.19	8.46	ns
100 µA	16 mA	Std.	1.55	3.33	0.26	1.66	2.14	1.10	3.33	2.62	4.62	5.65	9.11	8.41	ns
100 µA	24 mA	Std.	1.55	3.36	0.26	1.66	2.14	1.10	3.36	2.54	4.71	6.24	9.15	8.32	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Timing Characteristics

1.5 V DC Core Voltage

**Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	7.61	0.18	1.47	1.77	0.66	7.76	6.33	2.81	2.34	11.36	9.92	ns
4 mA	Std.	0.97	6.54	0.18	1.47	1.77	0.66	6.67	5.56	3.09	2.88	10.26	9.16	ns
6 mA	Std.	0.97	6.15	0.18	1.47	1.77	0.66	6.27	5.42	3.15	3.02	9.87	9.02	ns
8 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns
12 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.47	1.77	0.66	3.32	3.00	2.80	2.43	6.92	6.59	ns
4 mA	Std.	0.97	2.81	0.18	1.47	1.77	0.66	2.87	2.51	3.08	2.97	6.46	6.10	ns
6 mA	Std.	0.97	2.72	0.18	1.47	1.77	0.66	2.78	2.41	3.14	3.12	6.37	6.01	ns
8 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns
12 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-85 • **Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

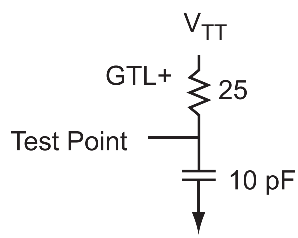

Figure 2-16 • **AC Loading**

Table 2-86 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-87 • **2.5 V GTL+ – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.97	0.19	1.29	0.67	2.00	1.84			5.63	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-88 • **2.5 V GTL+ – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.23	0.26	1.55	1.10	2.28	2.11			8.08	7.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

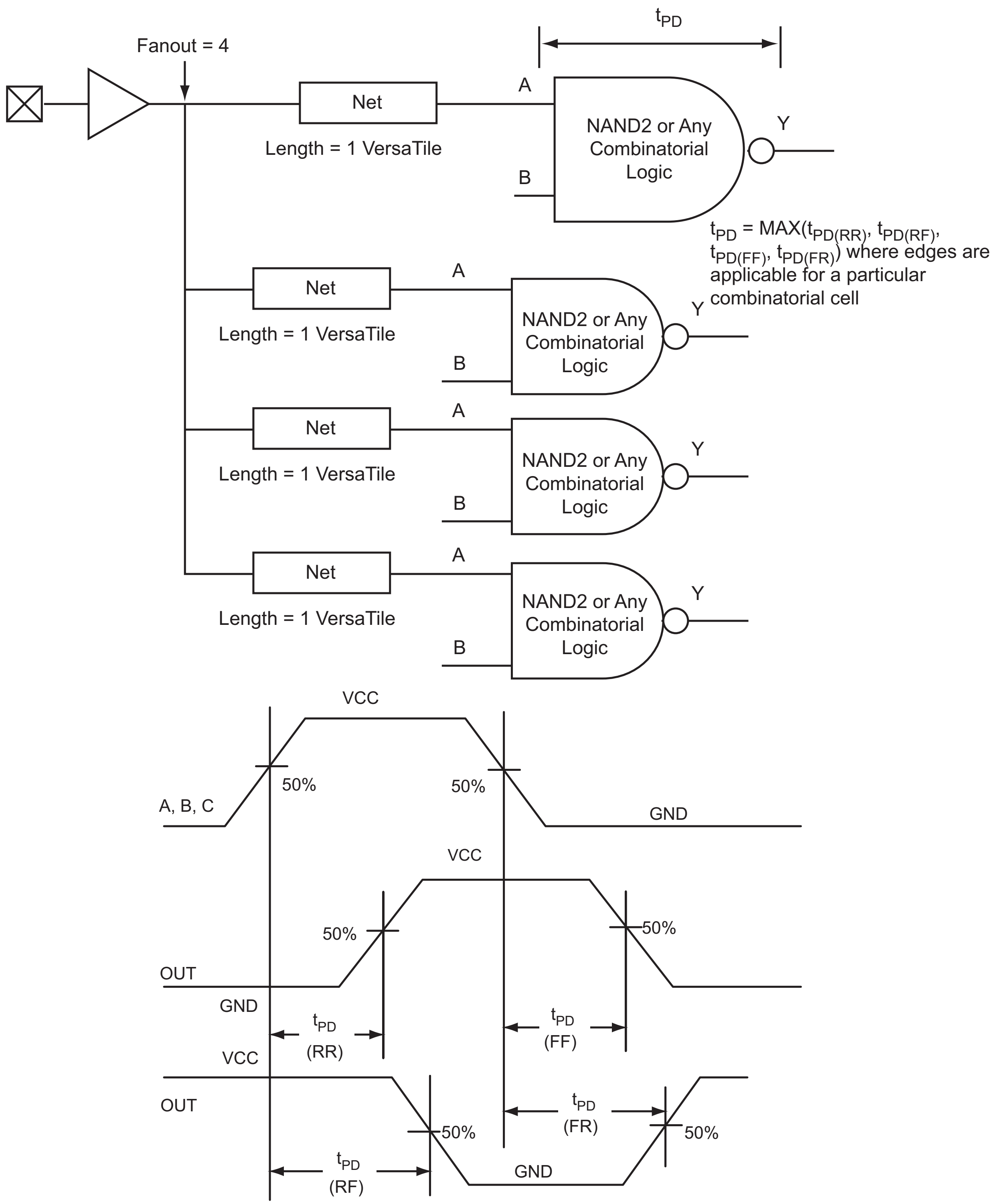

Figure 2-36 **• Timing Model and Waveforms**

Timing Waveforms

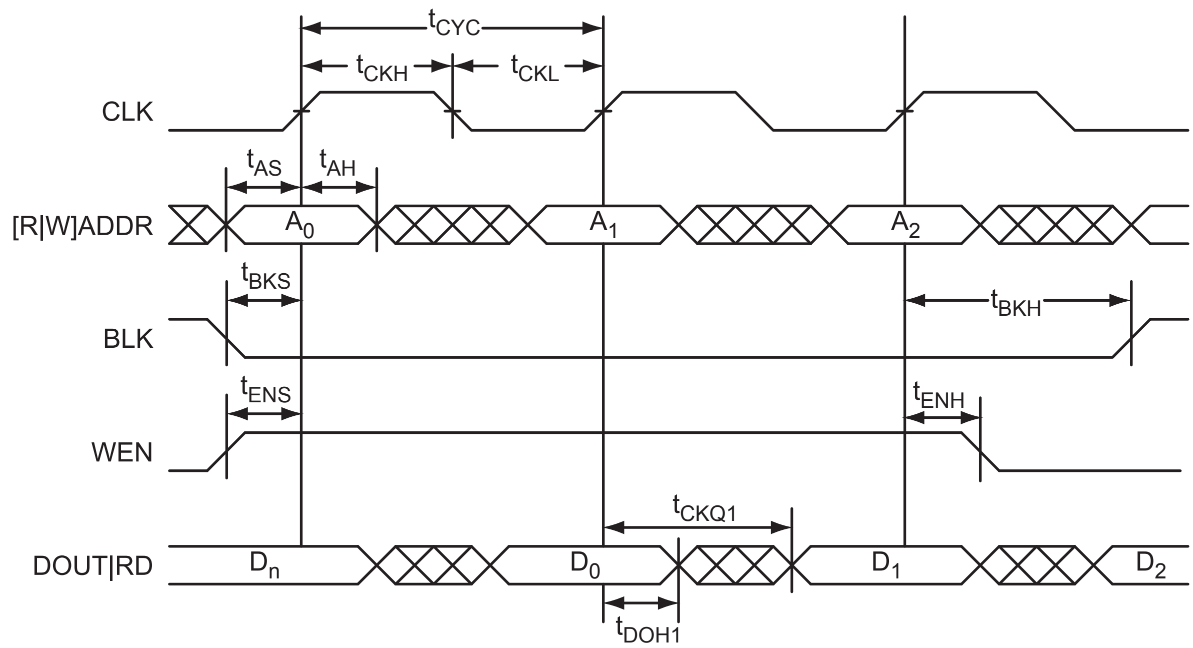

Figure 2-42 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512X18.**

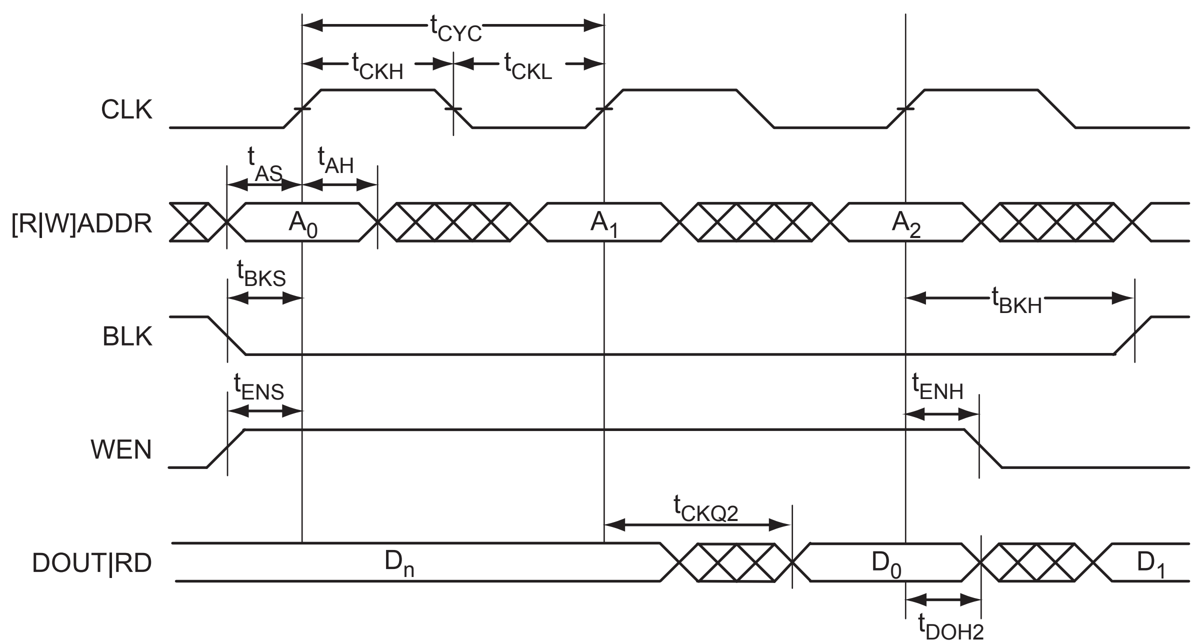

Figure 2-43 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512X18.**

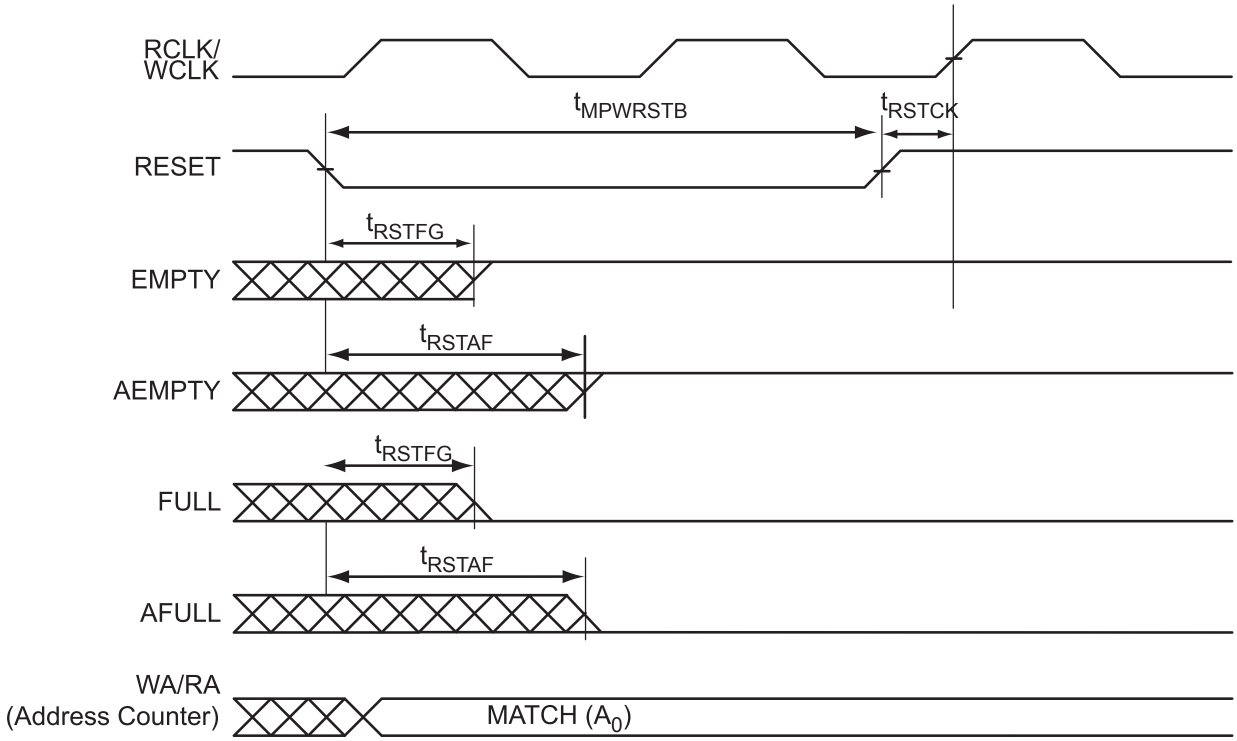

Figure 2-50 • **FIFO Reset**

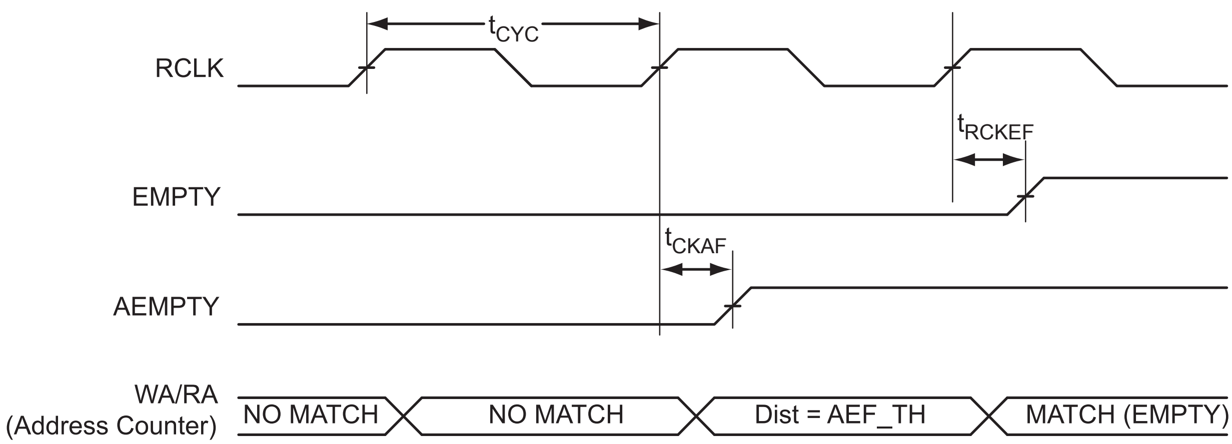

Figure 2-51 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

Table 3-1 shows the Flash*Freeze pin location on the available packages. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOOe FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 **• Flash*Freeze Pin Locations for IGLOOe Devices**

Package	Flash*Freeze Pin
FG256	T3
FG484	W6
FG896	AH4

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 **• Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance [1,2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled-up or pulled-down.*
2. *The TRST pin is pulled-down.*
3. *Equivalent parallel resistance if more than one device is on the JTAG chain*

FG484	
Pin Number	AGLE3000 Function
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2

FG484	
Pin Number	AGLE3000 Function
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1

FG484	
Pin Number	AGLE3000 Function
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOOe datasheet.

Revision	Changes	Page
Revision 13 (December 2012)	The "IGLOOe Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43176). Also added the missing heading 'Supply Voltage' under V2.	III
	The note in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42568).	2-91, 2-92
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40272).	N/A
Revision 11 (August 2012)	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 37180): Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels, Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-28 • I/O Output Buffer Maximum Resistances1 Table 2-73 • Minimum and Maximum DC Input and Output Levels Table 2-77 • Minimum and Maximum DC Input and Output Levels Also added note stating "*Output drive strength is below JEDEC specification.*" for Tables 2-25, 2-26, and 2-28. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-21 (SAR 39713).	 2-20 2-25 2-26 2-28 2-51 2-53
	In Table 2-117 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37183).	2-65
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38318). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 10 (April 2012)	In Table 2-2 • Recommended Operating Conditions 1, VPUMP programming voltage for operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 32256). Values for VCCPLL at 1.2–1.5 V DC core supply voltage were changed from "1.14 to 1.26 V" to "1.14 to 1.575 V" (SAR 34701).	2-2
	The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD. Table 2-8 • Power Supply State per Mode is new (SARs 34745, 36949).	2-7
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37105).	2-17
	"TBD" for 3.3 V LVCMOS Wide Range in Table 2-28 • I/O Output Buffer Maximum Resistances1 and Table 2-30 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33855). Values were also added for 1.2 V LVCMOS and 1.2 V LVCMOS Wide Range.	2-28, 2-30
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34753).	2-29
	IOSH and IOSL values were added to 3.3 V LVCMOS Wide Range Table 2-40 • Minimum and Maximum DC Input and Output Levels, 1.2 V LVCMOS Table 2-64 • Minimum and Maximum DC Input and Output Levels, and 1.2 V LVCMOS Wide Range Table 2-68 • Minimum and Maximum DC Input and Output Levels (SAR 33855).	2-35, 2-47, 2-48
	Figure 2-48 • FIFO Read and Figure 2-49 • FIFO Write have been added (SAR 34844).	2-103
	Values for $F_{DDRIMAX}$ and F_{DDOMAX} were added to the tables in the Input DDR "Timing Characteristics" section and Output DDR "Timing Characteristics" section (SAR 34802).	2-77,2-81
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36952).	2-89
Revision 9 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34665).	I, 1-2
	The Y security option and Licensed DPA Logo were added to the "IGLOOe Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34725).	III
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface" (SAR 34685).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 34696).	1-7
	Values for VCCPLL at 1.5 V DC core supply voltage were changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" in Table 2-2 • Recommended Operating Conditions 1 (SAR 32292).	2-2
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide* (SAR 34731).	2-13

Revision	Changes	Page
Revision 9 (continued)	The example in the paragraph above Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 32287).	2-31
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34766).	2-23, 2-35, 2-48
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34886).	2-32
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34793): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-38
	Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34818).	2-91, 2-92
	The following figures were deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34869). Figure 2-46 • Write Access after Write onto Same Address Figure 2-47 • Read Access after Write onto Same Address Figure 2-48 • Write Access after Read onto Same Address The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-50 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35749).	2-95, 2-98, 2-104, 2-106
	The "Pin Descriptions and Packaging" chapter is new (SAR 34768).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34768)	4-1
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOOe Device Status" table on page II indicates the status for each device in the device family.	N/A

Revision	Changes	Page
Revision 3 (cont'd)	Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 was updated to change PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. Table note 4 is new.	2-10
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power.	2-11, 2-12
	A table subtitle was added for Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices.	2-12
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P_{STAT}, including PDC6 and PDC7.	2-13
	Footnote 1 was updated to include information about P_{AC13}. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14}$ * FCLKOUT to PPLL = $P_{DC4} + P_{AC13}$ * F_{CLKOUT}.	2-14
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-16
	In Table 2-22 • Summary of Maximum and Minimum DC Input Levels, T_J was changed to T_A in notes 1 and 2.	2-22
	Table 2-22 • Summary of Maximum and Minimum DC Input Levels was updated to included a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode).	2-22
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-47
Revision 2 (Jun 2008) Product Brief v1.0	The product brief section of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
Revision 2 (cont'd) Packaging v1.1	The naming conventions changed for the following pins in the "FG484" for the A3GLE600: Pin Number — New Function Name J19 — IO45PPB2V1 K20 — IO45NPB2V1 M2 — IO114NPB6V1 N1 — IO114PPB6V1 N4 — GFC2/IO115PPB6V1 P3 — IO115NPB6V1	4-6
Revision 1 (Mar 2008) Product Brief rev. 1	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 µW)" was removed from "Low Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" section sections.	I I, 1-7
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0.	N/A

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