Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	270
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agle600v5-fgg484i

SRAM and FIFO

IGLOOe devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOOe devices provide designers with very flexible clock conditioning capabilities. Each member of the IGLOOe family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

IGLOOe devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient Temperature		0 to +70	–40 to +85	°C
T_J	Junction Temperature[2]		0 to + 85	–40 to +100	°C
VCC [3]	1.5 V DC core supply voltage[4]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core voltage[5, 6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage[6]	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[4]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V DC core supply voltage[5]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV[9]	1.2 V DC supply voltage[5]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V wide range DC supply voltage[5]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage[10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-20. VCCI should be at the same voltage within a given I/O bank.*
4. *For IGLOOe V5 devices*
5. *For IGLOOe V2 devices only, operating at VCCI ≥ VCC*
6. *All IGLOOe devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "VCCPLA/B/C/D/E/F PLL Supply Voltage" section for further information.*
9. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section for further information.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1, 3]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

Power per I/O Pin

Table 2-13 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range [3]	3.3	–	16.34
3.3 V LVCMOS Wide Range – Schmitt trigger [3]	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS [4]	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger [4]	1.2	–	0.53
1.2 V LVCMOS Wide Range [4]	1.2	–	0.60
1.2 V LVCMOS Wide Range – Schmitt trigger [4]	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	.079
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*
4. *Applicable for IGLOOe V2 devices only.*

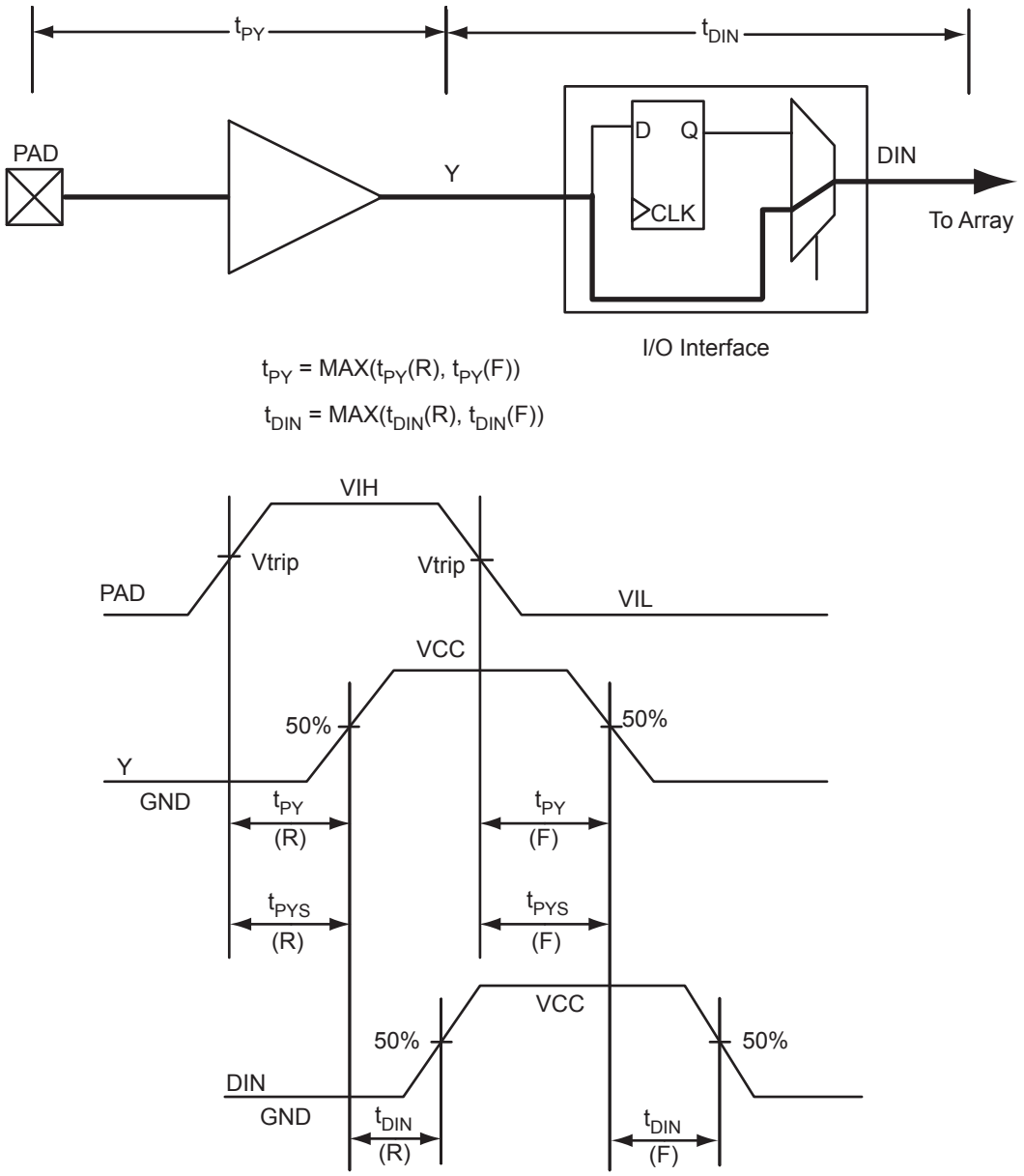

Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels (continued) Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
HSTL (II)	15 mA[5]	15 mA[5]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
5. *Output drive strength is below JEDEC specification.*
6. *Output Slew Rates can be extracted from IBIS Models, http://www.microsemi.com/soc/download/ibis/default.aspx.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

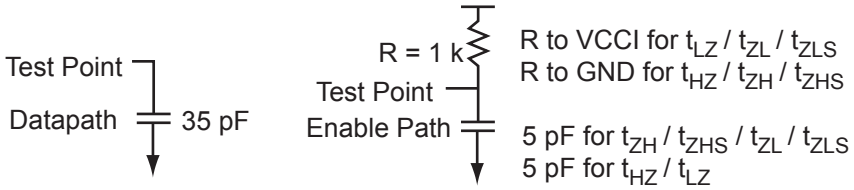

Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-73 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
20 mA[5]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	268	181	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

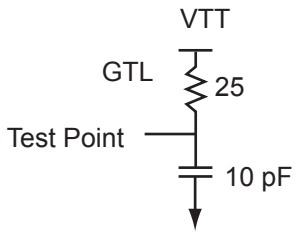

Figure 2-13 • AC Loading

Table 2-74 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-85 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

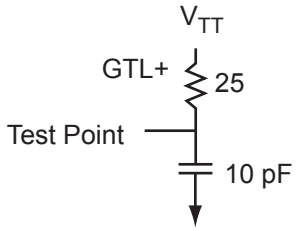

Figure 2-16 • AC Loading

Table 2-86 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-87 • 2.5 V GTL+ – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.97	0.19	1.29	0.67	2.00	1.84			5.63	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-88 • 2.5 V GTL+ – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.23	0.26	1.55	1.10	2.28	2.11			8.08	7.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	32	39	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

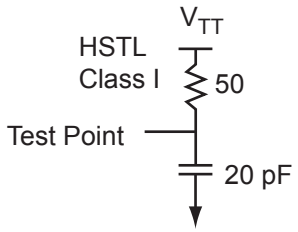

Figure 2-17 • AC Loading

Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-91 • HSTL Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.74	0.19	1.77	0.67	2.79	2.73			6.42	6.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	3.10	0.26	1.94	1.10	3.12	3.10			8.93	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-101 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

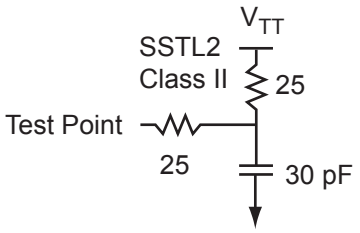

Figure 2-20 • AC Loading

Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.94	0.19	1.15	0.67	1.97	1.66			5.60	5.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.20	0.26	1.39	1.10	2.24	1.97			8.05	7.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-105 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
14 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14	51	54	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

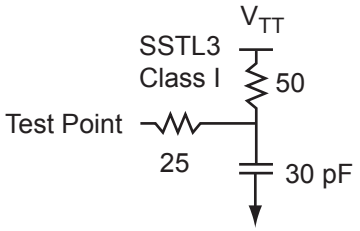

Figure 2-21 • AC Loading

Table 2-106 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-107 • SSTL 3 Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.05	0.19	1.09	0.67	2.09	1.71			5.72	5.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-108 • SSTL 3 Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.32	0.26	1.32	1.10	2.37	2.02			8.17	7.83	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-131 • Input DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

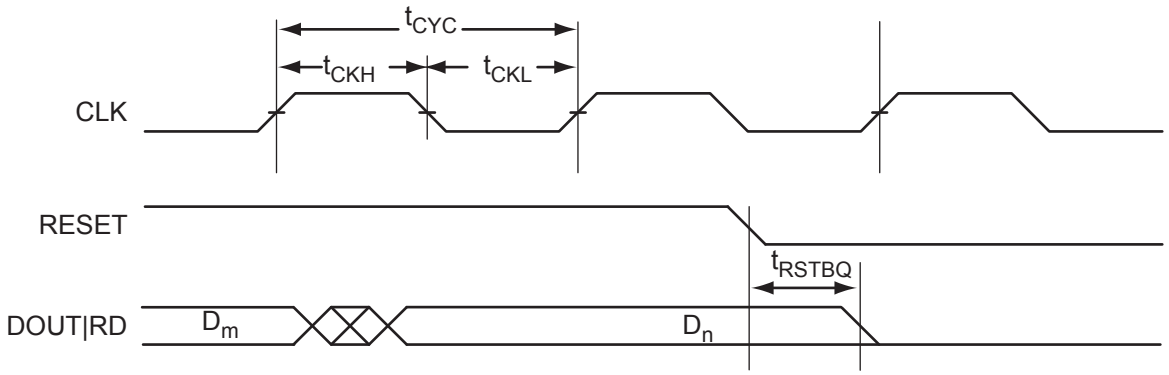

Figure 2-46 • **RAM Reset**

Table 2-146 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	0.83	ns
t_{AH}	Address Hold Time	0.16	ns
t_{ENS}	REN, WEN Setup Time	0.73	ns
t_{ENH}	REN, WEN Hold Time	0.08	ns
t_{DS}	Input Data (WD) Setup Time	0.71	ns
t_{DH}	Input Data (WD) Hold Time	0.36	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (output retained, WMODE = 0)	4.21	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.71	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.42	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	2.06	ns
	RESET Low to Data Out Low on RD (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET Removal	0.61	ns
$t_{RECRSTB}$	RESET Recovery	3.21	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

FG256	
Pin Number	AGLE600 Function
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	VCOMPLF
H5	GFC0/IO120NPB7V0
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	VCOMPLC
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	VCCPLF
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	VCCPLC
J16	GCA2/IO53PSB3V0

FG256	
Pin Number	AGLE600 Function
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1
K5	VCCIB6
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB3
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	VCCIB6
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB3
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0
M4	GEC0/IO104NPB6V0

FG256	
Pin Number	AGLE600 Function
M5	VMV5
M6	VCCIB5
M7	VCCIB5
M8	IO84NDB5V0
M9	IO84PDB5V0
M10	VCCIB4
M11	VCCIB4
M12	VMV3
M13	VCCPLD
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	VCOMPLE
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	VCOMPLD
N14	VJTAG
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	VCCPLE
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1
P8	IO90PDB5V1

FG484	
Pin Number	AGLE600 Function
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO54NPB3V0
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC

FG484	
Pin Number	AGLE600 Function
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1

FG484	
Pin Number	AGLE600 Function
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC

FG896	
Pin Number	AGLE3000 Function
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC
AG3	IO232NPB5V4
AG4	GND
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC

FG896	
Pin Number	AGLE3000 Function
AH4	FF/GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2

FG896	
Pin Number	AGLE3000 Function
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4