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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1agle3000v2-fg896i

I/Os Per Package [1]

IGLOOe Devices	AGLE600		AGLE3000	
ARM-Enabled IGLOOe Devices			M1AGLE3000	
	I/O Types			
Package	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs
FG256	165	79	–	–
FG484	270	135	341	168
FG896	–	–	620	310

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the IGLOOe FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *For AGLE3000 devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
4. *FG256 and FG484 are footprint-compatible packages.*
5. *When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).*
6. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
7. *"G" indicates RoHS-compliant packages. Refer to "IGLOOe Ordering Information" on page III for the location of the "G" in the part number.*

IGLOOe FPGAs Package Sizes Dimensions

Package	FG256	FG484	FG896
Length × Width (mm × mm)	17 × 17	23 × 23	31 × 31
Nominal Area (mm2)	289	529	961
Pitch (mm)	1	1	1
Height (mm)	1.6	2.23	2.23

IGLOOe Device Status

IGLOOe Devices	Status	M1 IGLOOe Devices	Status
AGLE600	Production		
AGLE3000	Production	M1AGLE3000	Production

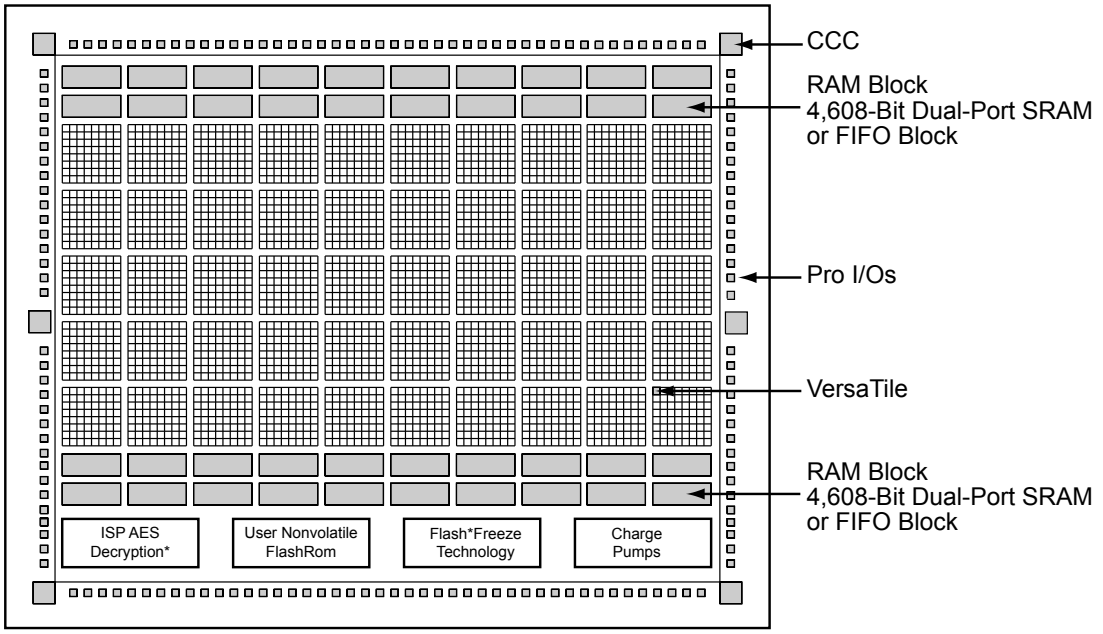

Figure 1-1 • **IGLOOe Device Architecture Overview**

*Flash*Freeze Technology*

The IGLOOe device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static and dynamic capabilities of the IGLOOe device. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode.

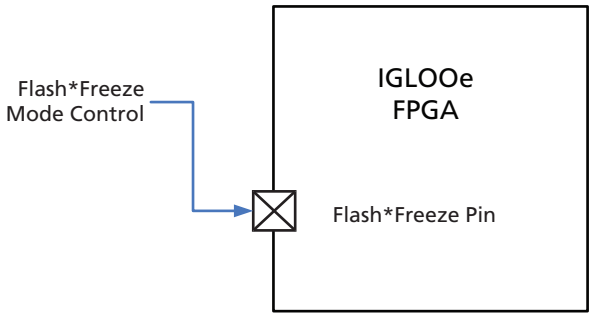

Figure 1-2 • **IGLOOe Flash*Freeze Mode**

Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1]

	Core Voltage	AGLE600	AGLE3000	Units
ICCA Current[2]				
Typical (25°C)	1.2 V	28	89	µA
	1.5 V	82	320	µA
ICCI or IJTAG Current[3]				
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI/VJTAG= 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

Notes:

1. *IDD = N_{BANKS} × ICCI + ICCA. JTAG counts as one bank when powered.*
2. *Includes VCC and VPUMP and VCCPLL currents.*
3. *Values do not include I/O static contribution (PDC6 and PDC7).*

Power per I/O Pin

Table 2-13 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range [3]	3.3	–	16.34
3.3 V LVCMOS Wide Range – Schmitt trigger [3]	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS [4]	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger [4]	1.2	–	0.53
1.2 V LVCMOS Wide Range [4]	1.2	–	0.60
1.2 V LVCMOS Wide Range – Schmitt trigger [4]	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	.079
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*
4. *Applicable for IGLOOe V2 devices only.*

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-15.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-20 on page 2-15.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-20 on page 2-15.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-20 on page 2-15.

PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Table 2-24 • I/O AC Parameter Definitions

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

1.2 V DC Core Voltage

Table 2-44 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	1.55	8.14	0.26	1.66	2.14	1.10	8.14	6.46	3.80	3.79	13.93	12.25	ns
100 µA	8 mA	Std.	1.55	6.68	0.26	1.66	2.14	1.10	6.68	5.57	4.25	4.69	12.47	11.36	ns
100 µA	12 mA	Std.	1.55	5.65	0.26	1.66	2.14	1.10	5.65	4.91	4.55	5.25	11.44	10.69	ns
100 µA	16 mA	Std.	1.55	5.36	0.26	1.66	2.14	1.10	5.36	4.76	4.61	5.41	11.14	10.55	ns
100 µA	24 mA	Std.	1.55	5.20	0.26	1.66	2.14	1.10	5.20	4.78	4.69	6.00	10.99	10.56	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-45 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	1.55	4.65	0.26	1.66	2.14	110	4.65	3.64	3.80	4.00	10.44	9.43	ns
100 µA	8 mA	Std.	1.55	3.85	0.26	1.66	2.14	1.10	3.85	2.99	4.25	4.91	9.64	8.77	ns
100 µA	12 mA	Std.	1.55	3.40	0.26	1.66	2.14	1.10	3.40	2.68	4.55	5.49	9.19	8.46	ns
100 µA	16 mA	Std.	1.55	3.33	0.26	1.66	2.14	1.10	3.33	2.62	4.62	5.65	9.11	8.41	ns
100 µA	24 mA	Std.	1.55	3.36	0.26	1.66	2.14	1.10	3.36	2.54	4.71	6.24	9.15	8.32	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V

Table 2-81 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	268	181	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

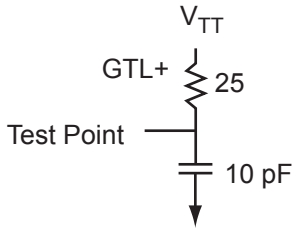

Figure 2-15 • AC Loading

Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

**Table 2-83 • 3.3 V GTL+ – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 1.0 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.85	0.19	1.35	0.67	1.88	1.81			5.51	5.44	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

**Table 2-84 • 3.3 V GTL+ – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 1.0 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.11	0.26	1.61	1.10	2.15	2.07			7.95	7.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-93 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA[5]	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	66	55	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

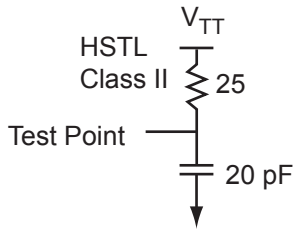

Figure 2-18 • AC Loading

Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

**Table 2-95 • HSTL Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.62	0.19	1.77	0.67	2.66	2.40			6.29	6.03	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

**Table 2-96 • HSTL Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.93	0.26	1.94	1.10	2.98	2.75			8.79	8.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

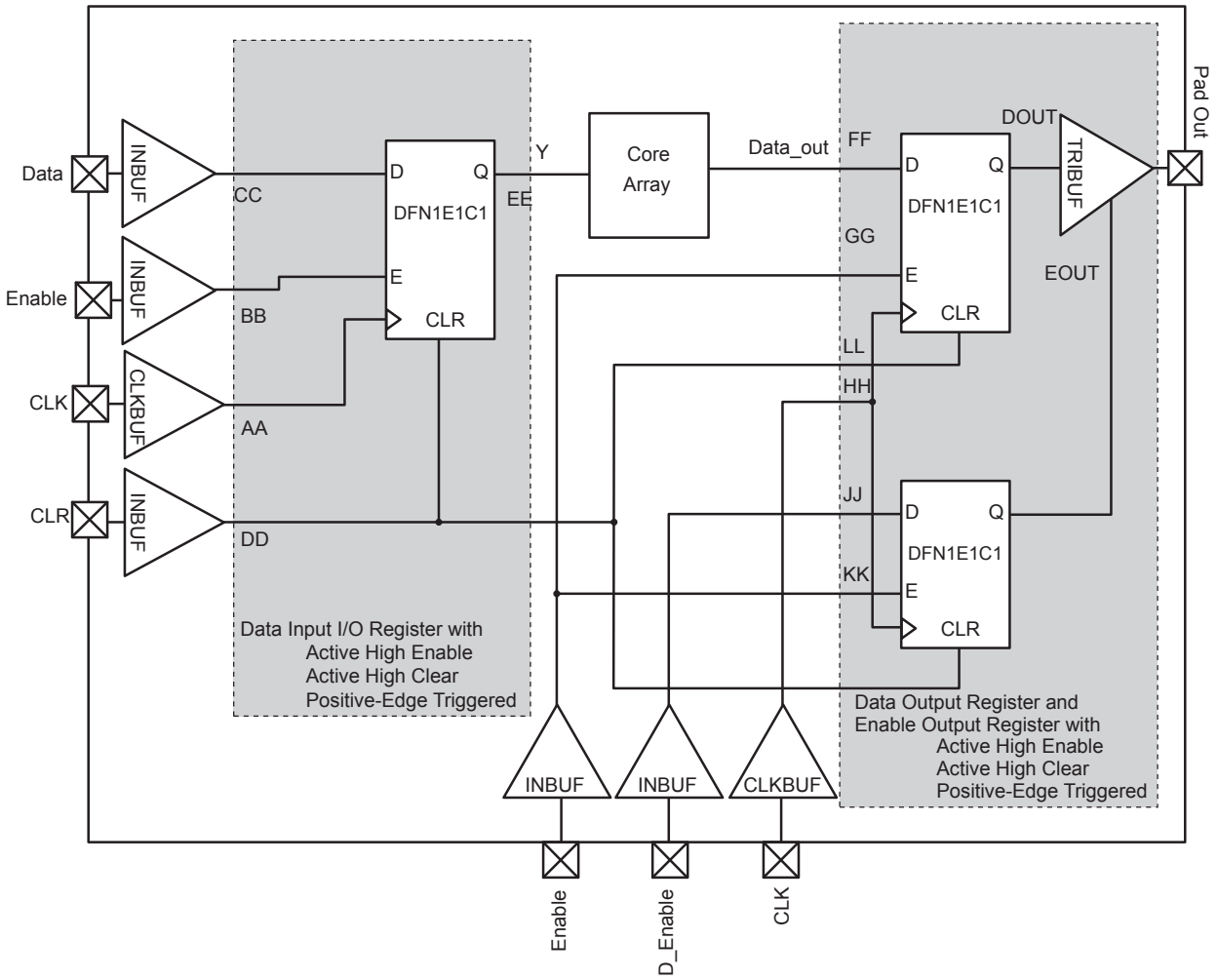

Figure 2-27 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Output Register

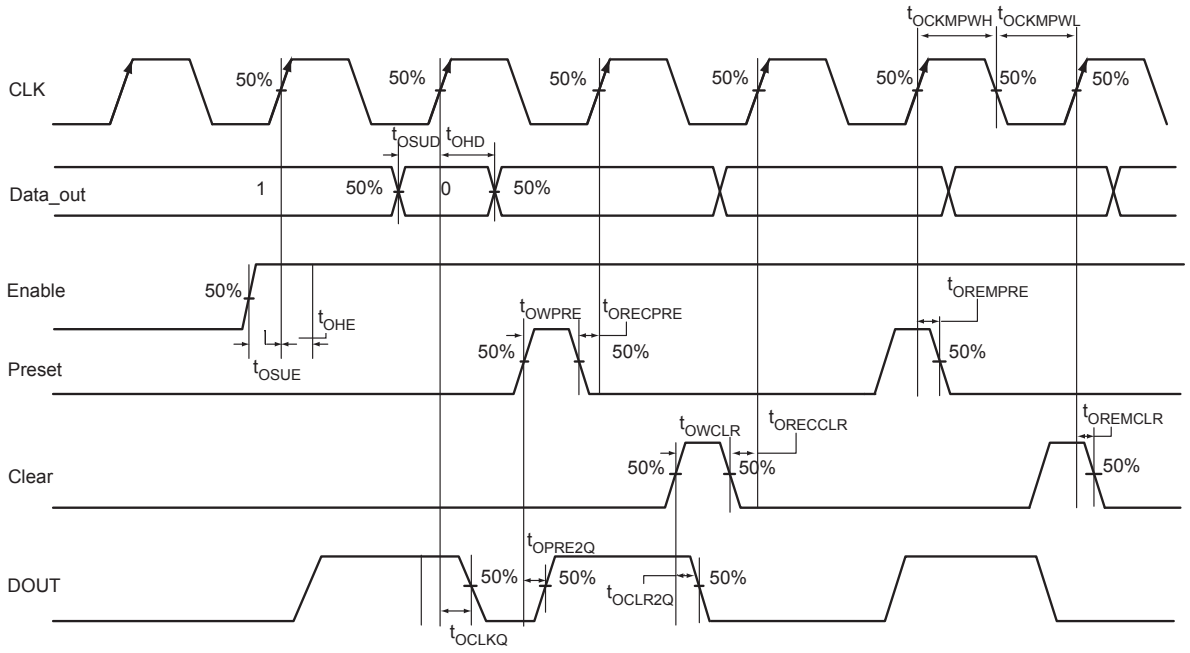

Figure 2-29 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-125 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-128 • Output Enable Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Output DDR Module

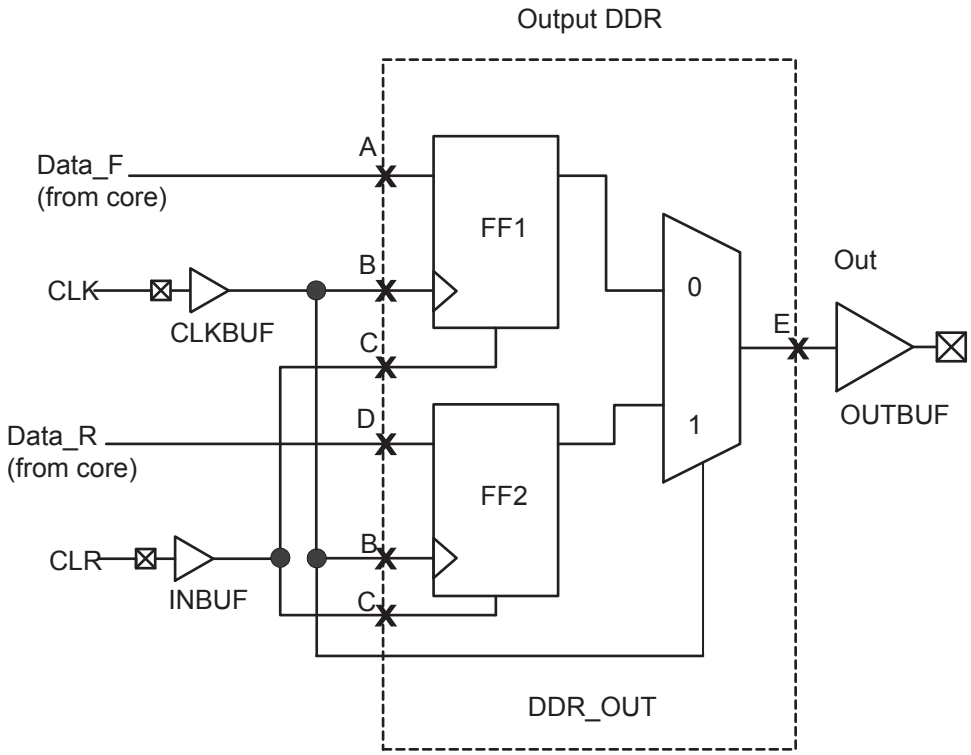

Figure 2-33 • **Output DDR Timing Model**

Table 2-132 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Timing Characteristics

1.5 V DC Core Voltage

Table 2-135 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y = !(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	Y = A ⊕ B	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.33	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-136 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.35	ns
AND2	Y = A · B	t_{PD}	1.42	ns
NAND2	Y = !(A · B)	t_{PD}	1.58	ns
OR2	Y = A + B	t_{PD}	2.10	ns
NOR2	Y = !(A + B)	t_{PD}	1.94	ns
XOR2	Y = A ⊕ B	t_{PD}	2.33	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.34	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.05	ns
MUX2	Y = A !S + B S	t_{PD}	2.64	ns
AND3	Y = A · B · C	t_{PD}	2.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

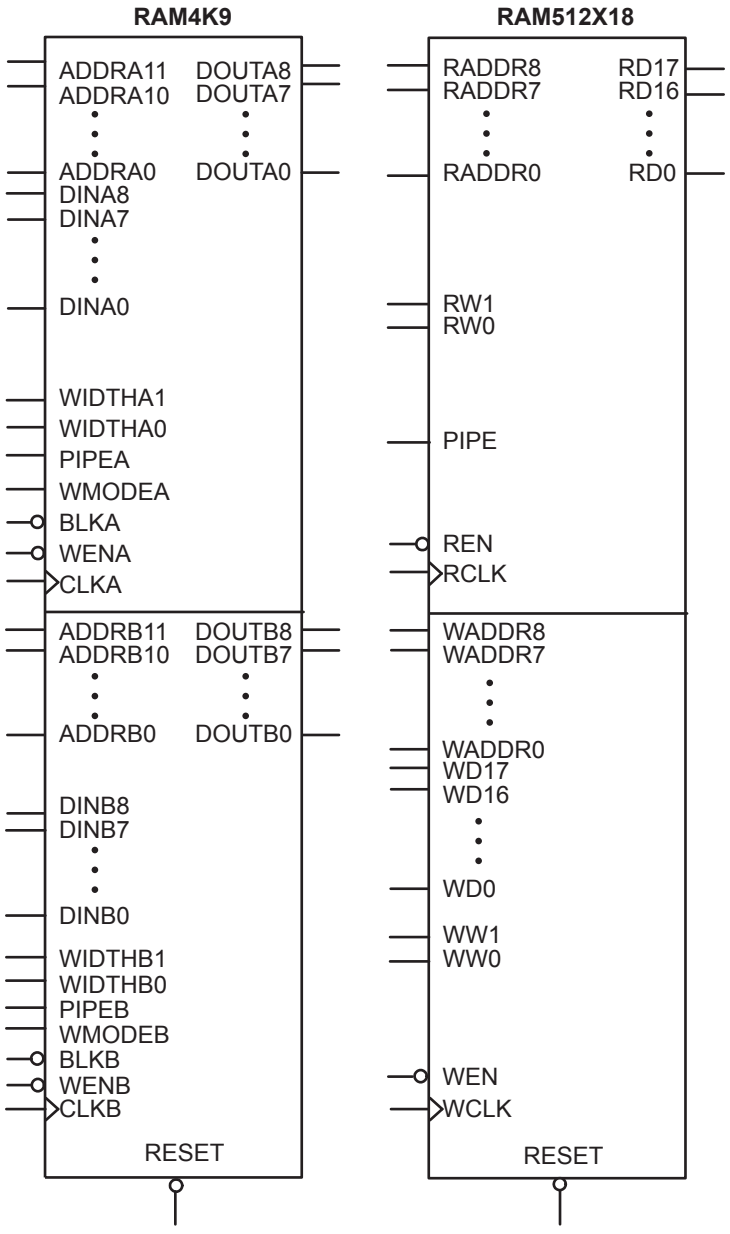

Figure 2-41 • **RAM Models**

Applies to 1.2 V DC Core Voltage

Table 2-147 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	1.53	ns
t_{AH}	Address Hold Time	0.29	ns
t_{ENS}	REN, WEN Setup Time	1.50	ns
t_{ENH}	REN, WEN Hold Time	0.29	ns
t_{BKS}	BLK Setup Time	3.05	ns
t_{BKH}	BLK Hold Time	0.29	ns
t_{DS}	Input Data (DIN) Setup Time	1.33	ns
t_{DH}	Input Data (DIN) Hold Time	0.66	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.01	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (pass-through)	3.86	ns
	RESET Low to Data Out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET Removal	1.12	ns
$t_{RECRSTB}$	RESET Recovery	5.93	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

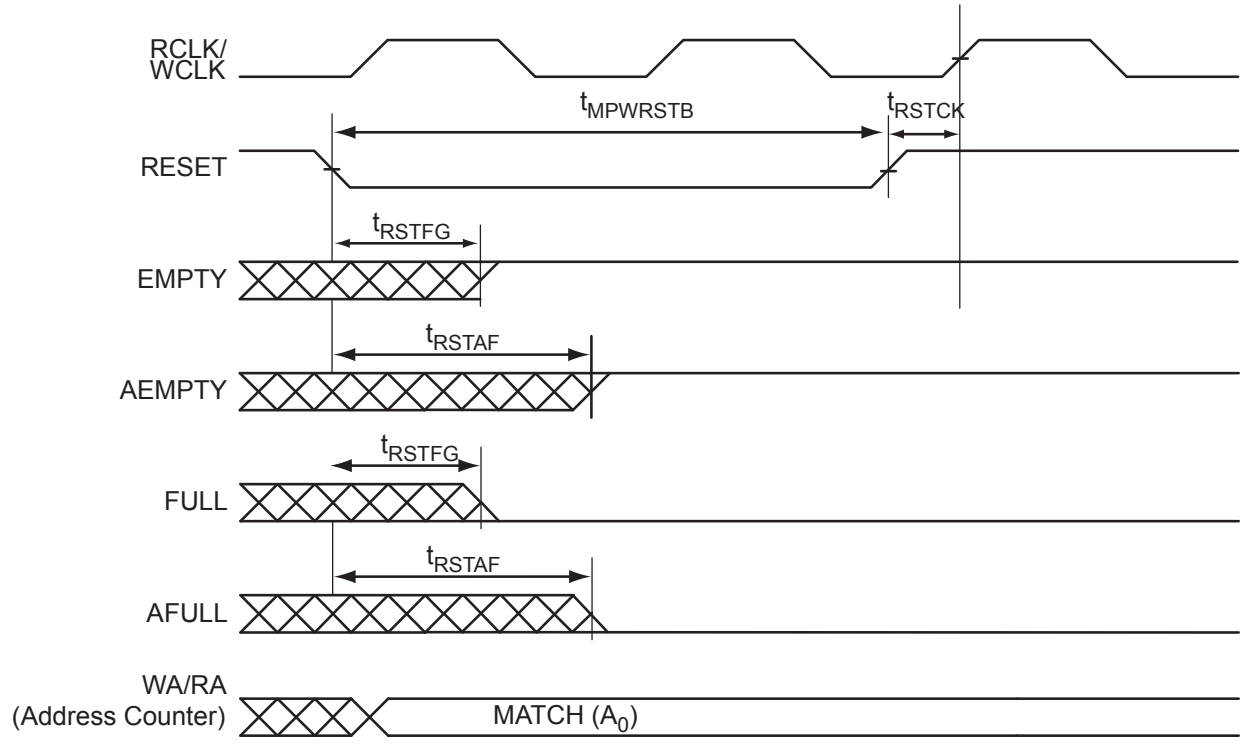

Figure 2-50 • **FIFO Reset**

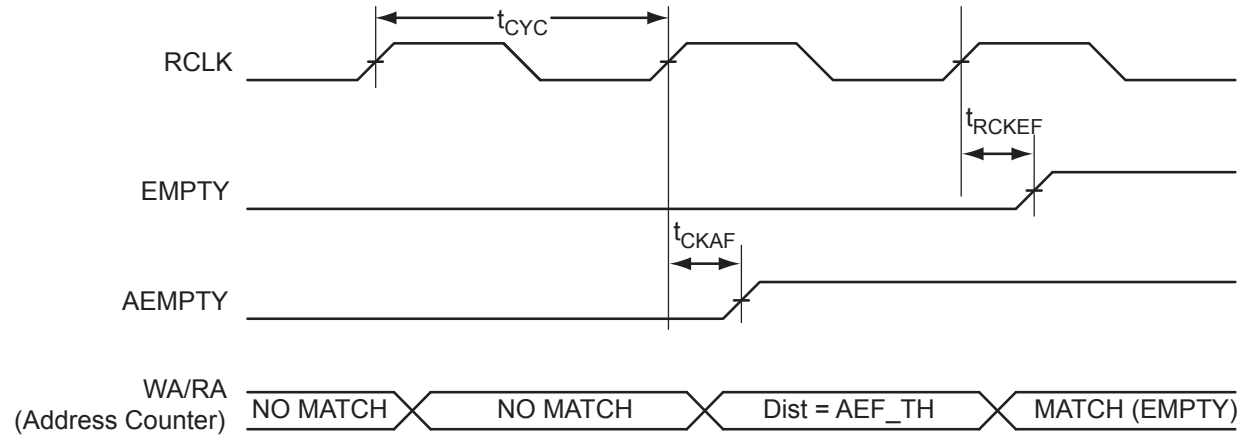

Figure 2-51 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

FG896	
Pin Number	AGLE3000 Function
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	VCCIB7
E4	IO305PPB7V3
E5	VCC
E6	GAC0/IO02NDB0V0
E7	VCCIB0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2

FG896	
Pin Number	AGLE3000 Function
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G6	GNDQ

FG896	
Pin Number	AGLE3000 Function
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOOe datasheet.

Revision	Changes	Page
Revision 13 (December 2012)	The "IGLOOe Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43176). Also added the missing heading 'Supply Voltage' under V2.	III
	The note in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42568).	2-91, 2-92
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40272).	N/A
Revision 11 (August 2012)	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 37180): Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels, Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-28 • I/O Output Buffer Maximum Resistances1 Table 2-73 • Minimum and Maximum DC Input and Output Levels Table 2-77 • Minimum and Maximum DC Input and Output Levels Also added note stating "*Output drive strength is below JEDEC specification.*" for Tables 2-25, 2-26, and 2-28. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-21 (SAR 39713).	2-20 2-25 2-26 2-28 2-51 2-53
	In Table 2-117 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37183).	2-65
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38318). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 8 (Nov 2009)	The version changed to v2.0 for IGLOOe datasheet chapters, indicating the datasheet contains information based on final characterization.	N/A
Product Brief v2.0	The "Pro (Professional) I/O" section was revised to add "Hot-swappable and cold-sparing I/Os."	I
	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	Definitions of hot-swap and cold-sparing were added to the "Pro I/Os with Advanced I/O Standards" section.	1-7
DC and Switching Characteristics v2.0	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	Values for 1.2 V wide range DC core supply voltage were added to Table 2-2 • Recommended Operating Conditions 1. Table notes regarding 3.3 V wide range and the core voltage required for programming were added to the table.	2-2
	The data in Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (1.5 V DC core supply voltage) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (1.2 V DC core supply voltage) was revised.	2-6
	3.3 V LVCMOS wide range data was included in Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1. Table notes were added in connection with this data.	2-9, 2-10
	The temperature was revised from 110ºC to 100ºC in Table 2-31 • Duration of Short Circuit Event before Failure and Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*.	2-31, 2-31
	The tables in the "Overview of I/O Performance" section and "Detailed I/O DC Characteristics" sectionwere revised to include 3.3 V LVCMOS and 1.2 V LVCMOS wide range.	2-20, 2-28
	Most tables were updated in the following sections, revising existing values and adding information for 3.3 V and 1.2 V wide range: "Single-Ended I/O Characteristics" "Voltage-Referenced I/O Characteristics" "Differential I/O Characteristics"	2-32, 2-51, 2-62
	The value for "Delay range in block: fixed delay" was revised in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification.	2-91, 2-92
	The timing characteristics tables for RAM4K9 and RAM512X18 were updated, including renaming of the address collision parameters.	2-98 – 2-101
Revision 7 (Apr 2009) Product Brief v1.4 DC and Switching Characteristics Advance v0.4	The –F speed grade is no longer offered for IGLOOe devices and was removed from the documentation. The speed grade column and note regarding –F speed grade were removed from "IGLOOe Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV