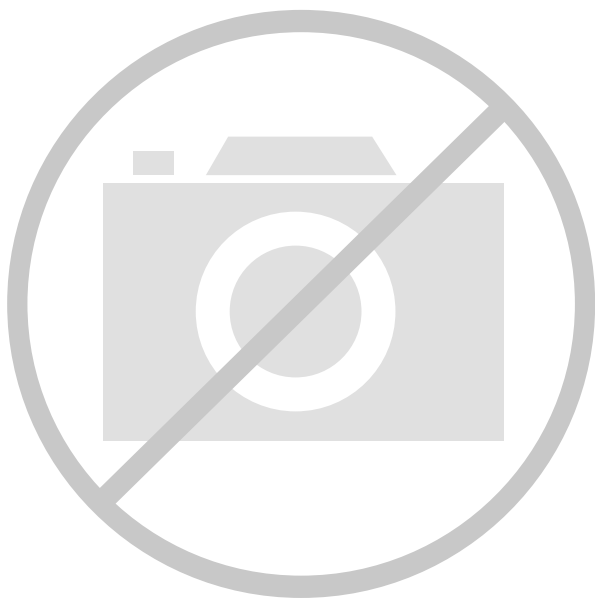




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1agle3000v5-fg896

Table 2-2 • Recommended Operating Conditions ¹

Symbol	Parameter		Commercial	Industrial	Units
T _A	Ambient Temperature		0 to +70	–40 to +85	°C
T _J	Junction Temperature ²		0 to + 85	–40 to +100	°C
VCC ³	1.5 V DC core supply voltage ⁴		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core voltage ^{5, 6}		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage ⁶	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁷	0 to 3.6	0 to 3.6	V
VCCPLL ⁸	Analog power supply (PLL)	1.5 V DC core supply voltage ⁴	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V DC core supply voltage ⁵	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV ⁹	1.2 V DC supply voltage ⁵		1.14 to 1.26	1.14 to 1.26	V
	1.2 V wide range DC supply voltage ⁵		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage ¹⁰		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.
3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-21 on page 2-20](#). VCCI should be at the same voltage within a given I/O bank.
4. For IGLOOe V5 devices
5. For IGLOOe V2 devices only, operating at VCCI ≥ VCC
6. All IGLOOe devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.
7. VPUMP can be left floating during operation (not programming mode).
8. VCCPLL pins should be tied to VCC pins. See the "[VCCPLA/B/C/D/E/F PLL Supply Voltage](#)" section for further information.
9. VMV pins must be connected to the corresponding VCCI pins. See the "[VMVx I/O Supply Voltage \(quiet\)](#)" section for further information.
10. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOOe FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

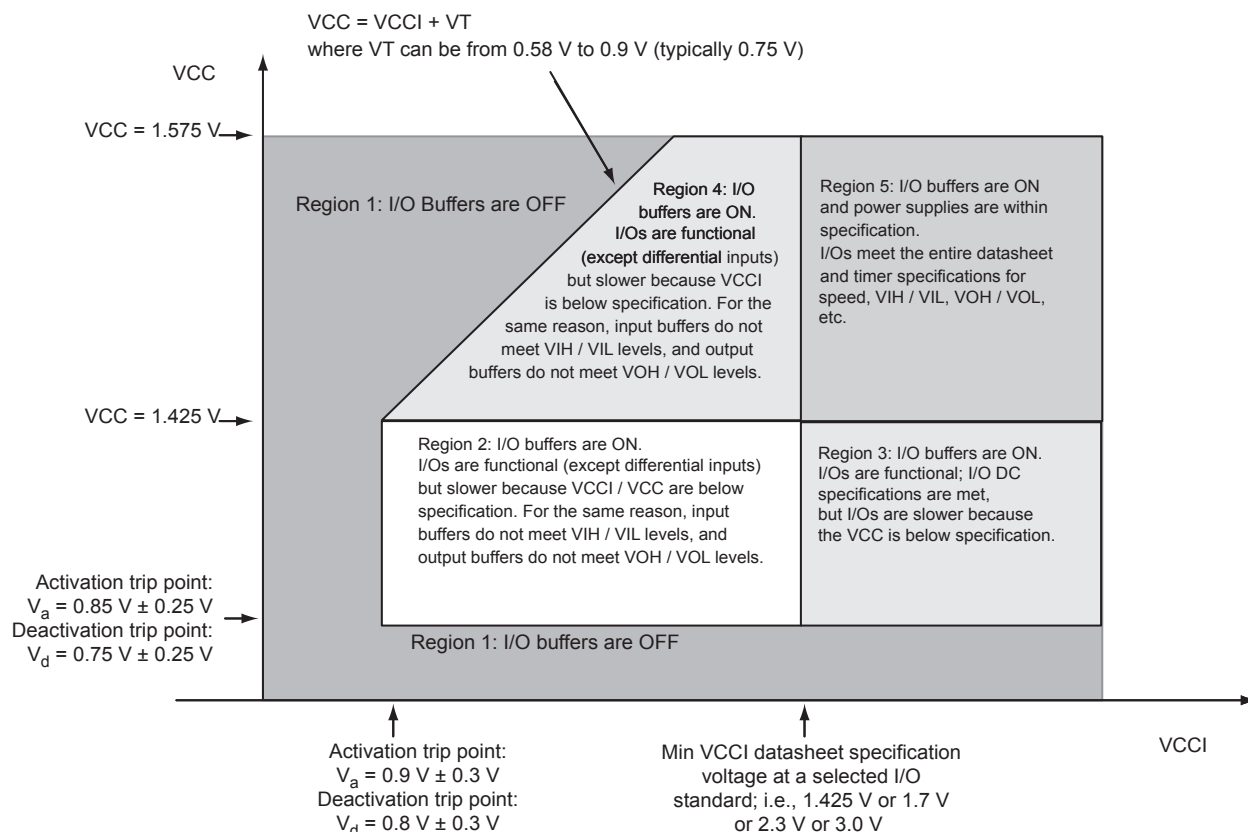


Figure 2-1 • V5 – I/O State as a Function of VCCI and VCC Voltage Levels

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range ³	3.3	–	16.34
3.3 V LVCMOS Wide Range – Schmitt trigger ³	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS ⁴	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger ⁴	1.2	–	0.53
1.2 V LVCMOS Wide Range ⁴	1.2	–	0.60
1.2 V LVCMOS Wide Range – Schmitt trigger ⁴	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	.079
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. PDC6 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.
4. Applicable for IGLOOe V2 devices only.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	–	–	1.4 V
3.3 V LVCMOS Wide Range	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
1.2 V LVCMOS*	–	–	0.6 V
1.2 V LVCMOS – Wide Range*	–	–	0.6 V
3.3 V PCI	–	–	0.285 * VCCI (RR)
	–	–	0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR)
	–	–	0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Note: *Applicable to V2 devices ONLY operating in the 1.2 V core range.

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings (continued)
Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case V_{CCI} (per standard)

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{POUT} (ns)	t_{PP} (ns)	t_{PIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
LVDS	24	–	High	–	–	1.55	2.26	0.25	1.95	–	–	–	–	–	–	–	–	ns
LVPECL	24	–	High	–	–	1.55	2.17	0.25	1.70	–	–	–	–	–	–	–	–	ns

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-49](#) for connectivity. This resistor is not required during normal operation.
5. Output drive strength is below JEDEC specification.
6. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Detailed I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances¹

Standard	Drive Strength	$R_{PULL-DOWN} (\Omega)^2$	$R_{PULL-UP} (\Omega)^3$
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 μA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS ⁴	2 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Applicable to IGLOOe V2 devices operating in the 1.2 V core range ONLY.
5. Output drive strength is below JEDEC specification.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

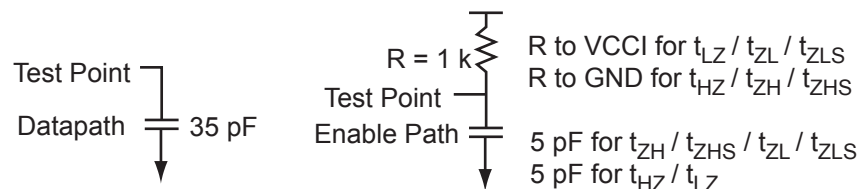


Figure 2-7 • AC Loading

Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	–	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-36 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	4.90	0.18	1.08	1.34	0.66	5.00	3.99	2.27	2.16	8.60	7.59	ns
8 mA	Std.	0.97	4.05	0.18	1.08	1.34	0.66	4.13	3.45	2.53	2.65	7.73	7.05	ns
12 mA	Std.	0.97	3.44	0.18	1.08	1.34	0.66	3.51	3.05	2.71	2.95	7.11	6.64	ns
16 mA	Std.	0.97	3.27	0.18	1.08	1.34	0.66	3.34	2.96	2.74	3.04	6.93	6.55	ns
24 mA	Std.	0.97	3.18	0.18	1.08	1.34	0.66	3.24	2.97	2.79	3.36	6.84	6.56	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-37 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.85	0.18	1.08	1.34	0.66	2.92	2.27	2.27	2.27	6.51	5.87	ns
8 mA	Std.	0.97	2.39	0.18	1.08	1.34	0.66	2.44	1.88	2.53	2.76	6.03	5.47	ns
12 mA	Std.	0.97	2.12	0.18	1.08	1.34	0.66	2.17	1.69	2.71	3.08	5.76	5.28	ns
16 mA	Std.	0.97	2.08	0.18	1.08	1.34	0.66	2.12	1.65	2.75	3.17	5.72	5.25	ns
24 mA	Std.	0.97	2.10	0.18	1.08	1.34	0.66	2.14	1.60	2.80	3.49	5.74	5.20	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-69 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min., V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Per PCI specification	Per PCI curves										10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in [Figure 2-12](#).

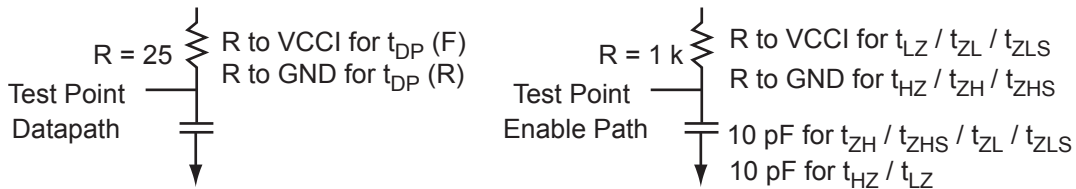


Figure 2-12 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in [Table 2-70](#).

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	0.285 * VCCI for t _{DP(R)} 0.615 * VCCI for t _{DP(F)}	–	10

Note: *Measuring point = V_{trip}. See [Table 2-23 on page 2-23](#) for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-75 • 3.3 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.83	0.19	2.41	0.67	1.84	1.83			5.47	5.46	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-76 • 3.3 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.09	0.26	2.75	1.10	2.10	2.09			7.91	7.89	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
8 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	32	39	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

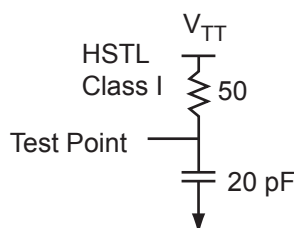


Figure 2-17 • AC Loading

Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = V_{trip}. See [Table 2-23 on page 2-23](#) for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-91 • HSTL Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.98	2.74	0.19	1.77	0.67	2.79	2.73			6.42	6.36	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	1.55	3.10	0.26	1.94	1.10	3.12	3.10			8.93	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-105 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
14 mA	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.7	VCCI - 1.1	14	14	51	54	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

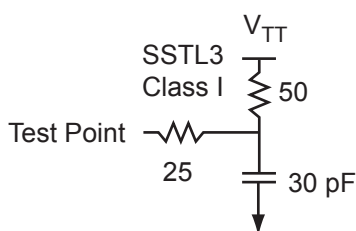


Figure 2-21 • AC Loading

Table 2-106 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip} . See [Table 2-23 on page 2-23](#) for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-107 • SSTL 3 Class I – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.98	2.05	0.19	1.09	0.67	2.09	1.71			5.72	5.34	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-108 • SSTL 3 Class I – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	1.55	2.32	0.26	1.32	1.10	2.37	2.02			8.17	7.83	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-126 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	1.11	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-147 • RAM4K9

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	1.53	ns
t_{AH}	Address Hold Time	0.29	ns
t_{ENS}	REN, WEN Setup Time	1.50	ns
t_{ENH}	REN, WEN Hold Time	0.29	ns
t_{BKS}	BLK Setup Time	3.05	ns
t_{BKH}	BLK Hold Time	0.29	ns
t_{DS}	Input Data (DIN) Setup Time	1.33	ns
t_{DH}	Input Data (DIN) Hold Time	0.66	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.30	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.89	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.01	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (pass-through)	3.86	ns
	RESET Low to Data Out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET Removal	1.12	ns
$t_{RECRSTB}$	RESET Recovery	5.93	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

FG256		FG256		FG256	
Pin Number	AGLE600 Function	Pin Number	AGLE600 Function	Pin Number	AGLE600 Function
A1	GND	C5	GAC0/IO02NDB0V0	E9	IO21NDB1V0
A2	GAA0/IO00NDB0V0	C6	GAC1/IO02PDB0V0	E10	VCCIB1
A3	GAA1/IO00PDB0V0	C7	IO15NDB0V2	E11	VCCIB1
A4	GAB0/IO01NDB0V0	C8	IO15PDB0V2	E12	VMV1
A5	IO05PDB0V0	C9	IO20PDB1V0	E13	GBC2/IO38PDB2V0
A6	IO10PDB0V1	C10	IO25NDB1V0	E14	IO37NDB2V0
A7	IO12PDB0V2	C11	IO27PDB1V0	E15	IO41NDB2V0
A8	IO16NDB0V2	C12	GBC0/IO33NDB1V1	E16	IO41PDB2V0
A9	IO23NDB1V0	C13	VCCPLB	F1	IO124PDB7V0
A10	IO23PDB1V0	C14	VMV2	F2	IO125PDB7V0
A11	IO28NDB1V1	C15	IO36NDB2V0	F3	IO126PDB7V0
A12	IO28PDB1V1	C16	IO42PDB2V0	F4	IO130NDB7V1
A13	GBB1/IO34PDB1V1	D1	IO128PDB7V1	F5	VCCIB7
A14	GBA0/IO35NDB1V1	D2	IO129PDB7V1	F6	GND
A15	GBA1/IO35PDB1V1	D3	GAC2/IO132PDB7V1	F7	VCC
A16	GND	D4	VCOMPLA	F8	VCC
B1	GAB2/IO133PDB7V1	D5	GNDQ	F9	VCC
B2	GAA2/IO134PDB7V1	D6	IO09NDB0V1	F10	VCC
B3	GNDQ	D7	IO09PDB0V1	F11	GND
B4	GAB1/IO01PDB0V0	D8	IO13PDB0V2	F12	VCCIB2
B5	IO05NDB0V0	D9	IO21PDB1V0	F13	IO38NDB2V0
B6	IO10NDB0V1	D10	IO25PDB1V0	F14	IO40NDB2V0
B7	IO12NDB0V2	D11	IO27NDB1V0	F15	IO40PDB2V0
B8	IO16PDB0V2	D12	GNDQ	F16	IO45PSB2V1
B9	IO20NDB1V0	D13	VCOMPLB	G1	IO124NDB7V0
B10	IO24NDB1V0	D14	GBB2/IO37PDB2V0	G2	IO125NDB7V0
B11	IO24PDB1V0	D15	IO39PDB2V0	G3	IO126NDB7V0
B12	GBC1/IO33PDB1V1	D16	IO39NDB2V0	G4	GFC1/IO120PPB7V0
B13	GBB0/IO34NDB1V1	E1	IO128NDB7V1	G5	VCCIB7
B14	GNDQ	E2	IO129NDB7V1	G6	VCC
B15	GBA2/IO36PDB2V0	E3	IO132NDB7V1	G7	GND
B16	IO42NDB2V0	E4	IO130PDB7V1	G8	GND
C1	IO133NDB7V1	E5	VMV0	G9	GND
C2	IO134NDB7V1	E6	VCCIB0	G10	GND
C3	VMV7	E7	VCCIB0	G11	VCC
C4	VCCPLA	E8	IO13NDB0V2	G12	VCCIB2

FG896	
Pin Number	AGLE3000 Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1

FG896	
Pin Number	AGLE3000 Function
AA8	IO245NDB6V1
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1

FG896	
Pin Number	AGLE3000 Function
AB13	IO206PDB5V1
AB14	IO198NDB5V0
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4

FG896	
Pin Number	AGLE3000 Function
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1

FG896	
Pin Number	AGLE3000 Function
AD22	VCCIB4
AD23	TCK
AD24	VCC
AD25	TRST
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND

FG896	
Pin Number	AGLE3000 Function
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	VCC
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ

FG896	
Pin Number	AGLE3000 Function
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0

FG896	
Pin Number	AGLE3000 Function
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0

FG896	
Pin Number	AGLE3000 Function
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7

Revision	Changes	Page
Revision 6 (Feb 2009) Product Brief v1.3	The "Pro (Professional) I/O" section was revised to add two bullets regarding wide range power supply voltage support.	I
	3.0 V was added to the list of supported voltages in the "Pro I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new.	1-7
Revision 5 (Oct 2008) Product Brief v1.2	The Quiescent Current values in Table 1 • IGLOOe Product Family table were updated.	I
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather than simulation values.	N/A
	Table 2-144 • IGLOOe CCC/PLL Specification was updated to add VMV to the VCCI parameter row and remove the word "output" from the parameter description for VCCI. Table note 3 was added.	2-92
	Table 2-2 • Recommended Operating Conditions 1 was updated to include the T _J parameter. Table note 9 is new.	2-2
	In Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature ¹ , the maximum operating junction temperature was changed from 110° to 100°.	2-3
	VMV was removed from Table 2-4 • Overshoot and Undershoot Limits 1, 3 . The title of the table was revised to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels is new.	2-5
	EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-9 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode* , Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Sleep Mode* , and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode* were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode* .	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode ¹ was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.	2-8
	Table note 3 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and referenced for 1.2 V LVCMOS.	2-9

Revision	Changes	Page
Advance v0.4 (December 2007)	The Table 1 • IGLOOe Product Family table was updated to change the maximum number of user I/Os for AGLE3000.	I
	The "IGLOOe FPGAs Package Sizes Dimensions" table is new. Package dimensions were removed from the "I/Os Per Package¹" table. The number of I/Os was updated for FG896.	II
	A note regarding marking information was added to the "IGLOOe Ordering Information" table.	III
	Table 2-4 • IGLOOe CCC/PLL Specification and Table 2-5 • IGLOOe CCC/PLL Specification were updated.	2-18, 2-19
	The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core.	2-60
	Figure 2-38 • Flash*Freeze Mode Type 1 – Timing Diagram was updated to modify the LSICC signal.	2-56
	Table 2-32 • Flash*Freeze Pin Location in IGLOOe Family Packages (device-independent) was updated for the FG896 package.	2-64
	Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal.	2-58
	Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section.	3-6
	Table 3-8 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode† was updated.	3-6
	Table 3-9 • Quiescent Supply Current (IDD), IGLOOe Sleep Mode (VCC = 0 V)† was updated.	3-6
	Table 3-11 • Quiescent Supply Current, No IGLOOe Flash*Freeze Mode ¹ was updated.	3-6
	Table 3-99 • Minimum and Maximum DC Input and Output Levels was updated.	3-51
	Table 3-136 • JTAG 1532 and Table 3-135 • JTAG 1532 were updated.	3-95
	The "484-Pin FBGA" table for AGLE3000 is new.	4-11
	The "896-Pin FBGA" package and table for AGLE3000 is new.	4-16
Advance v0.3 (September 2007)	Cortex-M1 device information was added to the Table 1 • IGLOOe Product Family table, the "I/Os Per Package 1" table, "IGLOOe Ordering Information" , and "Temperature Grade Offerings" .	I, II, III, IV
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOOe Ordering Information" , "Temperature Grade Offerings" , and "Speed Grade and Temperature Grade Matrix" sections.	III, IV
	The T _J parameter in Table 3-2 • Recommended Operating Conditions was changed to T _A , ambient temperature, and table notes 6–8 were added.	3-2