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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1agle3000v5-fgg896

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1 – IGLOOe Device Family Overview

General Description

The IGLOOe family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOOe devices enables entering and exiting an ultra-low power mode while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOOe device is completely functional in the system. This allows the IGLOOe device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOOe devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOOe is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOOe devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on 6 integrated phase-locked loops (PLLs). IGLOOe devices have up to 3 million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

M1 IGLOOe devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOOe device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Microsemi for use in M1 IGLOOe FPGAs.

The ARM-enabled devices have Microsemi ordering numbers that begin with M1AGLE and do not support AES decryption.

Flash*Freeze Technology

The IGLOOe device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOOe devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOOe V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOOe device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOOe devices the best fit for portable electronics.

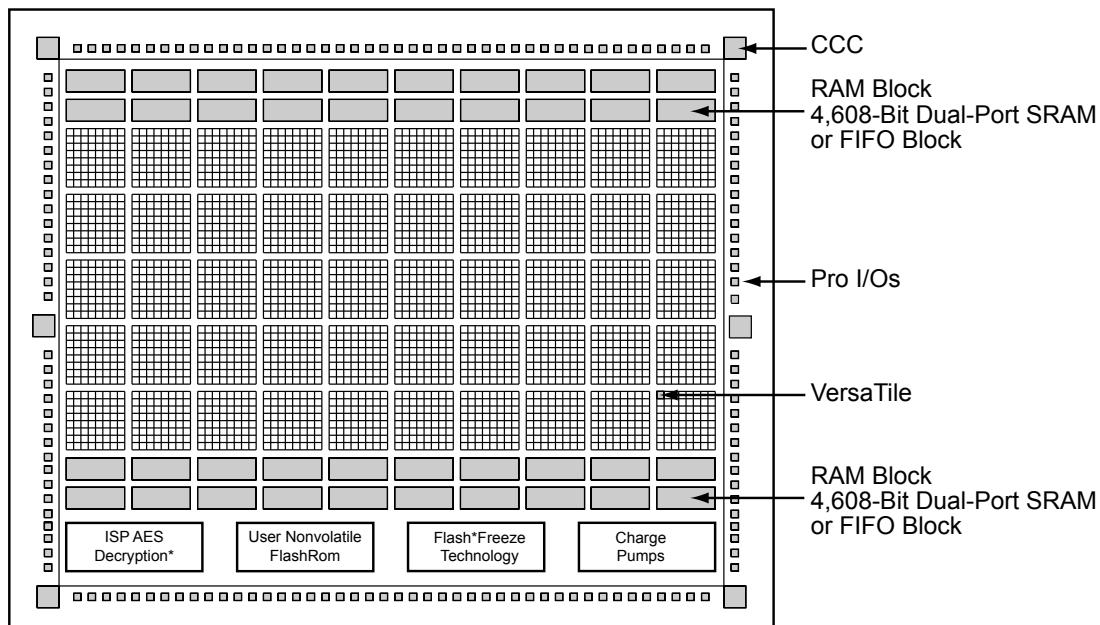


Figure 1-1 • IGLOOe Device Architecture Overview

Flash*Freeze Technology

The IGLOOe device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static and dynamic capabilities of the IGLOOe device. Refer to [Figure 1-2](#) for an illustration of entering/exiting Flash*Freeze mode.

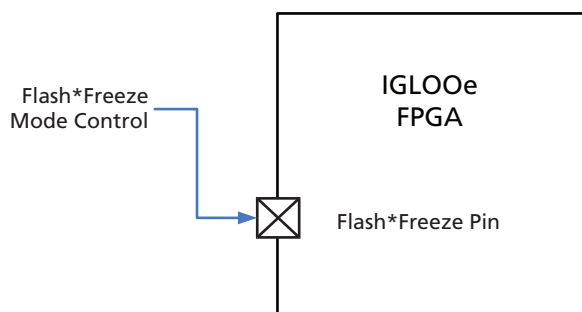


Figure 1-2 • IGLOOe Flash*Freeze Mode

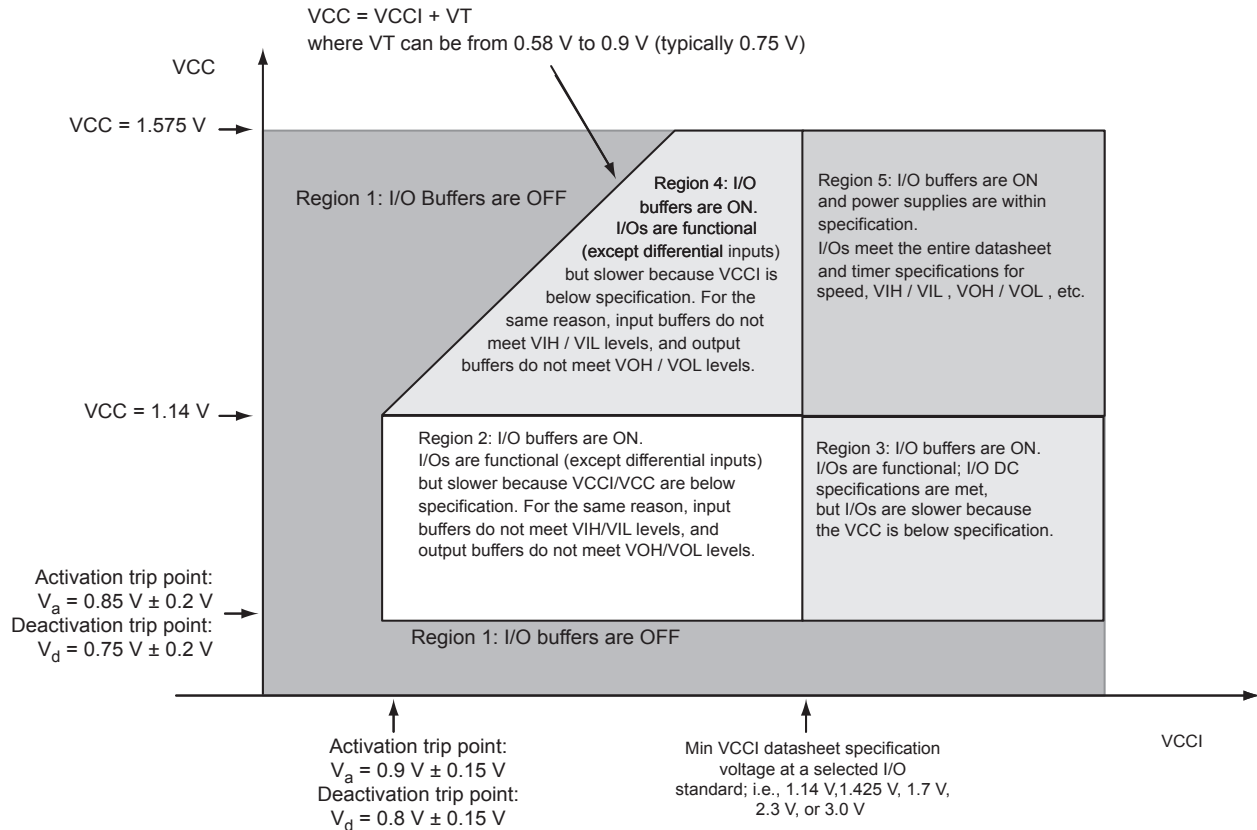


Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in [Table 2-5](#).

P = Power dissipation

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range ³	3.3	–	16.34
3.3 V LVCMOS Wide Range – Schmitt trigger ³	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS ⁴	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger ⁴	1.2	–	0.53
1.2 V LVCMOS Wide Range ⁴	1.2	–	0.60
1.2 V LVCMOS Wide Range – Schmitt trigger ⁴	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	.079
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. PDC6 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.
4. Applicable for IGLOOe V2 devices only.

Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL/LVCMOS	5	3.3	–	148.00
3.3 V LVCMOS Wide Range ⁴	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS (JESD8-11)	5	1.2	–	17.94
1.2 V LVCMOS (JESD8-11) – Wide Range				17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.18
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.67
SSTL3 (II)	30	3.3	42.21	131.69
Differential				
LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	167.86

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PDC7 is the static power (where applicable) measured on V_{CCI}.
3. PAC10 is the total dynamic power measured on V_{CCI}.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case V_{CCI} (per standard)

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{POUT} (ns)	t_{PP} (ns)	t_{PIN} (ns)	t_{PV} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12	12	High	5	—	1.55	2.47	0.26	1.31	1.58	1.10	2.51	2.04	3.28	3.97	8.29	7.82	ns
3.3 V LVCMOS Wide Range ^{1,2}	100 μA	12	High	35	—	1.55	3.40	0.26	1.66	2.14	1.10	3.40	2.68	4.55	5.49	9.19	8.46	ns
2.5 V LVCMOS	12	12	High	5	—	1.55	2.51	0.26	1.55	1.77	1.10	2.54	2.22	3.36	3.85	8.33	8.00	ns
1.8 V LVCMOS	12	12	High	5	—	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns
1.5 V LVCMOS	12	12	High	5	—	1.55	3.10	0.26	1.72	2.16	1.10	3.15	2.70	3.86	4.68	8.93	8.49	ns
1.2 V LVCMOS	2	2	High	5	—	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns
1.2 V LVCMOS Wide Range ^{1,3}	100 μA	2	High	5	—	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns
3.3 V PCI	Per PCI spec	—	High	10	25 ⁴	1.55	2.76	0.26	1.19	1.63	1.10	2.79	2.16	3.29	3.97	8.58	7.94	ns
3.3 V PCI-X	Per PCI-X spec	—	High	10	25 ⁴	1.55	2.76	0.25	1.22	1.58	1.10	2.79	2.16	3.29	3.97	8.58	7.94	ns
3.3 V GTL	20 ⁵	—	High	10	25	1.55	2.08	0.25	2.76	—	1.10	2.09	2.08	—	—	7.88	7.87	ns
2.5 V GTL	20 ⁵	—	High	10	25	1.55	2.17	0.25	2.35	—	1.10	2.20	2.13	—	—	7.99	7.91	ns
3.3 V GTL+	35	—	High	10	25	1.55	2.12	0.25	1.62	—	1.10	2.14	2.07	—	—	7.93	7.85	ns
2.5 V GTL+	33	—	High	10	25	1.55	2.25	0.25	1.55	—	1.10	2.27	2.10	—	—	8.06	7.89	ns
HSTL (I)	8	—	High	20	50	1.55	3.09	0.25	1.95	—	1.10	3.11	3.09	—	—	8.90	8.88	ns
HSTL (II)	15	—	High	20	25	1.55	2.94	0.25	1.95	—	1.10	2.98	2.74	—	—	8.77	8.53	ns
SSTL2 (I)	15	—	High	30	50	1.55	2.18	0.25	1.40	—	1.10	2.21	2.03	—	—	7.99	7.82	ns
SSTL2 (II)	18	—	High	30	25	1.55	2.21	0.25	1.40	—	1.10	2.24	1.97	—	—	8.03	7.76	ns
SSTL3 (I)	14	—	High	30	50	1.55	2.33	0.25	1.33	—	1.10	2.36	2.02	—	—	8.15	7.81	ns
SSTL3 (II)	21	—	High	30	25	1.55	2.13	0.25	1.33	—	1.10	2.16	1.89	—	—	7.94	7.67	ns

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-49](#) for connectivity. This resistor is not required during normal operation.
5. Output drive strength is below JEDEC specification.
6. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	6	6	35	44	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	8	8	45	51	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	12	12	91	74	10	10
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	16	16	91	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

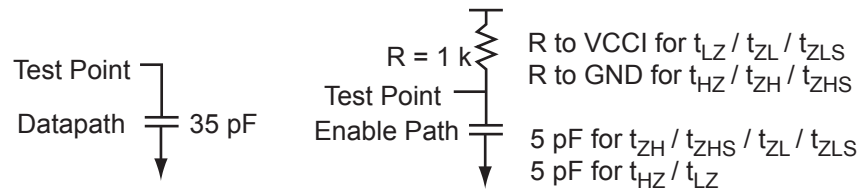


Figure 2-9 • AC Loading

Table 2-53 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	–	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-77 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
20 mA ⁵	-0.3	VREF - 0.05	VREF + 0.05	3.6	0.4	-	20	20	169	124	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Output drive strength is below JEDEC specification.

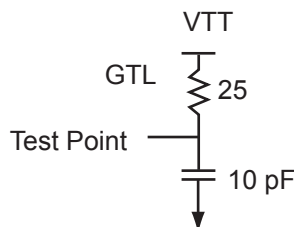


Figure 2-14 • AC Loading

Table 2-78 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-79 • 2.5 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.98	1.90	0.19	2.04	0.67	1.94	1.87			5.57	5.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-80 • 2.5 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	1.55	2.16	0.26	2.35	1.10	2.20	2.13			8.01	7.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
8 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	32	39	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

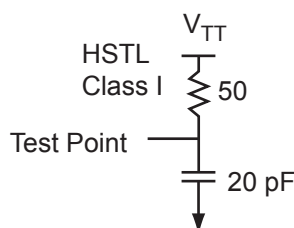


Figure 2-17 • AC Loading

Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See [Table 2-23 on page 2-23](#) for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-91 • HSTL Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.98	2.74	0.19	1.77	0.67	2.79	2.73			6.42	6.36	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	1.55	3.10	0.26	1.94	1.10	3.12	3.10			8.93	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-101 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
18 mA	−0.3	VREF − 0.2	VREF + 0.2	3.6	0.35	VCCI − 0.43	18	18	169	124	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

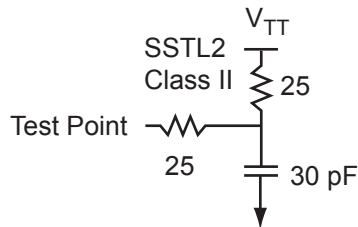


Figure 2-20 • AC Loading

Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.98	1.94	0.19	1.15	0.67	1.97	1.66			5.60	5.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	1.55	2.20	0.26	1.39	1.10	2.24	1.97			8.05	7.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-117 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-118 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)
1.64	1.94	Cross point	–

Note: *Measuring point = V_{trip} . See [Table 2-23 on page 2-23](#) for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-119 • LVPECL – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.98	1.75	0.19	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-120 • LVPECL – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.16	0.26	1.70	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-121 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{iCLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{iSUD}	Data Setup Time for the Input Data Register	C, A
t_{iHD}	Data Hold Time for the Input Data Register	C, A
t_{iSUE}	Enable Setup Time for the Input Data Register	B, A
t_{iHE}	Enable Hold Time for the Input Data Register	B, A
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: See Figure 2-26 on page 2-66 for more information.

Output Register

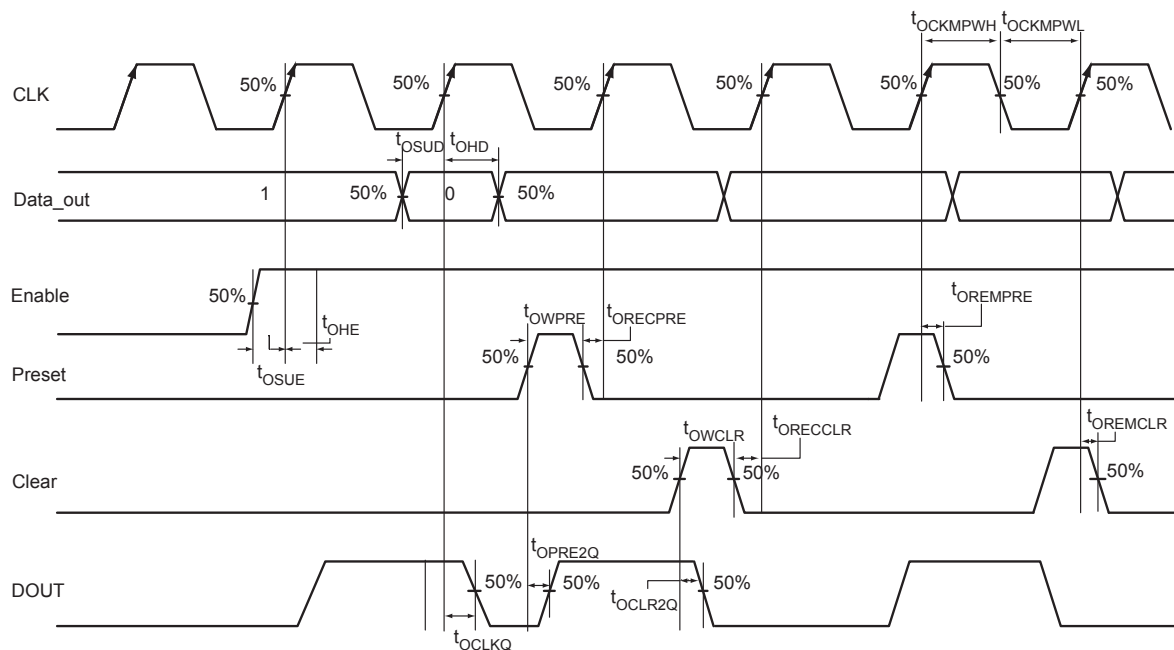


Figure 2-29 • Output Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-125 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOOe library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [IGLOO](#), [Fusion](#), and [ProASIC3 Macro Library Guide](#).

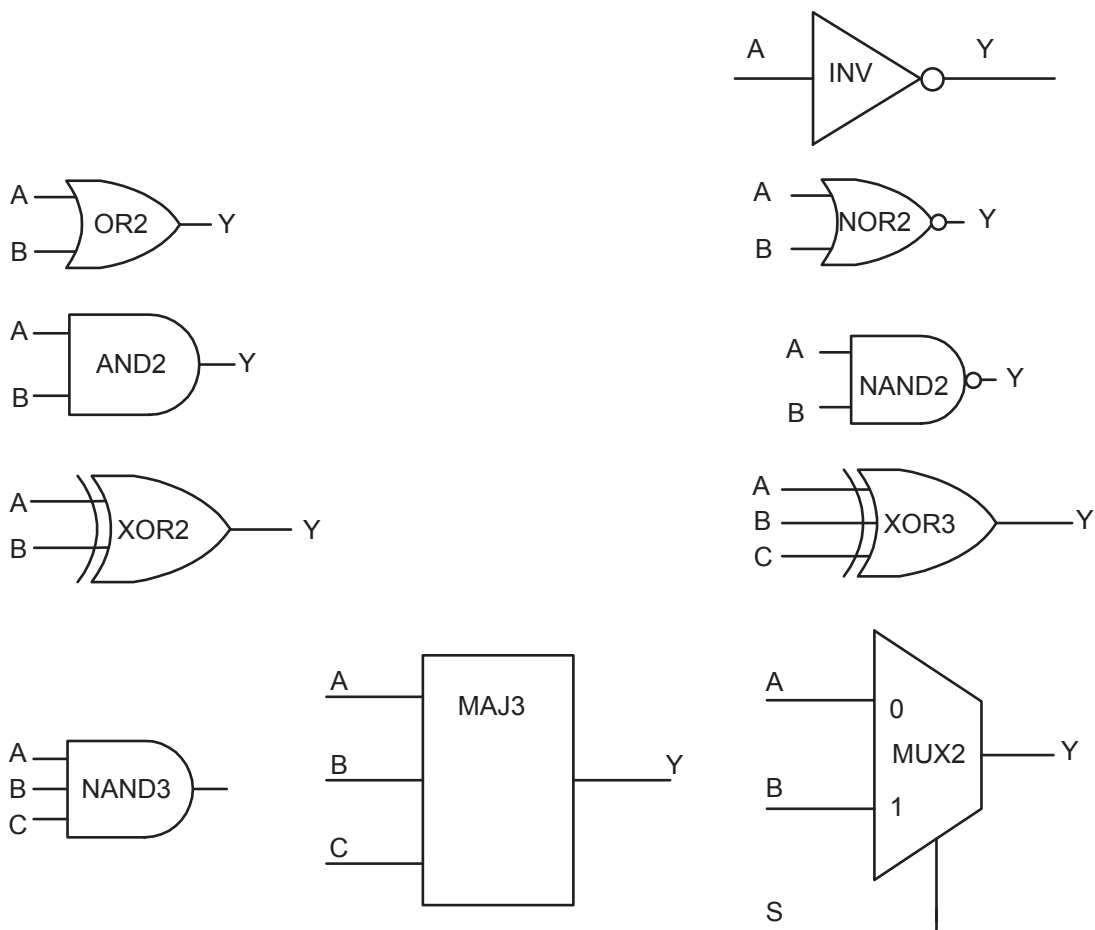


Figure 2-35 • Sample of Combinatorial Cells

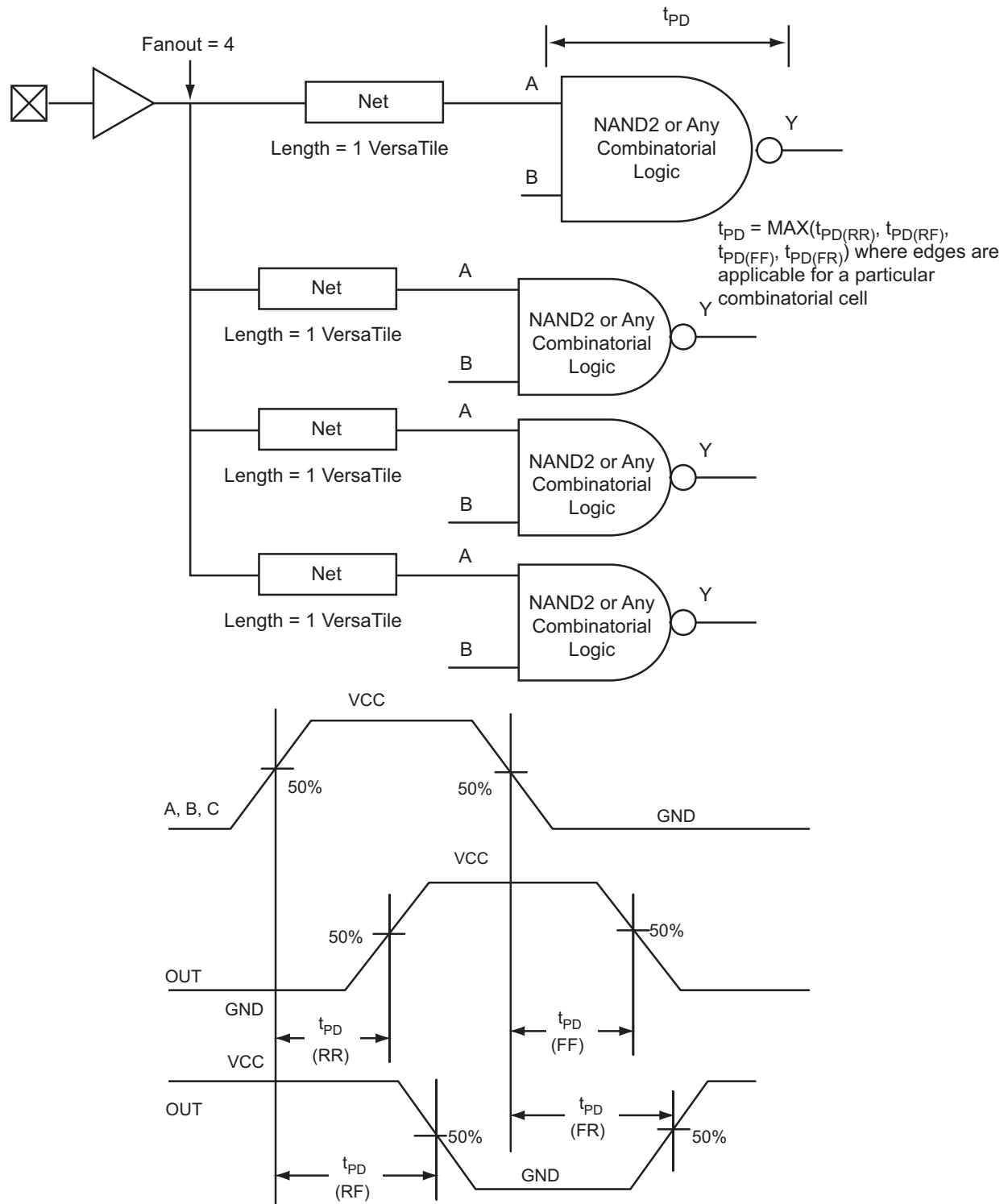


Figure 2-36 • Timing Model and Waveforms

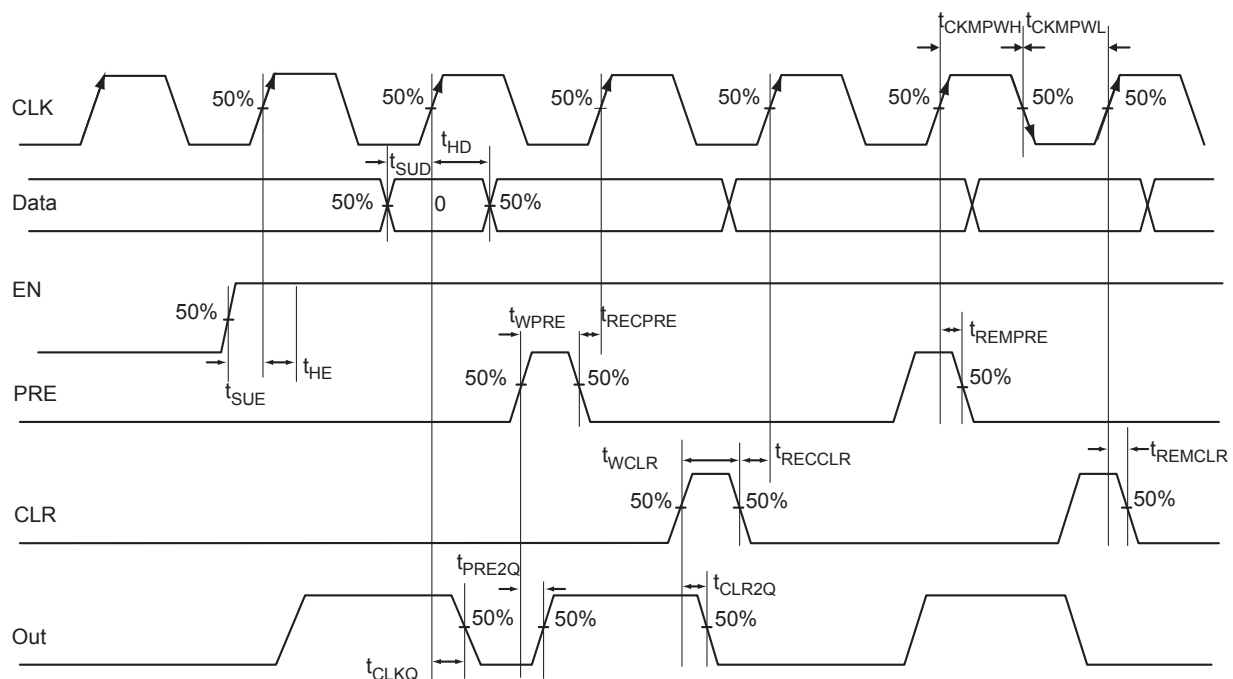


Figure 2-38 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-137 • Register Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
$t_{REMCCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-147 • RAM4K9

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	1.53	ns
t_{AH}	Address Hold Time	0.29	ns
t_{ENS}	REN, WEN Setup Time	1.50	ns
t_{ENH}	REN, WEN Hold Time	0.29	ns
t_{BKS}	BLK Setup Time	3.05	ns
t_{BKH}	BLK Hold Time	0.29	ns
t_{DS}	Input Data (DIN) Setup Time	1.33	ns
t_{DH}	Input Data (DIN) Hold Time	0.66	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.30	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.89	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.01	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (pass-through)	3.86	ns
	RESET Low to Data Out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET Removal	1.12	ns
$t_{RECRSTB}$	RESET Recovery	5.93	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

FG256		FG256		FG256	
Pin Number	AGLE600 Function	Pin Number	AGLE600 Function	Pin Number	AGLE600 Function
G13	GCC1/IO50PPB2V1	K1	GFC2/IO115PSB6V1	M5	VMV5
G14	IO44NDB2V1	K2	IO113PPB6V1	M6	VCCIB5
G15	IO44PDB2V1	K3	IO112PDB6V1	M7	VCCIB5
G16	IO49NSB2V1	K4	IO112NDB6V1	M8	IO84NDB5V0
H1	GFB0/IO119NPB7V0	K5	VCCIB6	M9	IO84PDB5V0
H2	GFA0/IO118NDB6V1	K6	VCC	M10	VCCIB4
H3	GFB1/IO119PPB7V0	K7	GND	M11	VCCIB4
H4	VCOMPLF	K8	GND	M12	VMV3
H5	GFC0/IO120NPB7V0	K9	GND	M13	VCCPLD
H6	VCC	K10	GND	M14	GDB1/IO66PPB3V1
H7	GND	K11	VCC	M15	GDC1/IO65PDB3V1
H8	GND	K12	VCCIB3	M16	IO61NDB3V1
H9	GND	K13	IO54NPB3V0	N1	IO105PDB6V0
H10	GND	K14	IO57NPB3V0	N2	IO105NDB6V0
H11	VCC	K15	IO55NPB3V0	N3	GEC1/IO104PPB6V0
H12	GCC0/IO50NPB2V1	K16	IO57PPB3V0	N4	VCOMPLE
H13	GCB1/IO51PPB2V1	L1	IO113NPB6V1	N5	GNDQ
H14	GCA0/IO52NPB3V0	L2	IO109PPB6V0	N6	GEA2/IO101PPB5V2
H15	VCOMPLC	L3	IO108PDB6V0	N7	IO92NDB5V1
H16	GCB0/IO51NPB2V1	L4	IO108NDB6V0	N8	IO90NDB5V1
J1	GFA2/IO117PSB6V1	L5	VCCIB6	N9	IO82NDB5V0
J2	GFA1/IO118PDB6V1	L6	GND	N10	IO74NDB4V1
J3	VCCPLF	L7	VCC	N11	IO74PDB4V1
J4	IO116NDB6V1	L8	VCC	N12	GNDQ
J5	GFB2/IO116PDB6V1	L9	VCC	N13	VCOMPLD
J6	VCC	L10	VCC	N14	VJTAG
J7	GND	L11	GND	N15	GDC0/IO65NDB3V1
J8	GND	L12	VCCIB3	N16	GDA1/IO67PDB3V1
J9	GND	L13	GDB0/IO66NPB3V1	P1	GEB1/IO103PDB6V0
J10	GND	L14	IO60NDB3V1	P2	GEB0/IO103NDB6V0
J11	VCC	L15	IO60PDB3V1	P3	VMV6
J12	GCB2/IO54PPB3V0	L16	IO61PDB3V1	P4	VCCPLE
J13	GCA1/IO52PPB3V0	M1	IO109NPB6V0	P5	IO101NPB5V2
J14	GCC2/IO55PPB3V0	M2	IO106NDB6V0	P6	IO95PPB5V1
J15	VCCPLC	M3	IO106PDB6V0	P7	IO92PDB5V1
J16	GCA2/IO53PSB3V0	M4	GEC0/IO104NPB6V0	P8	IO90PDB5V1

FG896	
Pin Number	AGLE3000 Function
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC
AG3	IO232NPB5V4
AG4	GND
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC

FG896	
Pin Number	AGLE3000 Function
AH4	FF/GE2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2

FG896	
Pin Number	AGLE3000 Function
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4