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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8247cvrtiea

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
 - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
 - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
 - Microcode tracing capabilities
 - Eight CPM trap registers
- Universal serial bus (USB) controller
 - Supports USB 2.0 full/low rate compatible
 - USB host mode
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loopback mode for diagnostics (12 Mbps only)
 - Supports USB slave mode
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate
 - Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Two fast communication controllers (FCCs) supporting the following protocols:
 - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
 - Transparent
 - HDLC—up to T3 rates (clear channel)



Operating Conditions

I/O supply voltage

Junction temperature (maximum)

Input voltage

1

This table lists recommended operational voltage conditions.

•	•	
Rating	Symbol	Value
Core supply voltage	VDD	1.425 – 575
PLL supply voltage	VCCSYN	1.425 – 575

VDDH

VIN

Τi

Table 4. Recommended Operating Conditions¹

 Ambient temperature
 T_A
 0-70²
 °C

 Caution: These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.
 State
 State

² Note that for extended temperature parts the range is $(-40)_{T_A} - 105_{T_i}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

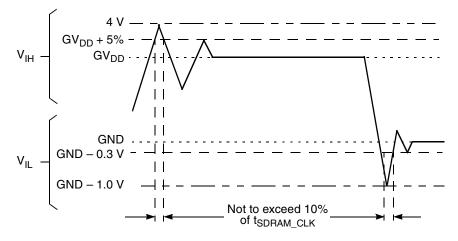


Figure 2. Overshoot/Undershoot Voltage

Unit

V

V

V

V

°C

3.135 - 3.465

GND (-0.3) - 3.465

105²



DC Electrical Characteristics

⁵ MPC8272 and MPC8271 only.

Table 6.

Characteristic	Symbol	Min	Мах	Unit
Input high voltage—all inputs except TCK, TRST and PORESET ¹	V _{IH}	2.0	3.465	V
Input low voltage	V _{IL}	GND	0.8	V
CLKIN input high voltage	V _{IHC}	2.4	3.465	V
CLKIN input low voltage	V _{ILC}	GND	0.4	V
Input leakage current, V _{IN} = VDDH ²	I _{IN}		10	μA
Hi-Z (off state) leakage current, V _{IN} = VDDH ²	I _{OZ}		10	μA
Signal low input current, $V_{IL} = 0.8 V^3$	١L	_	1	μA
Signal high input current, V _{IH} = 2.0 V	I _H	_	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except UTOPIA mode, and open drain pins In UTOPIA mode ⁴ (UTOPIA pins only): $I_{OH} = -8.0 \text{mA}$	V _{OH}	2.4	_	V
In UTOPIA mode ⁴ (UTOPIA pins only): I _{OL} = 8.0mA	V _{OL}	_	0.5	V
IoL = 6.0mA BR BG ABB/IRQ2 TS A[0-31] TTI[0-4] TBST TSIZE[0-3] AACK ARTRY DBG DBB/IRQ3 D[0-63] //EXT_BR3 //EXT_BR3 //EXT_BG3 /TEN/EXT_DBG3/CINT PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 BADDR31/IRQ5/CINT CPU_BR IRQ0/NMI_OUT /PCL_RST HRESET SRESET REQONF	V _{OL}		0.4	V



DC Electrical Characteristics

Та	h	P	6	
ıa	N	e.	υ.	

Characteristic	Symbol	Min	Max	Unit
I _{OL} = 5.3mA	V _{OL}		0.4	V
CS[0-9]	VOL VOL		0.4	v
CS(10)/BCTL1				
<u>CS(11)/AP(0)</u>				
BADDR[27–28]				
ALE				
BCTLO				
PWE[0-7]/PSDDQM[0-7]/PBS[0-7]				
PSDA10/PGPL0				
PSDWE/PGPL1				
POE/PSDRAS/PGPL2				
PSDCAS/PGPL3				
PGTA/PUPMWAIT/PGPL4/PPBS				
PSDAMUX/PGPL5				
LWE[0-3]LSDDQM[0-3]/LBS[0-3]/PCI_CFG[0-3]				
LSDA10/LGPL0/PCI_MODCKH0				
LSDWE/LGPL1/PCI_MODCKH1				
LOE/LSDRAS/LGPL2/PCI_MODCKH2				
LSDCAS/LGPL3/PCI_MODCKH3				
LGTA/LUPMWAIT/LGPL4/LPBS				
LSDAMUX/LGPL5/PCI_MODCK				
LWR				
MODCK[1-3]/AP[1-3]/TC[0-2]/BNKSEL[0-2]				
I _{OL} = 3.2mA				
L_A14/PAR				
L_A15/FRAME/SMI				
L_A16/TRDY				
L_A17/IRDY/CKSTP_OUT				
L_A18/STOP				
L_A19/DEVSEL				
L_A20/IDSEL				
L_A21/PERR				
L_A22/SERR				
L_A23/ <u>REQ0</u>				
L_A24/REQ1/HSEJSW				
L_A25/GNT0				
L_A26/GNT1/HSLED				
L_A27/GNT2/HSENUM				
L_A29/INTAL_A30/REQ2				
LCL_D[0-31)]/AD[0-31] LCL_DP[03]/C/BE[0-3]				
PA[0–31]				
PB[4–31]				
PC[0-31]				
PD[4–31]				
TDO				
QREQ				

TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ have min VIH = 2.5V. 1

² The leakage current is measured for nominal VDDH,VCCSYN, and VDD.
 ³ V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.



AC Electrical Characteristics

This figure shows the FCC external clock.

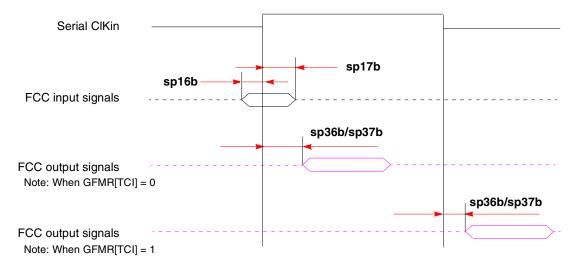
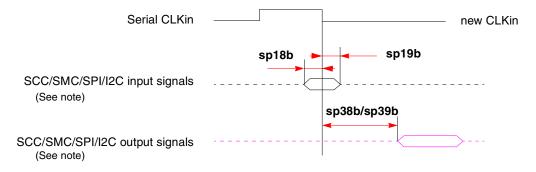


Figure 4. FCC External Clock Diagram

This figure shows the SCC/SMC/SPI/I²C external clock.



Note: There are four possible timing conditions for SPI:

- 1. Input sampled on the rising edge and output driven on the rising edge.
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge (shown).
- 4. Input sampled on the falling edge and output driven on the rising edge.

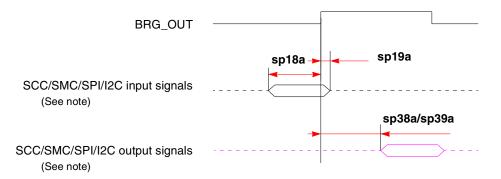
Note: There are two possible timing conditions for SCC/SMC/I²C:

- 1. Input sampled on the falling edge and output driven on the falling edge (shown).
- 2. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram



This figure shows the SCC/SMC/SPI/I²C internal clock.

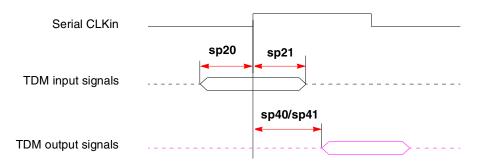


Note: There are four possible timing conditions for SCC and SPI:

- 1. Input sampled on the rising edge and output driven on the rising edge (shown).
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge.
- 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

- 1. Input sampled on the rising edge and output driven on the rising edge (shown).
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge.
- 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram



7 Clock Configuration Modes

As shown in this table, the clocking mode is set according to two sources:

- PCI_CFG[0]— An input signal. Also defined as "PCI_HOST_EN." See Chapter 6, "External Signals," and Chapter 9, "PCI Bridge," in the SoC reference manual.
- PCI_MODCK—Bit 27 in the Hard Reset Configuration Word. See Chapter 5, "Reset," in the SoC reference manual.

Pi	ns	Clocking Mode	PCI Clock Frequency Range (MHz)	Reference		
PCI_CFG[0] ¹	PCI_MODCK ²	Clocking Mode	Torolock rrequency hange (Milz)			
0	0	PCI host	50–66	Table 17		
0	1		25–50	Table 18		
1	0	PCI agent	50–66	Table 19		
1	1		25–50	Table 20		

Table 16. SoC Clocking Modes

¹ PCI_HOST_EN

² Determines PCI clock frequency range.

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

NOTE

Clock configurations change only after PORESET is asserted.

NOTE: Tval (Output Hold)

The minimum Tval = 2 ns when $PCI_MODCK = 1$, and the minimum Tval = 1 ns when $PCI_MODCK = 0$. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

7.1 PCI Host Mode

These tables show configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI host mode the input clock is the bus clock.



Mode ³		Clock Hz)	CPM Multiplication	CPM Clock (MHz)		CPU Multiplication		U Clock (MHz) PCI Division			Clock Hz)
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor ⁶	Low	High
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0101_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0101_010	50.0	66.7	2	100.0	133.3	3.5	175.0	233.3	2	50.0	66.7
0101_011	50.0	66.7	2	100.0	133.3	4	200.0	266.6	2	50.0	66.7
0101_100	50.0	66.7	2	100.0	133.3	4.5	225.0	300.0	2	50.0	66.7
0101_101	83.3	111.1	3	250.0	333.3	3.5	291.7	388.9	5	50.0	66.7
0101_110	83.3	111.1	3	250.0	333.3	4	333.3	444.4	5	50.0	66.7
0101_111	83.3	111.1	3	250.0	333.3	4.5	375.0	500.0	5	50.0	66.7
	1	1					1				
0110_000	60.0	80.0	2.5	150.0	200.0	2.5	150.0	200.0	3	50.0	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0110_011	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7
0111_000						Reserved					
0111_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0111_010	50.0	66.7	3	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0111_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0111_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
	1										
1000_000						Reserved	1				
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0) ^{1,2} (continued)



Mode ³	Bus Clock (MHz)		CPM Multiplication				PCI Division		Clock Hz)		
MODCK_H- MODCK[1-3]	Low	High	Eactor ⁴	Low	High	Factor ⁵	Low	High	Factor ⁶	Low	High
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000						Reserved					
1100_001						Reserved					
1100_010						Reserved					

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

¹ The "low" values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The "high" values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPU frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor



Mode ³		Clock Hz)	CPM		Clock Hz)	CPU		Clock Hz)	Bus		Clock Hz)
MODCK_H- MODCK[1-3]	Low	High	Multiplication Factor ⁴	Low	High	Multiplication Factor ⁵	Low	High	Division Factor	Low	High
1000_000			Γ			Reserved			r		
1000_001	50.0	66.7	3	150.0	200.0	2.5	150.0	166.7	2.5	60.0	80.0
1000_010	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
1000_011	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
1000_100	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
1000_101	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
1001_000						Reserved					
1001_001						Reserved					
1001_010						Reserved					
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0		4.5	225.0		4	50.0	66.7
1010_000						Reserved					
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000						Reserved					
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
	1	1	1	1	1		1	r		1	
1011_101	50.0	66.7	4	200.0	266.6	2.5	250.0	333.3	2	100.0	133.3
1011_110	50.0	66.7	4	200.0	266.6	3	300.0	400.0	2	100.0	133.3
1011_111	50.0	66.7	4	200.0	266.6	3.5	350.0	466.6	2	100.0	133.3

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2} (continued)



		CPM Multiplication	-		CPU			Bus	Bus Clock (MHz)	
Low	High	Factor ⁴		Factor	Low	High				
50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7
50.0	66.7	5	250.0	333.3	4	500.0	666.6	2	125.0	166.7
										•
50.0	66.7	5	250.0	333.3	4	333.3	444.4	3	83.3	111.1
50.0	66.7	5	250.0	333.3	4.5	375.0	500.0	3	83.3	111.1
50.0	66.7	5	250.0	333.3	5	416.7	555.5	3	83.3	111.1
50.0	66.7	5	250.0	333.3	5.5	458.3	611.1	3	83.3	111.1
		•						•		
					Reserved					
					Reserved					
					Reserved					
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FactorS((MHz)LowHighLowHighLowHighLowHigh50.066.76300.0400.04.5.0500.050.050.066.76300.0400.05.5.0500.066.650.066.76300.0400.05.5.0550.073.350.066.76300.0400.05.5.0550.073.350.066.76300.0400.03.5.5420.0559.950.066.76300.0400.04.5.5540.079.950.066.76300.0400.04.5.5540.079.950.066.776300.0400.04.5.5500.079.950.066.776300.0400.04.5.5500.079.950.066.775250.033.33.15.5416.7540.050.066.75250.033.33.5.5437.5533.350.066.75250.033.33.4.5313.5416.750.066.75250.033.34.5.530.030.0400.050.066.75250.033.34.5.5350.0350.0350.050.066.75250.033.33.5.5416.7550.050.066</td><td>(MHz)CPM Multiplication Factor4(MHz)CPU Multiplication Factor5(MHz)Bus Division Factor5Bus Division50.066.76300.040.044400.053.3350.066.76300.040.04.5450.059.9350.066.76300.040.05.550.066.6350.066.76300.040.05.5550.073.3350.066.76300.040.05.5550.073.3350.066.76300.040.03.5420.0559.92.550.066.76300.040.03.5420.0559.92.550.066.76300.040.0480.063.92.550.066.76300.040.0480.063.92.550.066.76300.040.0480.060.079.92.550.066.75250.033.33.5416.6250.066.75250.033.33.5416.6250.066.75250.033.33.5416.7350.066.75250.033.33.5416.7350.066.7533.33.433.344.4350.066.75250.033.35.5458.331.1</td></t<><td>(MH2)CPM Multiplication Factor4(M(M+z)Bus Multiplication Factor5(M(M50.066.766.0300.0400.044.00533.33.3100.050.066.766.0300.0400.04.50.059.93.0100.050.066.766.0300.0400.05.50.0500.066.63.00.0100.050.066.766.0300.0400.05.50.0550.073.33.0100.050.066.766.0300.0400.03.5.5550.073.33.0100.050.066.766.0300.0400.03.5.5550.073.33.0100.050.066.766.0300.0400.03.5.5540.071.9.92.5.5120.050.066.766.0300.0400.03.5.5540.071.9.92.5.5120.050.066.766.760.030.040.0550.050.071.9.92.5.5120.050.066.766.760.030.040.0550.050.071.9.92.5.5120.050.066.776300.040.03.3.32.5.071.9.92.5.5120.050.066.7550.030.33.3.33.1.551.0.351.0.92.5.5120.050.066.7550.0250.033.33.4.550.0.366.6.62.2.5120.0<!--</td--></td></td>	(MHz) CPM Multiplication ⁴ (M Low High Low Low 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 6 300.0 50.0 66.7 5 250.0 50.0 66.7 5 250.0 50.0 66.7 5 250.0 50.0 66.7 5 250.0 50.0 66.7 5 250.0 50.0 66.7 5 250.0 50.0 66.7	(MHz) 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FactorS((MHz)LowHighLowHighLowHighLowHigh50.066.76300.0400.04.5.0500.050.050.066.76300.0400.05.5.0500.066.650.066.76300.0400.05.5.0550.073.350.066.76300.0400.05.5.0550.073.350.066.76300.0400.03.5.5420.0559.950.066.76300.0400.04.5.5540.079.950.066.76300.0400.04.5.5540.079.950.066.776300.0400.04.5.5500.079.950.066.776300.0400.04.5.5500.079.950.066.775250.033.33.15.5416.7540.050.066.75250.033.33.5.5437.5533.350.066.75250.033.33.4.5313.5416.750.066.75250.033.34.5.530.030.0400.050.066.75250.033.34.5.5350.0350.0350.050.066.75250.033.33.5.5416.7550.050.066</td><td>(MHz)CPM Multiplication Factor4(MHz)CPU Multiplication Factor5(MHz)Bus Division Factor5Bus Division50.066.76300.040.044400.053.3350.066.76300.040.04.5450.059.9350.066.76300.040.05.550.066.6350.066.76300.040.05.5550.073.3350.066.76300.040.05.5550.073.3350.066.76300.040.03.5420.0559.92.550.066.76300.040.03.5420.0559.92.550.066.76300.040.0480.063.92.550.066.76300.040.0480.063.92.550.066.76300.040.0480.060.079.92.550.066.75250.033.33.5416.6250.066.75250.033.33.5416.6250.066.75250.033.33.5416.7350.066.75250.033.33.5416.7350.066.7533.33.433.344.4350.066.75250.033.35.5458.331.1</td></t<> <td>(MH2)CPM Multiplication Factor4(M(M+z)Bus Multiplication Factor5(M(M50.066.766.0300.0400.044.00533.33.3100.050.066.766.0300.0400.04.50.059.93.0100.050.066.766.0300.0400.05.50.0500.066.63.00.0100.050.066.766.0300.0400.05.50.0550.073.33.0100.050.066.766.0300.0400.03.5.5550.073.33.0100.050.066.766.0300.0400.03.5.5550.073.33.0100.050.066.766.0300.0400.03.5.5540.071.9.92.5.5120.050.066.766.0300.0400.03.5.5540.071.9.92.5.5120.050.066.766.760.030.040.0550.050.071.9.92.5.5120.050.066.766.760.030.040.0550.050.071.9.92.5.5120.050.066.776300.040.03.3.32.5.071.9.92.5.5120.050.066.7550.030.33.3.33.1.551.0.351.0.92.5.5120.050.066.7550.0250.033.33.4.550.0.366.6.62.2.5120.0<!--</td--></td>	(MH)CPM Multiplication Factor4(MH)CPU Multiplication Factor5(MH)50.066.76300.0400.0400.050.066.76300.0400.040.050.066.76300.0400.050.050.066.76300.0400.05.550.066.76300.0400.05.550.066.76300.0400.05.550.066.76300.0400.03.550.066.766.7300.0400.04.550.066.766.7300.0400.04.550.066.766.7300.0400.04.550.066.77.6300.0400.04.550.066.77.6300.0400.05.550.066.77.6300.0400.04.550.066.77.6300.0400.04.550.066.75.5250.033.33.550.066.75.5250.033.34.550.066.75.5250.033.34.550.066.75.5250.033.34.550.066.75.5250.033.34.550.066.75.5250.033.34.550.066.75.5250.033.34.550.066.75.5250.033.34.5<	(MHz)CPM Multiplication FactorA(MHz)CPU Multiplication FactorS((MHz)LowHighLowHighLowHighLowHigh50.066.76300.0400.04.5.0500.050.050.066.76300.0400.05.5.0500.066.650.066.76300.0400.05.5.0550.073.350.066.76300.0400.05.5.0550.073.350.066.76300.0400.03.5.5420.0559.950.066.76300.0400.04.5.5540.079.950.066.76300.0400.04.5.5540.079.950.066.776300.0400.04.5.5500.079.950.066.776300.0400.04.5.5500.079.950.066.775250.033.33.15.5416.7540.050.066.75250.033.33.5.5437.5533.350.066.75250.033.33.4.5313.5416.750.066.75250.033.34.5.530.030.0400.050.066.75250.033.34.5.5350.0350.0350.050.066.75250.033.33.5.5416.7550.050.066	(MHz)CPM Multiplication Factor4(MHz)CPU Multiplication Factor5(MHz)Bus Division Factor5Bus Division50.066.76300.040.044400.053.3350.066.76300.040.04.5450.059.9350.066.76300.040.05.550.066.6350.066.76300.040.05.5550.073.3350.066.76300.040.05.5550.073.3350.066.76300.040.03.5420.0559.92.550.066.76300.040.03.5420.0559.92.550.066.76300.040.0480.063.92.550.066.76300.040.0480.063.92.550.066.76300.040.0480.060.079.92.550.066.75250.033.33.5416.6250.066.75250.033.33.5416.6250.066.75250.033.33.5416.7350.066.75250.033.33.5416.7350.066.7533.33.433.344.4350.066.75250.033.35.5458.331.1	(MH2)CPM Multiplication Factor4(M(M+z)Bus Multiplication Factor5(M(M50.066.766.0300.0400.044.00533.33.3100.050.066.766.0300.0400.04.50.059.93.0100.050.066.766.0300.0400.05.50.0500.066.63.00.0100.050.066.766.0300.0400.05.50.0550.073.33.0100.050.066.766.0300.0400.03.5.5550.073.33.0100.050.066.766.0300.0400.03.5.5550.073.33.0100.050.066.766.0300.0400.03.5.5540.071.9.92.5.5120.050.066.766.0300.0400.03.5.5540.071.9.92.5.5120.050.066.766.760.030.040.0550.050.071.9.92.5.5120.050.066.766.760.030.040.0550.050.071.9.92.5.5120.050.066.776300.040.03.3.32.5.071.9.92.5.5120.050.066.7550.030.33.3.33.1.551.0.351.0.92.5.5120.050.066.7550.0250.033.33.4.550.0.366.6.62.2.5120.0 </td

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2} (continued)

¹ The "low" values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The "high" values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower range configurations.

- ³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.
- ⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

Mode ³		Clock Hz)	CPM Multiplication			(MHz)		Bus Division		Clock Hz)	
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Multiplication Factor ⁵	Low	High	Factor	Low	High
			Defau	ult Mod	es (MO	DCK_H=0000)					
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
	1	1	F	-ull Cor	nfigurati	on Modes	1				1
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000						Reserved					
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000						Reserved					
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2}



Mode ³		Clock Hz)	CPM Clock CPM (MHz) Multiplication		CPU Multiplication	CPU Clock (MHz)		Bus Division	Bus Clock (MHz)		
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor	Low	High
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
	1	1	L	1	1		1	1			1
1100_000		Reserved									
1100_001		Reserved									
1100_010		Reserved									

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2} (continued)

¹ The "low" values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The "high" values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

⁴ CPM multiplication factor = CPM clock/bus clock

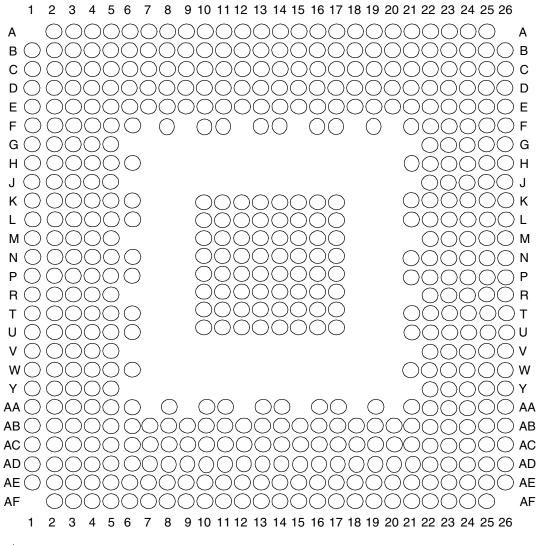
⁵ CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.



This figure shows the pinout of the 516 PBGA package as viewed from the top surface.



Not to Scale

Figure 12. Pinout of the 516 PBGA Package (View from Top)

This table lists the pins of the MPC8272. Note that the pins in the "MPC8272/8271 Only" column relate to Utopia functionality.

Table 2	21. P	inout
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Pin I			
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball	
Ē	BR		
BG/	BG/IRQ6		
ABB	C1		



Pinout

Table 21. Pinout (continued)						
Pin I						
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball				
D	D46					
D	D47					
D	AB1					
D	49	U4				
D	50	U1				
D	51	R3				
D	52	N3				
D	53	K2				
D	54	H5				
D	55	F4				
D	56	AA3				
D	57	U5				
D	U2					
D	P5					
D	М3					
D	K4					
D	62	НЗ				
D	63	E1				
IRQ3/CKSTP_	OUT/EXT_BR3	B16				
IRQ4/CORE_SF	RESET/EXT_BG3	C15				
IRQ5/TBEN/EX	KT_DBG3/CINT	Y4				
PSI	DVAL	C19				
ī	Ā	AA4				
TI	EA	AB6				
GBL	/IRQ1	D15				
CI/BADD	CI/BADDR29/IRQ2					
WT/BADD	0R30/IRQ3	C16				
BADDR31	/IRQ5/CINT	E17				
CPU_BR	/INT_OUT	B20				
C	SO	AE6				

Table 21. Pinout (continued)

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CS1

AD7



Table 21. Pinout	(continued)
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Pin N	Pin Name				
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball			
C	CS2				
C	53	AC8			
C	CS4				
C	55	AD8			
CS6/BC	TL1/SMI	AC9			
CS7/TL	BISYNC	AB9			
BADDR	27/IRQ1	AB8			
BADDR	28/IRQ2	AC7			
ALE/	IRQ4	AF4			
BC	TLO	AF3			
PWE0/PSDI	DQM0/PBS0	AD6			
PWE1/PSDI	DQM1/PBS1	AE5			
PWE2/PSDI	PWE2/PSDDQM2/PBS2				
PWE3/PSDI	PWE3/PSDDQM3/PBS3				
PWE4/PSDI	PWE4/PSDDQM4/PBS4				
PWE5/PSDI	DQM5/PBS5	AC5			
PWE6/PSDI	PWE6/PSDDQM6/PBS6				
PWE7/PSDI	PWE7/PSDDQM7/PBS7				
PSDA10)/PGPL0	AE2			
PSDWE	/PGPL1	AD3			
POE/PSDF	AS/PGPL2	AB4			
PSDCAS	5/PGPL3	AC3			
PGTA/PUPM	WAIT/PGPL4	AD2			
PSDAMU	X/PGPL5	AC2			
PCI_N	10DE ¹	AD22			
PCI_CFG0 (P	CI_HOST_EN)	AC21			
PCI_CFG1 (Ē	PCI_ARB_EN)	AE22			
PCI_CFG2 (D	DLL_ENABLE)	AE23			
PCI_	PAR	AF12			
PCI_F	RAME	AD15			
PCI_	TRDY	AF16			



Table 21. Pinout (continued)
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Pin Na		
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball
PCI_A	D16	AE16
PCI_A	D17	AF17
PCI_A	D18	AD16
PCI_A	D19	AC16
PCI_A	D20	AF18
PCI_A	D21	AB16
PCI_A	D22	AD17
PCI_A	D23	AF19
PCI_A	D24	AB17
PCI_A	D25	AF20
PCI_A	D26	AE19
PCI_A	D27	AC18
PCI_A	D28	AB18
PCI_A	D29	AD19
PCI_A	D30	AD21
PCI_A	D31	AC20
PCI_CC	ō/BE0	AE12
PCI_C1	/BE1	AF13
PCI_C2	2/BE2	AC15
PCI_C3	3/BE3	AE18
IRQ0/NM	II_OUT	A17
TRS	T ²	E21
TC	K	B22
ТМ	S	C23
TD	1	B24
TD	0	A22
TRI	S	B23
PORESET ²	/PCI_RST	C24
HRES	SET	D22
SRES	SET	F22
RSTC	ONF	A24



Pinout

Table 21. Pinout (continued)

Pin Na			
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball	
MODCK1/RSRV/	TC0/BNKSEL0	A20	
MODCK2/CSE0/	FC1/BNKSEL1	C20	
MODCK3/CSE1/	FC2/BNKSEL2	A21	
CLKI	N1	D21	
PA8/SMI	RXD2	AF25 ³	
PA9/SM	TXD2	AA22 ³	
PA10/MSNUM5	FCC1_UT_RXD0	AB23 ³	
PA11/MSNUM4	FCC1_UT_RXD1	AD26 ³	
PA12/MSNUM3	FCC1_UT_RXD2	AD25 ³	
PA13/MSNUM2	FCC1_UT_RXD3	AA24 ³	
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT_RXD4	W22 ³	
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT_RXD5	Y24 ³	
PA16/FCC1_MII_HDLC_RXD1	FCC1_UT_RXD6	T22 ³	
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RX D0	FCC1_UT_RXD7	W26 ³	
PA18/FCC1_MII_HDLC_TXD0/FCC1_MII _TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT_TXD7	V26 ³	
PA19/FCC1_MII_HDLC_TXD1/FCC1_RM II_TXD1	FCC1_UT_TXD6	R23 ³	
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT_TXD5	P25 ³	
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT_TXD4	N22 ³	
PA22	FCC1_UT_TXD3	N26 ³	
PA23	FCC1_UT_TXD2	N23 ³	
PA24/MSNUM1	FCC1_UT_TXD1	H26 ³	
PA25/MSNUM0	FCC1_UT_TXD0	G25 ³	
PA26/FCC1_MII_RMIIRX_ER	FCC1_UT_RXCLAV	L22 ³	
PA27/FCC1_MII_RX_DV/FCC1_RMII_CR S_DV	FCC1_UT_RXSOC	G24 ³	
PA28/FCC1_MII_RMII_TX_EN	FCC1_UT_RXENB	G23 ³	
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B26 ³	
PA30/FCC1_MII_CRS/FCC1_RTS	FCC1_UT_TXCLAV	A25 ³	



Package Description

9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

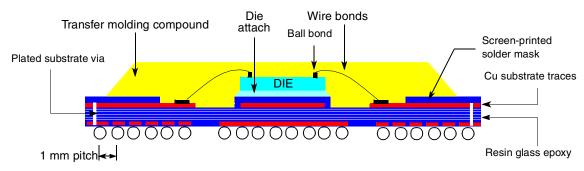


Figure 13. Side View of the PBGA Package Remove

9.1 Package Parameters

This table provides package parameters.

Table 22. Package Parameters

Code	Туре	Outline (mm)	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
VR, ZQ	PBGA	27 x 27	516	1	2.25

NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult "Freescale PowerQUICC II Pb-Free Packaging Information" (MPC8250PBFREEPKG) available on www.freescale.com.

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