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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8247zqtiea

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Overview

1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

			SoCs					
Functionality		MPC8272	MPC8248	MPC8271	MPC8247			
	Package ¹	516 PBGA						
Serial communications controllers (SC	Cs)	3	3	3	3			
QUICC multi-channel controller (QMC)		Yes	Yes	Yes	Yes			
Fast communication controllers (FCCs)	2	2	2	2				
I-Cache (Kbyte)		16	16	16	16			
D-Cache (Kbyte)		16	16	16	16			
Ethernet (10/100)		2	2	2	2			
UTOPIA II Ports		1	0	1	0			
Multi-channel controllers (MCCs)		0	0	0	0			
PCI bridge		Yes	Yes	Yes	Yes			
Transmission convergence (TC) layer				—				
Inverse multiplexing for ATM (IMA)	_	_		—				
Universal serial bus (USB) 2.0 full/low	1	1	1	1				
Security engine (SEC)	engine (SEC) Yes —							

Table 1. MPC8272 PowerQUICC II Family Functionality

¹ See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, "Ordering Information."

Code (Package)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
	MPC8272VR	MPC8272ZQ
Device	MPC8248VR	MPC8248ZQ
Device	MPC8271VR	MPC8271ZQ
	MPC8247VR	MPC8247ZQ

Table 2. MPC8272 PowerQUICC II Device Packages



Overview

- Floating-point unit (FPU) supports floating-point arithmetic
- Support for cache locking
- Low-power consumption
- Separate power supply for internal logic (1.5 V) and for I/O (3.3 V)
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
 - G2_LE core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 5.5:1, 6:1, 7:1, 8:1
 - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs—up to two external masters
 - Supports single transfers and burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
 - Programmable host bridge and agent
 - 32-bit data bus, 66 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE 1149.1 JTAG test access port
- Eight bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
 - Byte write enables
 - 32-bit address decodes with programmable bank size
 - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
 - Byte selects for 64-bit bus width (60x)
 - Dedicated interface logic for SDRAM
- Disable CPU mode





- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
 - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
 - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
 - Microcode tracing capabilities
 - Eight CPM trap registers
- Universal serial bus (USB) controller
 - Supports USB 2.0 full/low rate compatible
 - USB host mode
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loopback mode for diagnostics (12 Mbps only)
 - Supports USB slave mode
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate
 - Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Two fast communication controllers (FCCs) supporting the following protocols:
 - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
 - Transparent
 - HDLC—up to T3 rates (clear channel)



- PCI bridge
 - PCI Specification revision 2.2-compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI to 60x memory and 60x memory to PCI streaming
 - PCI host bridge or peripheral capabilities
 - Includes four DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - PCI-to-60x to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI
 - Includes the configuration registers required by the PCI standard (which are automatically loaded from the EPROM to configure the MPC8272) and message and doorbell registers
 - Supports the I_2O standard
 - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
 - Support for 66 MHz, 3.3 V specification
 - 60x-PCI bus core logic, which uses a buffer pool to allocate buffers for each port

2 **Operating Conditions**

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	-0.3 - 2.25	V
PLL supply voltage ²	VCCSYN	-0.3 - 2.25	V
I/O supply voltage ³	VDDH	-0.3 - 4.0	V
Input voltage ⁴	VIN	GND(-0.3) - 3.6	V
Junction temperature	Тj	120	°C
Storage temperature range	T _{STG}	(–55) – (+150)	°C

¹ Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

- ² Caution: VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.
- ³ Caution: VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.
- ⁴ Caution: VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.



Operating Conditions

I/O supply voltage

Junction temperature (maximum)

Input voltage

1

This table lists recommended operational voltage conditions.

•	•	
Rating	Symbol	Value
Core supply voltage	VDD	1.425 – 575
PLL supply voltage	VCCSYN	1.425 – 575

VDDH

VIN

Τi

Table 4. Recommended Operating Conditions¹

 Ambient temperature
 T_A
 0-70²
 °C

 Caution: These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.
 State
 State

² Note that for extended temperature parts the range is $(-40)_{T_A} - 105_{T_i}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.



Figure 2. Overshoot/Undershoot Voltage

Unit

V

V

V

V

°C

3.135 - 3.465

GND (-0.3) - 3.465

105²



3 DC Electrical Characteristics

This table shows DC electrical characteristics.

Table 5. DC Electrical Characteristics¹

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, TRST and PORESET ²	V _{IH}	2.0	3.465	V
Input low voltage ³	V _{IL}	GND	0.8	V
CLKIN input high voltage	V _{IHC}	2.4	3.465	V
CLKIN input low voltage	V _{ILC}	GND	0.4	V
Input leakage current, V _{IN} = VDDH ⁴	I _{IN}	—	10	μA
Hi-Z (off state) leakage current, V _{IN} = VDDH ²	I _{OZ}		10	μA
Signal low input current, V _{IL} = 0.8 V	١L	—	1	μA
Signal high input current, V _{IH} = 2.0 V	I _H	—	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except UTOPIA mode, and open drain pins In UTOPIA mode ⁵ (UTOPIA pins only): $I_{OH} = -8.0\text{mA}$ PA[8-31] PB[18-31] PC[0-1,4-29] PD[7-25, 29-31]	V _{OH}	2.4	_	V
In UTOPIA mode ⁵ (UTOPIA pins only): I _{OL} = 8.0mA PA[8–31] PB[18–31] PC[0–1,4–29] PD[7–25, 29–31]	V _{OL}	_	0.5	V



DC Electrical Characteristics

⁵ MPC8272 and MPC8271 only.

Table 6.

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, TRST and PORESET ¹	VIH	2.0	3.465	V
Input low voltage	V _{IL}	GND	0.8	V
CLKIN input high voltage	VIHC	2.4	3.465	V
CLKIN input low voltage	V _{ILC}	GND	0.4	V
Input leakage current, V _{IN} = VDDH ²	I _{IN}		10	μA
Hi-Z (off state) leakage current, V _{IN} = VDDH ²	I _{OZ}	_	10	μA
Signal low input current, V _{IL} = 0.8 V ³	١	_	1	μA
Signal high input current, V _{IH} = 2.0 V	Ι _Η	_	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except UTOPIA mode, and open drain pins In UTOPIA mode ⁴ (UTOPIA pins only): $I_{OH} = -8.0 \text{mA}$	V _{OH}	2.4	_	V
In UTOPIA mode ⁴ (UTOPIA pins only): I _{OL} = 8.0mA	V _{OL}	_	0.5	V
I _{OL} = 6.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0-3] AACK ARTRY DBG DBB/IRQ3 D[0-63] //EXT_BR3 //EXT_BR3 //EXT_BG3	V _{OL}		0.4	V



Thermal Characteristics

⁴ MPC8280, MPC8275VR, MPC8275ZQ only.

4 Thermal Characteristics

This table describes thermal characteristics. See Table 2 for information on a given SoC's package. Discussions of each characteristic are provided in Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance," through Section 4.7, "References." For the these discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

Characteristic	Symbol	Value	Unit	Air Flow
Junction-to-ambient—	P	27		Natural convection
single-layer board	R _{θJA}	21	°C/W	1 m/s
Junction-to-ambient—	R _{θJA} –	19		Natural convection
four-layer board		16	°C/W	1 m/s
Junction-to-board ²	$R_{ extsf{ heta}JB}$	11	°C/W	—
Junction-to-case ³	$R_{ extsf{ heta}JC}$	8	°C/W	_
Junction-to-package top ⁴	$R_{ extsf{ heta}JT}$	2	°C/W	—

Table 7. Thermal Characteristics

¹ Assumes no thermal vias

² Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

³ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁴ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_A = ambient temperature (°C)

 $R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_I - T_A$) are possible.



AC Electrical Characteristics

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100/133 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27 ²
Memory controller	45 or 27 ²
Parallel I/O	45
PCI	27

¹ These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.

² Impedance value is selected through SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

This table lists CPM output characteristics.

Spec N	Spec Number		Value (ns)							
Max Min	Characteristic	Maximum Delay				Minimum Delay				
		66 83 100 133 66 83 MHz MHz MHz MHz MHz MHz					100 MHz	133 MHz		
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	5.5	0.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	8	2	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	10	0	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	8	2	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	11	2.5	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	11	0.5	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	11	0.5	0.5	0.5	0.5

Table 10. AC Characteristics for CPM Outputs¹

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.





This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Spec N	lumber	nber		Value (ns)								
Setup Hold	Characteristic		Setup H					Characteristic Setup H		Но	old	
		66 83 100 133 66 8 MHz MLZ MLZ				83 MHz	100 MHz	133 MHz				
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0		
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2.5	2	2	2	2		
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0		
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	4	2	2	2	2		
sp20	sp21	TDM inputs/SI	3	3	3	3	2.5	2.5	2.5	2.5		
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	8	0.5	0.5	0.5	0.5		

Table 11. AC Characteristics for CPM Inputs¹

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.



Figure 3. FCC Internal Clock Diagram

Mode ³	Bus ((M	Clock Hz)	CPM Multiplication	CPM (M	Clock Hz)	CPU Clock CPU (MHz) Multiplication		PCI Division	PCI Clock (MHz)		
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor ⁶	Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0000_011	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0000_100	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0000_101	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_110	50.0	66.7	3.5	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0000_111	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
Full Configuration Modes											
0001_000	50.0	66.7	3	150.0	200.0	5	250.0	333.3	3	50.0	66.7
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
0100_000						Reserved					

 Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)^{1,2}



Mode ³	Bus (M	Clock Hz)	CPM Multiplication	CPM (M	Clock Hz)	CPU	CPU (M	Clock Hz)	PCI	PCI ((M	Clock Hz)
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor ⁶	Low	High
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0101_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0101_010	50.0	66.7	2	100.0	133.3	3.5	175.0	233.3	2	50.0	66.7
0101_011	50.0	66.7	2	100.0	133.3	4	200.0	266.6	2	50.0	66.7
0101_100	50.0	66.7	2	100.0	133.3	4.5	225.0	300.0	2	50.0	66.7
0101_101	83.3	111.1	3	250.0	333.3	3.5	291.7	388.9	5	50.0	66.7
0101_110	83.3	111.1	3	250.0	333.3	4	333.3	444.4	5	50.0	66.7
0101_111	83.3	111.1	3	250.0	333.3	4.5	375.0	500.0	5	50.0	66.7
0110_000	60.0	80.0	2.5	150.0	200.0	2.5	150.0	200.0	3	50.0	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0110_011	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7
0111_000						Reserved					
0111_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0111_010	50.0	66.7	3	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0111_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0111_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
1000_000						Reserved					
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7

Table 17. CIUCK CUTHIQUIATIONS IN FOURIST MODE (FOURIODORED) (CUTHINGED)	Table 17. Clo	ock Configuration	s for PCI Host Mod	e (PCI MODCK=0) ^{1,2} (continued)
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Mode ³	Bus ((MI	Clock Hz)	CPM Multiplication	CPM Clock (MHz) CPU Multiplication		CPU Clock (MHz)		PCI	PCI Clock (MHz)		
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	w High	Low	High	Factor ⁶	Low	High	
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000						Reserved					
1100_001						Reserved					
1100_010						Reserved					

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

¹ The "low" values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The "high" values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor



Mode ³	PCI ((MI	Clock Hz)	CPM Multiplication	CPM Clock CPM (MHz) C Multiplication Multiplication		CPU Clock CPU (MHz)		Bus Division -	Bus Clock (MHz)		
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor	Low	High
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7
1110_011	50.0	66.7	5	250.0	333.3	4	500.0	666.6	2	125.0	166.7
1110_100	50.0	66.7	5	250.0	333.3	4	333.3	444.4	3	83.3	111.1
1110_101	50.0	66.7	5	250.0	333.3	4.5	375.0	500.0	3	83.3	111.1
1110_110	50.0	66.7	5	250.0	333.3	5	416.7	555.5	3	83.3	111.1
1110_111	50.0	66.7	5	250.0	333.3	5.5	458.3	611.1	3	83.3	111.1
				•	•						
1100_000						Reserved					
1100_001						Reserved					
1100_010						Reserved					

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2} (continued)

¹ The "low" values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The "high" values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower range configurations.

- ³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.
- ⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor



Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	PCI ((MI	Clock Hz)	CPM Multiplication	CPM (M	Clock Hz)	CPU Multiplication	CPU (M	Clock Hz)	Bus	Bus ((M	Clock Hz)
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor	Low	High
1001_010						Reserved					
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000						Reserved					
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1011_101	25.0	50.0	8	200.0	400.0	2.5	250.0	500.0	2	100.0	200.0
1011_110	25.0	50.0	8	200.0	400.0	3	300.0	600.0	2	100.0	200.0
1011_111	25.0	50.0	8	200.0	400.0	3.5	350.0	700.0	2	100.0	200.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0



Pin N				
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball		
A	30	B15		
A	A15			
T	ГО	B3		
T.	Г1	E8		
T.	Г2	D7		
T.	ГЗ	C4		
T.	Г4	E7		
TB	ST	E3		
TS	IZO	E4		
TS	IZ1	E5		
TS	IZ2	C3		
TS	IZ3	D5		
ĀĀ	D3			
AR	C2			
DBG/	F16			
DBB/	D18			
D	0	AC1		
D	1	AA1		
D	2	V3		
D	3	R5		
D	4	P4		
D	5	M4		
D	6	J4		
D	7	G1		
D	8	W6		
D	9	Y3		
D	10	V1		
D	11	N6		
D	12	P3		
D	13	M2		
D	J5			

Table 21. Pinout (continued)



Pin N		
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball
D1	5	G3
D1	6	AB3
D1	7	Y1
D1	8	T4
D1	9	Т3
D2	20	P2
D2	21	M1
D2	22	J1
D2	23	G4
D2	24	AB2
D2	W4	
D2	V2	
D2	27	T1
D2	28	N5
D2	29	L1
D3	30	H1
D3	31	G5
D3	32	W5
D3	33	W2
D3	34	Т5
D3	35	Τ2
D3	36	N1
D3	37	КЗ
D3	38	H2
D3	39	F1
D4	0	AA2
D4	1	W1
D4	2	U3
D4	13	R2
D4		N2
D4	L2	

Table 21. Pinout (continued)



Pinout

Pin N	ame	
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball
D4	.6	H4
D4	F2	
D4	AB1	
D4	U4	
D5	50	U1
D5	1	R3
D5	2	N3
D5	3	К2
D5	54	H5
D5	5	F4
D5	AA3	
D5	U5	
D5	U2	
D5	P5	
De	М3	
De	1	К4
De	2	H3
De	3	E1
IRQ3/CKSTP_0	DUT/EXT_BR3	B16
IRQ4/CORE_SRI	ESET/EXT_BG3	C15
IRQ5/TBEN/EX	T_DBG3/CINT	Y4
PSD	VAL	C19
TA	Ā	AA4
TE	Ā	AB6
GBL/I	RQ1	D15
	D16	
WT/BADD	C16	
BADDR31/Ī	RQ5/CINT	E17
	NT_OUT	B20
<u>CS</u>	AE6	

Table 21. Pinout (continued)

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Table 21. Pinout (continued)
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Pin N					
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball			
PCI	AD16	AE16			
PCI	AD17	AF17			
PCI	AD18	AD16			
PCI	AC16				
PCI_/	PCI_AD20				
PCI_/	AD21	AB16			
PCI_/	AD22	AD17			
PCI_/	AD23	AF19			
PCI_/	AD24	AB17			
PCI_/	AD25	AF20			
PCI_/	AD26	AE19			
PCI_/	AD27	AC18			
PCI_/	AB18				
PCI_/	AD29	AD19			
PCI_/	AD30	AD21			
PCI_/	AD31	AC20			
PCI_C	0/BE0	AE12			
PCI_C	1/BE1	AF13			
PCI_C	2/BE2	AC15			
PCI_C	3/BE3	AE18			
IRQ0/NI	MI_OUT	A17			
TR	ST ²	E21			
тс	СК	B22			
ТМ	1S	C23			
Т	וכ	B24			
тс	00	A22			
₹T	IIS	B23			
PORESET	² /PCI_RST	C24			
HRE	SET	D22			
SRE	SET	F22			
RSTC	CONF	A24			



Revision	Date	Substantive Changes
1.2	09/2005	 Added 133-MHz to the list of frequencies in the opening sentence of Section 6, "AC Electrical Characteristics". Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13. Added footnote 2 to Table 13. Added the conditions note directly above Table 12.
1.1	01/2005	 Modification for correct display of assertion level ("overbar") for some signals
1.0	12/2004	 Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values Section 2: removed voltage tracking note Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed. Section 4.6: Updated description of layout practices Table 8: Note 3 added regarding IIC compatibility Table 8: Note 3 added regarding IIC compatibility Table 8: Note 3 added regarding IIC compatibility Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance Section 6: Added sentence providing derating factor Section 6: Added Note: Rise/Fall Time on CPM Input Pins Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22 Section 6.2: added pread spectrum clocking note Section 7: unit of ns added to Tval notes Section 7: unit of ns added to Tval notes Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz. Table 21: correct superscript of footnote number after pin AD22 Table 21: remove DONE3 from PC12 Table 21: signals referring to TDMs C2 and D2 removed