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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8247zqtmfa

- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
 - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
 - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
 - Microcode tracing capabilities
 - Eight CPM trap registers
- Universal serial bus (USB) controller
 - Supports USB 2.0 full/low rate compatible
 - USB host mode
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loopback mode for diagnostics (12 Mbps only)
 - Supports USB slave mode
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate
 - Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Two fast communication controllers (FCCs) supporting the following protocols:
 - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
 - Transparent
 - HDLC—up to T3 rates (clear channel)

- One of the FCCs supports ATM (MPC8272 and MPC8271 only)—full-duplex SAR at 155 Mbps, 8-bit UTOPIA interface 31 Mphys, AAL5, AAL1, AAL2, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64-K external connections
- Three serial communications controllers (SCCs) identical to those on the MPC860 supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BiSync) communications
 - Transparent
- QUICC multichannel controller (QMC) up to 64 channels
 - Independent transmit and receive routing, frame synchronization.
 - Serial-multiplexed (full-duplex) input/output 2048, 1544, and 1536 Kbps PCM highways
 - Compatible with T1/DS1 24-channel and CEPT E1 32-channel PCM highway, ISDN basic rate, ISDN primary rate, and user defined.
 - Subchanneling on each time slot.
 - Independent transmit and receive routing, frame synchronization and clocking
 - Concatenation of any not necessarily consecutive time slots to channels independently for receiver/transmitter
 - Supports H1, H11, and H12 channels
 - Allows dynamic allocation of channels
- SCC3 in NMSI mode is not usable when USB is enabled.
- Two serial management controllers (SMCs), identical to those of the MPC860
 - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
 - Transparent
 - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One I²C controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes
- Up to two TDM interfaces
 - Supports one groups of two TDM channels
 - 1024 bytes of SI RAM
- Eight independent baud rate generators and 14 input clock pins for supplying clocks to FCC, SCC, SMC, and USB serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

3 DC Electrical Characteristics

This table shows DC electrical characteristics.

Table 5. DC Electrical Characteristics¹

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ ²	V_{IH}	2.0	3.465	V
Input low voltage ³	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}$ ⁴	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}$ ²	I_{OZ}	—	10	μA
Signal low input current, $V_{IL} = 0.8 \text{ V}$	I_L	—	1	μA
Signal high input current, $V_{IH} = 2.0 \text{ V}$	I_H	—	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except UTOPIA mode, and open drain pins In UTOPIA mode ⁵ (UTOPIA pins only): $I_{OH} = -8.0 \text{ mA}$ PA[8–31] PB[18–31] PC[0–1,4–29] PD[7–25, 29–31]	V_{OH}	2.4	—	V
In UTOPIA mode ⁵ (UTOPIA pins only): $I_{OL} = 8.0 \text{ mA}$ PA[8–31] PB[18–31] PC[0–1,4–29] PD[7–25, 29–31]	V_{OL}	—	0.5	V

⁴ MPC8280, MPC8275VR, MPC8275ZQ only.

4 Thermal Characteristics

This table describes thermal characteristics. See [Table 2](#) for information on a given SoC's package. Discussions of each characteristic are provided in [Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance,"](#) through [Section 4.7, "References."](#) For the these discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

Table 7. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Air Flow
Junction-to-ambient—single-layer board ¹	$R_{\theta JA}$	27	°C/W	Natural convection
		21		1 m/s
Junction-to-ambient—four-layer board	$R_{\theta JA}$	19	°C/W	Natural convection
		16		1 m/s
Junction-to-board ²	$R_{\theta JB}$	11	°C/W	—
Junction-to-case ³	$R_{\theta JC}$	8	°C/W	—
Junction-to-package top ⁴	$R_{\theta JT}$	2	°C/W	—

¹ Assumes no thermal vias

² Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

³ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁴ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

4.7 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see [Section 7, “Clock Configuration Modes.”](#)

Table 8. Estimated Power Dissipation for Various Configurations¹

Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	$P_{INT}(W)^{2,3}$	
					Vddl 1.5 Volts	
					Nominal	Maximum
66.67	3	200	4	266	1	1.2
100	2	200	3	300	1.1	1.3
100	2	200	4	400	1.3	1.5
133	2	267	3	400	1.5	1.8

¹ Test temperature = 105° C

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

³ Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:

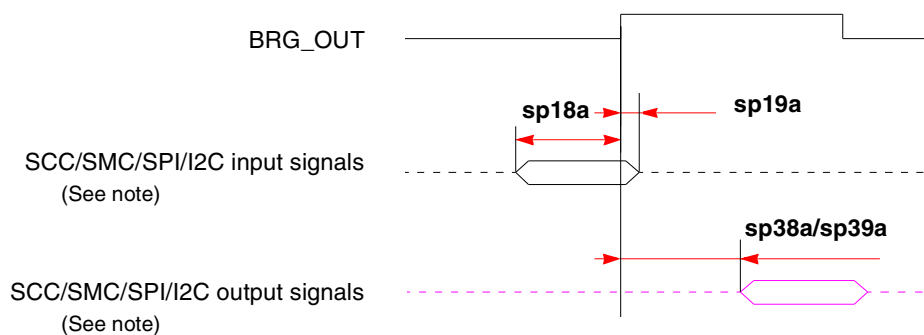
66.7 MHz = 0.35 W (nominal), 0.4 W (maximum)

83.3 MHz = 0.4 W (nominal), 0.5 W (maximum)

100 MHz = 0.5 W (nominal), 0.6 W (maximum)

133 MHz = 0.7 W (nominal), 0.8 W (maximum)

This figure shows the SCC/SMC/SPI/I²C internal clock.

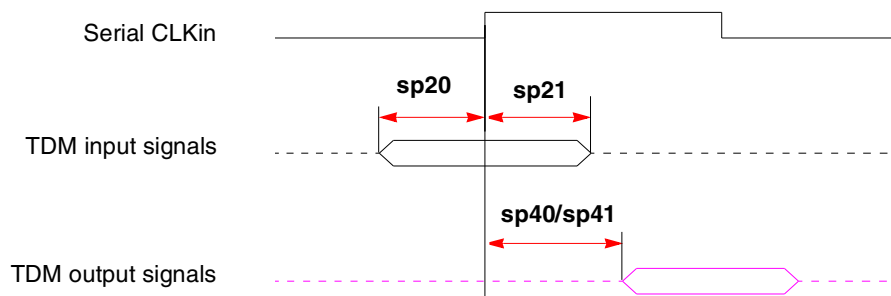


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

Table 12. AC Characteristics for SIU Inputs¹

Spec Number		Characteristic	Value (ns)							
Setup	Hold		Setup				Hold			
			66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp11	sp10	AACK/TA/TS/DBG/BG/BR/ARTRY/TEA	6	5	3.5	N/A	0.5	0.5	0.5	N/A
sp12	sp10	Data bus in normal mode	5	4	3.5	N/A	0.5	0.5	0.5	N/A
sp13	sp10	Data bus in pipeline mode (without ECC and PARITY)	N/A	4	2.5	1.5	N/A	0.5	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	N/A	0.5	0.5	0.5	N/A

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 13. AC Characteristics for SIU Outputs¹

Spec Number		Characteristic	Value (ns)							
Max	Min		Maximum Delay				Minimum Delay			
			66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp31	sp30	PSDVAL/TEA/TA	7	6	5.5	N/A	1	1	1	N/A
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	4.5 ²	1	1	1	1 ²
sp33	sp30	Data bus ³	6.5	6.5	5.5	4.5	0.8	0.8	0.8	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	4.5	1	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	N/A	1	1	1	N/A

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

² Value is for ADD only; other sp32/sp30 signals are not applicable.

³ To achieve 1 ns of hold time at 66.67/83.33/100 MHz, a minimum loading of 20 pF is required.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLK_{in}'s rising edge.

6.3 JTAG Timings

This table lists the JTAG timings.

Table 15. JTAG Timings¹

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t _{JTGR} and t _{JTGF}	0	5	ns	⁶
TRST assert time	t _{TRST}	25	—	ns	^{3, 6}
Input setup times	Boundary-scan data	t _{JTDVKH}	4	ns	^{4, 7}
	TMS, TDI	t _{JTIVKH}	4	ns	^{4, 7}
Input hold times	Boundary-scan data	t _{JTDXKH}	10	ns	^{4, 7}
	TMS, TDI	t _{JTIXKH}	10	ns	^{4, 7}
Output valid times	Boundary-scan data	t _{JTKLDV}	—	ns	^{5, 7}
	TDO	t _{JTKLOV}	10	ns	^{5, 7}
Output hold times	Boundary-scan data	t _{JTKLDX}	1	ns	^{5, 7}
	TDO	t _{JTKLOX}	1	ns	^{5, 7}
JTAG external clock to output high impedance	Boundary-scan data	t _{JTKLDZ}	1	ns	^{5, 6}
	TDO	t _{JTKLOZ}	1	ns	^{5, 6}

¹ All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

² The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

³ TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

⁴ Non-JTAG signal input timing with respect to t_{TCLK}.

⁵ Non-JTAG signal output timing with respect to t_{TCLK}.

⁶ Guaranteed by design.

⁷ Guaranteed by design and device characterization.

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)^{1,2} (continued)

Mode ³	Bus Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		PCI Division Factor ⁶	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
1000_010	66.7	88.9	3	200.0	266.6	3.5	233.3	311.1	4	50.0	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200.0	266.6	3.5	200.0	266.6	4	50.0	66.7
1001_011	57.1	76.2	3.5	200.0	266.6	4	228.6	304.7	4	50.0	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1010_101	100.0	133.3	2	200.0	266.6	2.5	250.0	333.3	4	50.0	66.7
1010_110	100.0	133.3	2	200.0	266.6	3	300.0	400.0	4	50.0	66.7
1010_111	100.0	133.3	2	200.0	266.6	3.5	350.0	466.6	4	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2}

Mode ³	Bus Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		PCI Division Factor ⁶	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0000_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0000_010	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0000_011	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0000_100	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0000_101	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0000_110	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0000_111	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
Full Configuration Modes											
0001_000	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
0001_001	50.0	100.0	3	150.0	300.0	6	300.0	600.0	6	25.0	50.0
0001_010	50.0	100.0	3	150.0	300.0	7	350.0	700.0	6	25.0	50.0
0001_011	50.0	100.0	3	150.0	300.0	8	400.0	800.0	6	25.0	50.0
0010_000	50.0	100.0	4	200.0	400.0	5	250.0	500.0	8	25.0	50.0
0010_001	50.0	100.0	4	200.0	400.0	6	300.0	600.0	8	25.0	50.0
0010_010	50.0	100.0	4	200.0	400.0	7	350.0	700.0	8	25.0	50.0
0010_011	50.0	100.0	4	200.0	400.0	8	400.0	800.0	8	25.0	50.0
0010_100	37.5	75.0	4	150.0	300.0	5	187.5	375.0	6	25.0	50.0
0010_101	37.5	75.0	4	150.0	300.0	5.5	206.3	412.5	6	25.0	50.0
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	Bus Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		PCI Division Factor ⁶	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	Bus Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		PCI Division Factor ⁶	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

¹ The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See [Table 17](#) for higher range configurations.

³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

- ⁶ CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
- PCIDF = 3 > CPM_CLK/PCI_CLK = 4
 - PCIDF = 5 > CPM_CLK/PCI_CLK = 6
 - PCIDF = 7 > CPM_CLK/PCI_CLK = 8
 - PCIDF = 9 > CPM_CLK/PCI_CLK = 5
 - PCIDF = B > CPM_CLK/PCI_CLK = 6

7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2}

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0000_110	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
Full Configuration Modes											
0001_001	60.0	66.7	2	120.0	133.3	5	150.0	166.7	4	30.0	33.3
0001_010	50.0	66.7	2	100.0	133.3	6	150.0	200.0	4	25.0	33.3
0001_011	50.0	66.7	2	100.0	133.3	7	175.0	233.3	4	25.0	33.3
0001_100	50.0	66.7	2	100.0	133.3	8	200.0	266.6	4	25.0	33.3
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0010_011	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2} (continued)

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0011_000	Reserved										
0011_001	Reserved										
0011_010	Reserved										
0011_011	Reserved										
0011_100	Reserved										
0100_000	Reserved										
0100_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0100_010	50.0	66.7	3	150.0	200.0	3.5	175.0	200.0	3	50.0	66.7
0100_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0100_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
0101_000	50.0	66.7	5	250.0	333.3	2.5	250.0	333.3	2.5	100.0	133.3
0101_001	50.0	66.7	5	250.0	333.3	3	300.0	400.0	2.5	100.0	133.3
0101_010	50.0	66.7	5	250.0	333.3	3.5	350.0	466.6	2.5	100.0	133.3
0101_011	50.0	66.7	5	250.0	333.3	4	400.0	533.3	2.5	100.0	133.3
0101_100	50.0	66.7	5	250.0	333.3	4.5	450.0	599.9	2.5	100.0	133.3
0101_101	50.0	66.7	5	250.0	333.3	5	500.0	666.6	2.5	100.0	133.3
0101_110	50.0	66.7	5	250.0	333.3	5.5	550.0	733.3	2.5	100.0	133.3
0110_000	Reserved										
0110_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
0110_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0110_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
0110_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
0111_000	50.0	66.7	3	150.0	200.0	2	150.0	200.0	2	75.0	100.0
0111_001	50.0	66.7	3	150.0	200.0	2.5	187.5	250.0	2	75.0	100.0
0111_010	50.0	66.7	3	150.0	200.0	3	225.0	300.0	2	75.0	100.0
0111_011	50.0	66.7	3	150.0	200.0	3.5	262.5	350.0	2	75.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2}

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
MODCK1/ $\overline{\text{RSRV}}$ /TC0/ $\overline{\text{BNKSEL0}}$		A20
MODCK2/CSE0/TC1/ $\overline{\text{BNKSEL1}}$		C20
MODCK3/CSE1/TC2/ $\overline{\text{BNKSEL2}}$		A21
CLKIN1		D21
PA8/SMRXD2		AF25 ³
PA9/SMTXD2		AA22 ³
PA10/MSNUM5	FCC1_UT_RXD0	AB23 ³
PA11/MSNUM4	FCC1_UT_RXD1	AD26 ³
PA12/MSNUM3	FCC1_UT_RXD2	AD25 ³
PA13/MSNUM2	FCC1_UT_RXD3	AA24 ³
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT_RXD4	W22 ³
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT_RXD5	Y24 ³
PA16/FCC1_MII_HDLC_RXD1	FCC1_UT_RXD6	T22 ³
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RX D0	FCC1_UT_RXD7	W26 ³
PA18/FCC1_MII_HDLC_TXD0/FCC1_MII _TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT_TXD7	V26 ³
PA19/FCC1_MII_HDLC_TXD1/FCC1_RM II_TXD1	FCC1_UT_TXD6	R23 ³
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT_TXD5	P25 ³
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT_TXD4	N22 ³
PA22	FCC1_UT_TXD3	N26 ³
PA23	FCC1_UT_TXD2	N23 ³
PA24/MSNUM1	FCC1_UT_TXD1	H26 ³
PA25/MSNUM0	FCC1_UT_TXD0	G25 ³
PA26/FCC1_MII_RMII_RX_ER	FCC1_UT_RXCLAV	L22 ³
PA27/FCC1_MII_RX_DV/FCC1_RMII_CR S_DV	FCC1_UT_RXSOC	G24 ³
PA28/FCC1_MII_RMII_TX_EN	FCC1_UT_RXENB	G23 ³
PA29/FCC1_MII_TX_ER	$\overline{\text{FCC1_UT_TXSOC}}$	B26 ³
PA30/FCC1_MII_CRS/ $\overline{\text{FCC1_RTS}}$	FCC1_UT_TXCLAV	A25 ³

9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

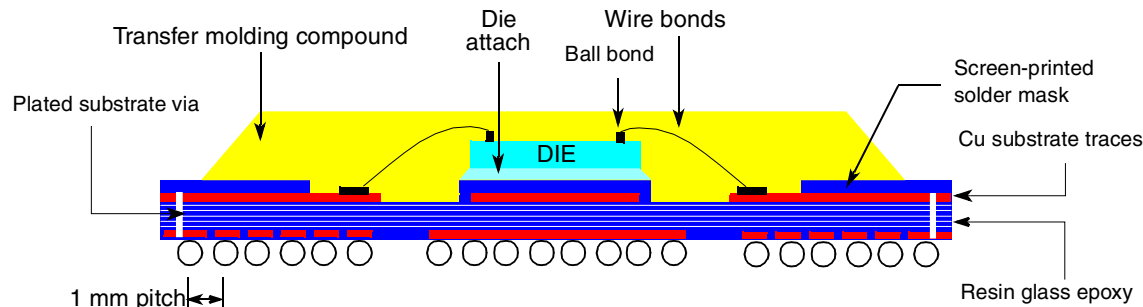


Figure 13. Side View of the PBGA Package Remove

9.1 Package Parameters

This table provides package parameters.

Table 22. Package Parameters

Code	Type	Outline (mm)	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
VR, ZQ	PBGA	27 x 27	516	1	2.25

NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
1.2	09/2005	<ul style="list-style-type: none"> Added 133-MHz to the list of frequencies in the opening sentence of Section 6, “AC Electrical Characteristics”. Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13. Added footnote 2 to Table 13. Added the conditions note directly above Table 12.
1.1	01/2005	<ul style="list-style-type: none"> Modification for correct display of assertion level (“overbar”) for some signals
1.0	12/2004	<ul style="list-style-type: none"> Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values Section 2: removed voltage tracking note Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed. Section 4.6: Updated description of layout practices Table 8: Note 3 added regarding IIC compatibility Table 8: Updated nominal and maximum power dissipation values Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance Section 6: Added sentence providing derating factor Section 6.1: added Note: Rise/Fall Time on CPM Input Pins Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22 Section 6.2: added spread spectrum clocking note Section 6.2: added CLKIN jitter note Table 12: combined specs sp11 and sp11a Table 13: sp30 Data Bus minimum delay values changed to 0.8 Section 7: unit of ns added to Tval notes Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. Section 7, “Clock Configuration Modes”: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. Table 21: correct superscript of footnote number after pin AD22 Table 21: remove DONE3 from PC12 Table 21: signals referring to TDMs C2 and D2 removed

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.2	12/2003	<ul style="list-style-type: none"> • Table 1: New • Table 2: New • Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V • Table 8: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see V_{IH} row of Table 8) • Table 8 and Table 21: Addition of muxed signals CPCI_HS_ES to $\overline{\text{PCI_REQ1}}$ (AF14) CPCI_HS_LED to $\overline{\text{PCI_GNT1}}$ (AE13) CPCI_HS_ENUM to $\overline{\text{PCI_GNT2}}$ (AF21) • Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices: $\overline{\text{PCI_CFG0}}$ ($\overline{\text{PCI_HOST_EN}}$) (AC21) $\overline{\text{PCI_CFG1}}$ ($\overline{\text{PCI_ARB_EN}}$) (AE22) $\overline{\text{PCI_CFG2}}$ ($\overline{\text{DLL_ENABLE}}$) (AE23) $\overline{\text{PCI_PAR}}$ (AF12) $\overline{\text{PCI_FRAME}}$ (AD15) $\overline{\text{PCI_TRDY}}$ (AF16) $\overline{\text{PCI_IRDY}}$ (AF15) $\overline{\text{PCI_STOP}}$ (AE15) $\overline{\text{DEVSEL}}$ (AE14) $\overline{\text{PCI_IDSEL}}$ (AC17) $\overline{\text{PCI_PERR}}$ (AD14) $\overline{\text{PCI_SERR}}$ (AD13) $\overline{\text{PCI_REQ0-2}}$ (AAE20, AF14, AB14) $\overline{\text{PCI_GNT0-2}}$ (AD20, AE13, AF21) $\overline{\text{PCI_RST}}$ (AF22) $\overline{\text{PCI_INTA}}$ (AE21) $\overline{\text{PCI_C0-3}}$ (AE12, AF13, AC15, AE18) $\overline{\text{PCI_AD0-31}}$ • Table 8 and Table 21: Corrected assertion level (added “$\overline{\text{~}}$”) $\overline{\text{PCI_HOST_EN}}$ (AC21) and $\overline{\text{PCI_ARB_EN}}$ (AE22) • Table 7: Addition of $R_{\theta JT}$ and note 4 • Sections 4.1–4.5 and 4.7 on thermal characteristics: New • Section 7, “Clock Configuration Modes”: Modification to first paragraph. Note that $\overline{\text{PCI_MODCK}}$ is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family. • Addition of “Note: Temperature Reflow for the VR Package” on page 56 • Table 21: Addition of note 2 to $\overline{\text{TRST}}$ (E21) and $\overline{\text{PORESET}}$ (C24) • Table 21: Removal of Thermal0 (D19) and Thermal1 (J3). These pins are now “No connects.” Note 4 unchanged. • Table 21: Removal of Spare0 (AD24). This pin is now a “No connect.” Note 5 unchanged. • Table 21: Addition of $\overline{\text{PCI_MODE}}$ (AD22). This pin was previously listed as “Ground.” Addition of note 1.
0.1	9/2003	<ul style="list-style-type: none"> • Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine) • Table 8: Addition of note 2 to V_{IH} • Table 8: Changed I_{OL} for 60x signals to 6.0 mA • Modification of note 1 for Table 17, Table 18, Table 19, and Table 20 • Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both $\overline{\text{CS5}}$ and GND. AD8 is only assigned to $\overline{\text{CS5}}$. • Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1 (J3) • Addition of ZQ package code to Figure 15
0	5/2003	NDA release