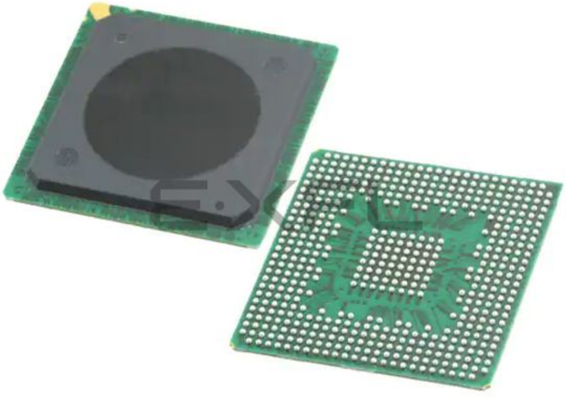


## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC G2_LE |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Communications; RISC CPM, Security; SEC |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8248czqtiea |

- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
  - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
  - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
  - Microcode tracing capabilities
  - Eight CPM trap registers
- Universal serial bus (USB) controller
  - Supports USB 2.0 full/low rate compatible
  - USB host mode
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
  - Supports USB slave mode
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Two fast communication controllers (FCCs) supporting the following protocols:
    - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—up to T3 rates (clear channel)

# 3 DC Electrical Characteristics

This table shows DC electrical characteristics.

**Table 5. DC Electrical Characteristics**[1]

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage[3] | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[4] | $I_{IN}$ | — | 10 | µA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | µA |
| Signal low input current, $V_{IL}$ = 0.8 V | $I_L$ | — | 1 | µA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | µA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[5] (UTOPIA pins only): $I_{OH}$ = -8.0mA<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31] | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[5] (UTOPIA pins only): $I_{OL}$ = 8.0mA<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31] | $V_{OL}$ | — | 0.5 | V |

### Table 5. DC Electrical Characteristics[1] (continued)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 5.3mA<br>CS[0–5]<br>CS6/BCTL1/SMI<br>CS7/TLBSYNC<br>BADDR27/ IRQ1<br>BADDR28/ IRQ2<br>ALE/ IRQ4<br>BCTL0<br>PWE[0–7]/PSDDQM[0–7]/PBS[0–7]<br>PSDA10/PGPL0<br>PSDWE/PGPL1<br>POE/PSDRAS/PGPL2<br>PSDCAS/PGPL3<br>PGTA/PUPMWAIT/PGPL4<br>PSDAMUX/PGPL5<br>PCI_CFG0 (PCI_HOST_EN)<br>PCI_CFG1 (PCI_ARB_EN)<br>PCI_CFG2 (DLL_ENABLE)<br>MODCK1/RSRV/TC(0)/BNKSEL(0)<br>MODCK2/CSE0/TC(1)/BNKSEL(1)<br>MODCK3CSE1/TC(2)/BNKSEL(2)<br>$I_{OL}$ = 3.2mA<br>PCI_PAR<br>PCI_FRAME<br>PCI_TRDY<br>PCI_IRDY<br>PCI_STOP<br>PCI_DEVSEL<br>PCI_IDSEL<br>PCI_PERR<br>PCI_SERR<br>PCI_REQ0<br>PCI_REQ1/ CPI_HS_ES<br>PCI_GNT0<br>PCI_GNT1/ CPI_HS_LES<br>PCI_GNT2/ CPI_HS_ENUM<br>PCI_RST<br>PCI_INTA<br>PCI_REQ2<br>DLLOUT<br>PCI_AD(0-31)<br>PCI_C(0–3)/BE(0-3)<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31]<br>TDO | $V_{OL}$ | — | 0.4 | V |

[1] The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

[2] TCK, TRST and PORESET have min VIH = 2.5V.

[3] $V_{IL}$ for IIC interface does not match IIC standard, but does meet IIC standard for $V_{OL}$ and should not cause any compatibility issue.

[4] The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

[5] MPC8272 and MPC8271 only.

**Table 6.**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[1] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[2] | $I_{IN}$ | — | 10 | µA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | µA |
| Signal low input current, $V_{IL}$ = 0.8 V[3] | $I_L$ | — | 1 | µA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | µA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[4] (UTOPIA pins only): $I_{OH}$ = -8.0mA | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[4] (UTOPIA pins only): $I_{OL}$ = 8.0mA | $V_{OL}$ | — | 0.5 | V |
| $I_{OL}$ = 6.0mA<br>$\overline{\text{BR}}$<br>$\overline{\text{BG}}$<br>$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$<br>$\overline{\text{TS}}$<br>A[0-31]<br>TT[0-4]<br>$\overline{\text{TBST}}$<br>TSIZE[0–3]<br>$\overline{\text{AACK}}$<br>$\overline{\text{ARTRY}}$<br>$\overline{\text{DBG}}$<br>$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$<br>D[0-63]<br>//$\overline{\text{EXT\_BR3}}$<br>//$\overline{\text{EXT\_BG3}}$<br>/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$/$\overline{\text{CINT}}$<br>$\overline{\text{PSDVAL}}$<br>$\overline{\text{TA}}$<br>$\overline{\text{TEA}}$<br>$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$<br>$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$<br>$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$<br>BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$<br>$\overline{\text{CPU\_BR}}$<br>$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$<br>/$\overline{\text{PCI\_RST}}$<br>$\overline{\text{HRESET}}$<br>$\overline{\text{SRESET}}$<br>$\overline{\text{RSTCONF}}$ | $V_{OL}$ | — | 0.4 | V |

# 6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100/133 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

**Table 9. Output Buffer Impedances[1]**

| Output Buffers | Typical Impedance (Ω) |
|---|---|
| 60x bus | 45 or 27[2] |
| Memory controller | 45 or 27[2] |
| Parallel I/O | 45 |
| PCI | 27 |

[1] These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.

[2] Impedance value is selected through SIUMCR[20,21]. See the SoC reference manual.

## 6.1 CPM AC Characteristics

This table lists CPM output characteristics.

**Table 10. AC Characteristics for CPM Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | | Minimum Delay | | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp36a | sp37a | FCC outputs—internal clock (NMSI) | 6 | 5.5 | 5.5 | 5.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| sp36b | sp37b | FCC outputs—external clock (NMSI) | 8 | 8 | 8 | 8 | 2 | 2 | 2 | 2 |
| sp38a | sp39a | SCC/SMC/SPI/I2C outputs—internal clock (NMSI) | 10 | 10 | 10 | 10 | 0 | 0 | 0 | 0 |
| sp38b | sp39b | SCC/SMC/SPI/I2C outputs—external clock (NMSI) | 8 | 8 | 8 | 8 | 2 | 2 | 2 | 2 |
| sp40 | sp41 | TDM outputs/SI | 11 | 11 | 11 | 11 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp42 | sp43 | TIMER/IDMA outputs | 11 | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 | 0.5 |
| sp42a | sp43a | PIO outputs | 11 | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 | 0.5 |

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure shows the FCC external clock.

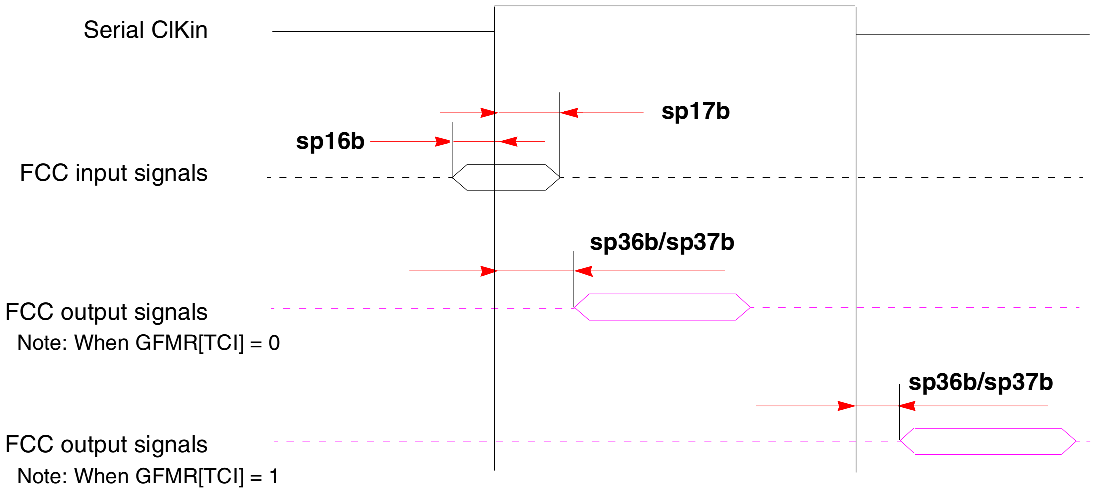
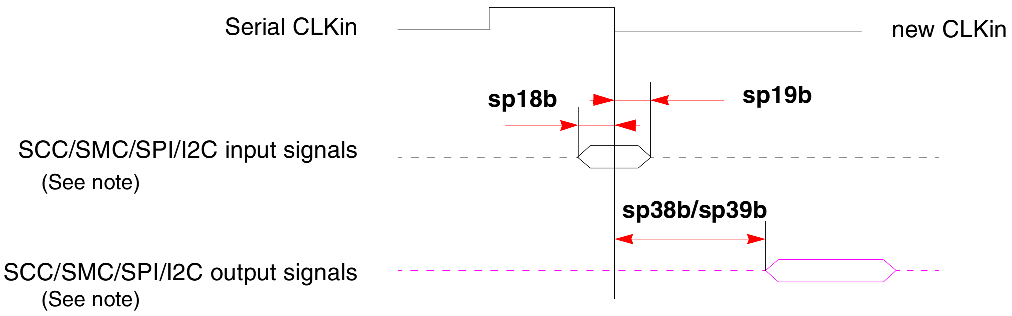


**Figure 4. FCC External Clock Diagram**

This figure shows the SCC/SMC/SPI/I$^2$C external clock.



**Note:** There are four possible timing conditions for SPI:

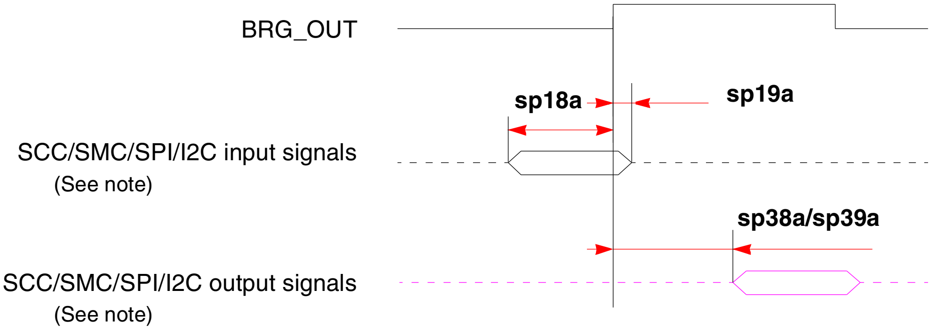
1. Input sampled on the rising edge and output driven on the rising edge.
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge (shown).
4. Input sampled on the falling edge and output driven on the rising edge.

**Note:** There are two possible timing conditions for SCC/SMC/I$^2$C:

1. Input sampled on the falling edge and output driven on the falling edge (shown).
2. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/I$^2$C External Clock Diagram**

This figure shows the SCC/SMC/SPI/I$^2$C internal clock.

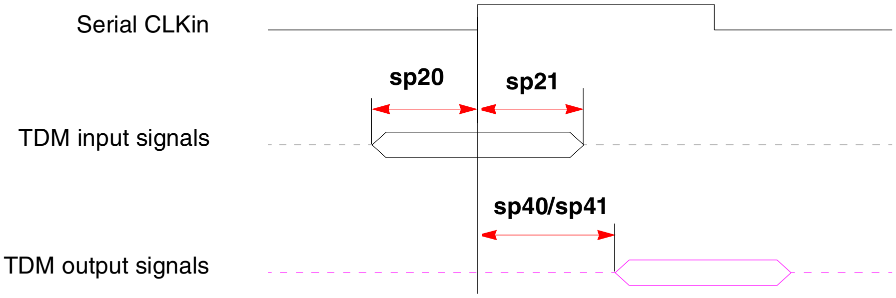


**Note:** There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I$^2$C Internal Clock Diagram**

This figure shows TDM input and output signals.



**Note:** There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

### Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 4 | 50.0 | 66.7 |
| 1000_011 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 4 | 50.0 | 66.7 |
| 1000_100 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 1000_101 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 6 | 400.0 | 533.3 | 4 | 50.0 | 66.7 |
| 1000_110 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 6.5 | 433.3 | 577.7 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 3.5 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_011 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 4 | 228.6 | 304.7 | 4 | 50.0 | 66.7 |
| 1001_100 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 4.5 | 257.1 | 342.8 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1001_101 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 5 | 428.6 | 571.4 | 6 | 50.0 | 66.7 |
| 1001_110 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 5.5 | 471.4 | 628.5 | 6 | 50.0 | 66.7 |
| 1001_111 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 6 | 514.3 | 685.6 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 1010_001 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 3 | 50.0 | 66.7 |
| 1010_010 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| 1010_011 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 3 | 50.0 | 66.7 |
| 1010_100 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 4 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 133.3 | 2 | 200.0 | 266.6 | 2.5 | 250.0 | 333.3 | 4 | 50.0 | 66.7 |
| 1010_110 | 100.0 | 133.3 | 2 | 200.0 | 266.6 | 3 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 1010_111 | 100.0 | 133.3 | 2 | 200.0 | 266.6 | 3.5 | 350.0 | 466.6 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1011_010 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 4 | 50.0 | 66.7 |
| 1011_011 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 4 | 50.0 | 66.7 |

### Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2]

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| Default Modes (MODCK_H=0000) | | | | | | | | | | | |
| 0000_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0000_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0000_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0000_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0000_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0000_101 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0000_110 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0000_111 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 0001_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 6 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0001_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 7 | 350.0 | 700.0 | 6 | 25.0 | 50.0 |
| 0001_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 8 | 400.0 | 800.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_000 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 0010_001 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 6 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 0010_010 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 7 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| 0010_011 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 8 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_100 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 0010_101 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5.5 | 206.3 | 412.5 | 6 | 25.0 | 50.0 |
| 0010_110 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 6 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0011_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 5 | 150.0 | 250.0 | 5 | 30.0 | 50.0 |
| 0011_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 6 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 0011_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 7 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 0011_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 8 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |

[6] CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

## 7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

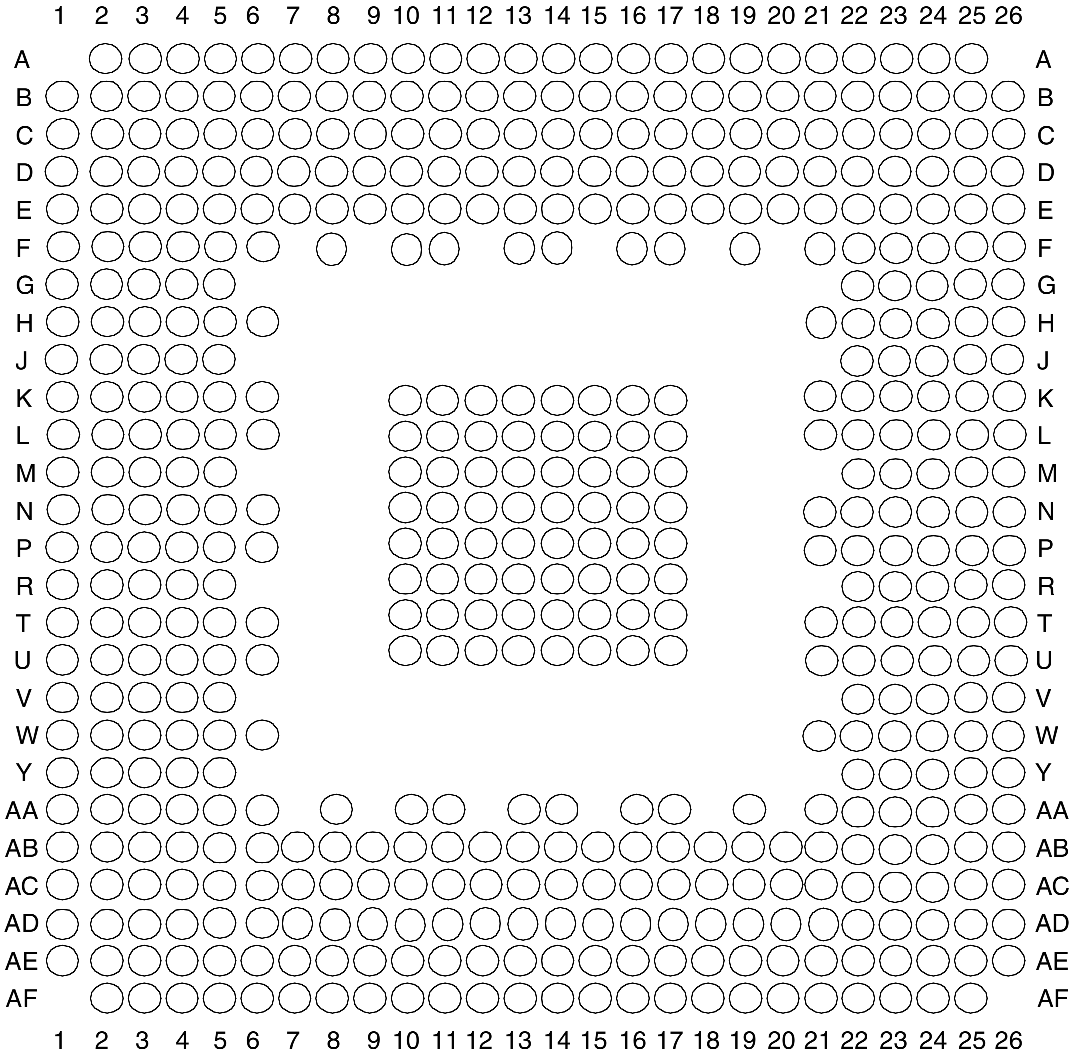
**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0000_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0000_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 5 | 150.0 | 166.7 | 4 | 30.0 | 33.3 |
| 0001_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 6 | 150.0 | 200.0 | 4 | 25.0 | 33.3 |
| 0001_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 7 | 175.0 | 233.3 | 4 | 25.0 | 33.3 |
| 0001_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 8 | 200.0 | 266.6 | 4 | 25.0 | 33.3 |
| | | | | | | | | | | | |
| 0010_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0010_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0010_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 0010_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 150.0 | 166.7 | 2.5 | 60.0 | 80.0 |
| 1000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 1000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 1000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 1000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 225.0 | 300.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 1010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 1010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 1010_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 2.5 | 80.0 | 106.7 |
| 1011_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| 1011_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 2.5 | 80.0 | 106.7 |
| 1011_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 2.5 | 80.0 | 106.7 |
| | | | | | | | | | | | |
| 1011_101 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 250.0 | 333.3 | 2 | 100.0 | 133.3 |
| 1011_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 300.0 | 400.0 | 2 | 100.0 | 133.3 |
| 1011_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 350.0 | 466.6 | 2 | 100.0 | 133.3 |
| | | | | | | | | | | | |

This figure shows the pinout of the 516 PBGA package as viewed from the top surface.



Not to Scale

**Figure 12. Pinout of the 516 PBGA Package (View from Top)**

This table lists the pins of the MPC8272. Note that the pins in the “MPC8272/8271 Only” column relate to Utopia functionality.

**Table 21. Pinout**

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| $\overline{\text{BR}}$ | | A19 |
| $\overline{\text{BG}}/\overline{\text{IRQ6}}$ | | D2 |
| $\overline{\text{ABB}}/\overline{\text{IRQ2}}$ | | C1 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| A30 | | B15 |
| A31 | | A15 |
| TT0 | | B3 |
| TT1 | | E8 |
| TT2 | | D7 |
| TT3 | | C4 |
| TT4 | | E7 |
| $\overline{\text{TBST}}$ | | E3 |
| TSIZ0 | | E4 |
| TSIZ1 | | E5 |
| TSIZ2 | | C3 |
| TSIZ3 | | D5 |
| $\overline{\text{AACK}}$ | | D3 |
| $\overline{\text{ARTRY}}$ | | C2 |
| $\overline{\text{DBG}}/\overline{\text{IRQ7}}$ | | F16 |
| $\overline{\text{DBB}}/\overline{\text{IRQ3}}$ | | D18 |
| D0 | | AC1 |
| D1 | | AA1 |
| D2 | | V3 |
| D3 | | R5 |
| D4 | | P4 |
| D5 | | M4 |
| D6 | | J4 |
| D7 | | G1 |
| D8 | | W6 |
| D9 | | Y3 |
| D10 | | V1 |
| D11 | | N6 |
| D12 | | P3 |
| D13 | | M2 |
| D14 | | J5 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| PCI_IRDY | | AF15 |
| PCI_STOP | | AE15 |
| PCI_DEVSEL | | AE14 |
| PCI_IDSEL | | AC17 |
| PCI_PERR | | AD14 |
| PCI_SERR | | AD13 |
| PCI_REQ0 | | AE20 |
| PCI_REQ1/CPCI_HS_ES | | AF14 |
| PCI_GNT0 | | AD20 |
| PCI_GNT1/CPCI_HS_LED | | AE13 |
| PCI_GNT2/CPCI_HS_ENUM | | AF21 |
| PCI_RST | | AF22 |
| PCI_INTA | | AE21 |
| PCI_REQ2 | | AB14 |
| DLLOUT | | AC22 |
| PCI_AD0 | | AF7 |
| PCI_AD1 | | AE10 |
| PCI_AD2 | | AB10 |
| PCI_AD3 | | AD10 |
| PCI_AD4 | | AE9 |
| PCI_AD5 | | AF8 |
| PCI_AD6 | | AC10 |
| PCI_AD7 | | AE11 |
| PCI_AD8 | | AB11 |
| PCI_AD9 | | AF10 |
| PCI_AD10 | | AF9 |
| PCI_AD11 | | AB12 |
| PCI_AD12 | | AC12 |
| PCI_AD13 | | AD12 |
| PCI_AD14 | | AF11 |
| PCI_AD15 | | AB13 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| PA31/FCC1_MII_COL | FCC1_UT_TXENB | G22[3] |
| PB18/FCC2_MII_HDLC_RXD3 | | T25[3] |
| PB19/FCC2_MII_HDLC_RXD2 | | P22[3] |
| PB20/FCC2_MII_HDLC_RMII_RXD1 | | L25[3] |
| PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD | | J26[3] |
| PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0 | | U23[3] |
| PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1 | | U26[3] |
| PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2 | | M24[3] |
| PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2 | | M23[3] |
| PB26/FCC2_MII_CRS/L1RXDB2 | | H24[3] |
| PB27/FCC2_MII_COL/L1TXDB2 | | E25[3] |
| PB28/FCC2_MII_RMII_RX_ER/FCC2_RTS/TXD1 | | D26[3] |
| PB29/FCC2_MII_RMII_TX_EN | | K21[3] |
| PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV | | D24[3] |
| PB31/FCC2_MII_TX_ER | | E23[3] |
| PC0/DREQ3/BRGO7/SMSYN1/L1CLKOA2 | | AF23[3] |
| PC1/BRGO6/L1RQA2 | | AD23[3] |
| PC4/SMRXD1/SI2_L1ST4/FCC2_CD | | AB22[3] |
| PC5/SMTXD1/SI2_L1ST3/FCC2_CTS | | AE24[3] |
| PC6/FCC1_CD/SI2_L1ST2 | FCC1_UT_RXADDR2 | AF24[3] |
| PC7/FCC1_CTS | FCC1_UT_TXADDR2 | AE26[3] |
| PC8/CD4/RTS1/SI2_L1ST2/CTS3 | | AC24[3] |
| PC9/CTS4/L1TSYNCA2 | | AA23[3] |
| PC10/CD3/USB_RN | | AB25[3] |
| PC11/CTS3/USB_RP/L1TXD3A2 | | V22[3] |
| PC12 | FCC1_UT_RXADDR1 | AA26[3] |
| PC13/BRGO5 | FCC1_UT_TXADDR1 | V23[3] |
| PC14/CD1 | FCC1_UT_RXADDR0 | W24[3] |
| PC15/CTS1 | FCC1_UT_TXADDR0 | U24[3] |
| PC16/CLK16 | | T23[3] |

# 9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

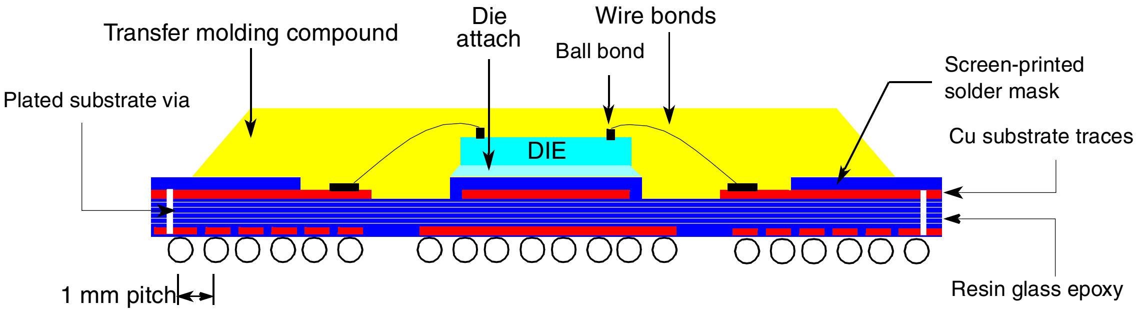


**Figure 13. Side View of the PBGA Package Remove**

## 9.1 Package Parameters

This table provides package parameters.

**Table 22. Package Parameters**

| Code | Type | Outline (mm) | Interconnects | Pitch (mm) | Nominal Unmounted Height (mm) |
|---|---|---|---|---|---|
| VR, ZQ | PBGA | 27 x 27 | 516 | 1 | 2.25 |

### NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

# 10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

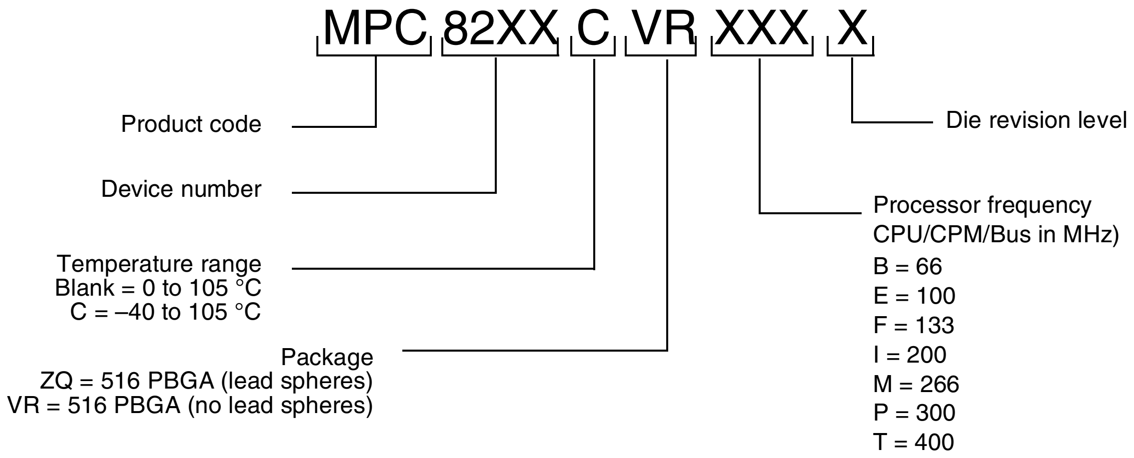


**Figure 15. Freescale Part Number Key**

# 11 Document Revision History

This table summarizes changes to this document.

**Table 23. Document Revision History**

| Revision | Date | Substantive Changes |
|---|---|---|
| 3 | 09/2011 | In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information. |
| 2 | 12/2008 | • Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes.<br>• In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.”<br>• In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency.<br>• Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.”<br>• Removed overbar from DLL_ENABLE in Table 21, “Pinout.” |
| 1.5 | 12/2006 | • Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions. |
| 1.4 | 05/2006 | • Added row for 133 MHz configurations to Table 8. |
| 1.3 | 02/2006 | • Inserted Section 6.3, “JTAG Timings.” |

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.2 | 09/2005 | • Added 133-MHz to the list of frequencies in the opening sentence of Section 6, “AC Electrical Characteristics”.<br>• Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13.<br>• Added footnote 2 to Table 13.<br>• Added the conditions note directly above Table 12. |
| 1.1 | 01/2005 | • Modification for correct display of assertion level (“overbar”) for some signals |
| 1.0 | 12/2004 | • Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values<br>• Section 2: removed voltage tracking note<br>• Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset<br>• Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V<br>• Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed.<br>• Section 4.6: Updated description of layout practices<br>• Table 8: Note 3 added regarding IIC compatibility<br>• Table 8: Updated nominal and maximum power dissipation values<br>• Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance<br>• Section 6: Added sentence providing derating factor<br>• Section 6.1: added Note: Rise/Fall Time on CPM Input Pins<br>• Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a<br>• Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22<br>• Section 6.2: added spread spectrum clocking note<br>• Section 6.2: added CLKIN jitter note<br>• Table 12: combined specs sp11 and sp11a<br>• Table 13: sp30 Data Bus minimum delay values changed to 0.8<br>• Section 7: unit of ns added to Tval notes<br>• Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Section 7, “Clock Configuration Modes”: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Table 21: correct superscript of footnote number after pin AD22<br>• Table 21: remove DONE3 from PC12<br>• Table 21: signals referring to TDMs C2 and D2 removed |

### Table 23. Document Revision History (continued)

| Revision | Date | Substantive Changes |
|---|---|---|
| 0.2 | 12/2003 | • Table 1: New<br>• Table 2: New<br>• Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V<br>• Table 8: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see $V_{IH}$ row of Table 8)<br>• Table 8 and Table 21: Addition of muxed signals<br>CPCI_HS_ES to $\overline{\text{PCI\_REQ1}}$ (AF14)<br>CPCI_HS_LED to $\overline{\text{PCI\_GNT1}}$ (AE13)<br>$\overline{\text{CPCI\_HS\_ENUM}}$ to $\overline{\text{PCI\_GNT2}}$ (AF21)<br>• Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices:<br>PCI_CFG0 ($\overline{\text{PCI\_HOST\_EN}}$) (AC21)<br>PCI_CFG1 ($\overline{\text{PCI\_ARB\_EN}}$) (AE22)<br>PCI_CFG2 (DLL_ENABLE) (AE23)<br>PCI_PAR (AF12)<br>$\overline{\text{PCI\_FRAME}}$ (AD15)<br>$\overline{\text{PCI\_TRDY}}$(AF16)<br>$\overline{\text{PCI\_IRDY}}$ (AF15)<br>$\overline{\text{PCI\_STOP}}$ (AE15)<br>$\overline{\text{DEVSEL}}$ (AE14)<br>PCI_IDSEL (AC17)<br>$\overline{\text{PCI\_PERR}}$ (AD14)<br>$\overline{\text{PCI\_SERR}}$ (AD13)<br>$\overline{\text{PCI\_REQ0–2}}$ (AAE20, AF14, AB14)<br>$\overline{\text{PCI\_GNT0–2}}$ (AD20, AE13, AF21)<br>$\overline{\text{PCI\_RST}}$ (AF22)<br>$\overline{\text{PCI\_INTA}}$ (AE21)<br>$\overline{\text{PCI\_C0-3}}$ (AE12, AF13, AC15, AE18)<br>PCI_AD0-31<br>• Table 8 and Table 21: Corrected assertion level (added “‾“) $\overline{\text{PCI\_HOST\_EN}}$ (AC21) and $\overline{\text{PCI\_ARB\_EN}}$ (AE22)<br>• Table 7: Addition of $R_{\theta JT}$ and note 4<br>• Sections 4.1–4.5 and 4.7 on thermal characteristics: New<br>• Section 7, “Clock Configuration Modes”: Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family.<br>• Addition of “Note: Temperature Reflow for the VR Package" on page 56<br>• Table 21: Addition of note 2 to $\overline{\text{TRST}}$ (E21) and $\overline{\text{PORESET}}$ (C24)<br>• Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now “No connects.” Note 4 unchanged.<br>• Table 21: Removal of Spare0 (AD24). This pin is now a “No connect.” Note 5 unchanged.<br>• Table 21: Addition of $\overline{\text{PCI\_MODE}}$ (AD22). This pin was previously listed as “Ground.” Addition of note 1. |
| 0.1 | 9/2003 | • Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine)<br>• Table 8: Addition of note 2 to $V_{IH}$<br>• Table 8: Changed $I_{OL}$ for 60x signals to 6.0 mA<br>• Modification of note 1 for Table 17, Table 18, Table 19, and Table 20<br>• Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both $\overline{\text{CS5}}$ and GND. AD8 is only assigned to $\overline{\text{CS5}}$.<br>• Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3)<br>• Addition of ZQ package code to Figure 15 |
| 0 | 5/2003 | NDA release |

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Tokyo 153-0064
Japan
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support.japan@freescale.com

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