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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC G2_LE |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Communications; RISC CPM, Security; SEC |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8248vrtmfa |

# 1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

**Table 1. MPC8272 PowerQUICC II Family Functionality**

| Functionality | SoCs | | | |
|---|---|---|---|---|
| | MPC8272 | MPC8248 | MPC8271 | MPC8247 |
| Package[1] | 516 PBGA | | | |
| Serial communications controllers (SCCs) | 3 | 3 | 3 | 3 |
| QUICC multi-channel controller (QMC) | Yes | Yes | Yes | Yes |
| Fast communication controllers (FCCs) | 2 | 2 | 2 | 2 |
| I-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| D-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| Ethernet (10/100) | 2 | 2 | 2 | 2 |
| UTOPIA II Ports | 1 | 0 | 1 | 0 |
| Multi-channel controllers (MCCs) | 0 | 0 | 0 | 0 |
| PCI bridge | Yes | Yes | Yes | Yes |
| Transmission convergence (TC) layer | — | — | — | — |
| Inverse multiplexing for ATM (IMA) | — | — | — | — |
| Universal serial bus (USB) 2.0 full/low rate | 1 | 1 | 1 | 1 |
| Security engine (SEC) | Yes | Yes | — | — |

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

**Table 2. MPC8272 PowerQUICC II Device Packages**

| Code (Package) | VR (516 PBGA—Lead free) | ZQ (516 PBGA—Lead spheres) |
|---|---|---|
| Device | MPC8272VR | MPC8272ZQ |
| | MPC8248VR | MPC8248ZQ |
| | MPC8271VR | MPC8271ZQ |
| | MPC8247VR | MPC8247ZQ |

5 MPC8272 and MPC8271 only.

**Table 6.**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, TRST and PORESET[1] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[2] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V[3] | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[4] (UTOPIA pins only): $I_{OH}$ = -8.0mA | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[4] (UTOPIA pins only): $I_{OL}$ = 8.0mA | $V_{OL}$ | — | 0.5 | V |
| $I_{OL}$ = 6.0mA<br>BR<br>BG<br>ABB/IRQ2<br>TS<br>A[0-31]<br>TT[0-4]<br>TBST<br>TSIZE[0–3]<br>AACK<br>ARTRY<br>DBG<br>DBB/IRQ3<br>D[0-63]<br>//EXT_BR3<br>//EXT_BG3<br>/TBEN/EXT_DBG3/CINT<br>PSDVAL<br>TA<br>TEA<br>GBL/IRQ1<br>CI/BADDR29/IRQ2<br>WT/BADDR30/IRQ3<br>BADDR31/IRQ5/CINT<br>CPU_BR<br>IRQ0/NMI_OUT<br>/PCI_RST<br>HRESET<br>SRESET<br>RSTCONF | $V_{OL}$ | — | 0.4 | V |

## 4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

## 4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

## 4.7 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

**Table 8. Estimated Power Dissipation for Various Configurations[1]**

| Bus (MHz) | CPM Multiplication Factor | CPM (MHz) | CPU Multiplication Factor | CPU (MHz) | $P_{INT}$(W)[2,3] | |
|---|---|---|---|---|---|---|
| | | | | | Vddl 1.5 Volts | |
| | | | | | Nominal | Maximum |
| 66.67 | 3 | 200 | 4 | 266 | 1 | 1.2 |
| 100 | 2 | 200 | 3 | 300 | 1.1 | 1.3 |
| 100 | 2 | 200 | 4 | 400 | 1.3 | 1.5 |
| 133 | 2 | 267 | 3 | 400 | 1.5 | 1.8 |

1 Test temperature = 105° C
2 $P_{INT} = I_{DD} \times V_{DD}$ Watts
3 Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.35 W (nominal), 0.4 W (maximum)
83.3 MHz = 0.4 W (nominal), 0.5 W (maximum)
100 MHz = 0.5 W (nominal), 0.6 W (maximum)
133 MHz = 0.7 W (nominal), 0.8 W (maximum)

# 6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100/133 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

**Table 9. Output Buffer Impedances[1]**

| Output Buffers | Typical Impedance (Ω) |
|---|---|
| 60x bus | 45 or 27[2] |
| Memory controller | 45 or 27[2] |
| Parallel I/O | 45 |
| PCI | 27 |

1 These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.
2 Impedance value is selected through SIUMCR[20,21]. See the SoC reference manual.

## 6.1 CPM AC Characteristics

This table lists CPM output characteristics.

**Table 10. AC Characteristics for CPM Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | | Minimum Delay | | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp36a | sp37a | FCC outputs—internal clock (NMSI) | 6 | 5.5 | 5.5 | 5.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| sp36b | sp37b | FCC outputs—external clock (NMSI) | 8 | 8 | 8 | 8 | 2 | 2 | 2 | 2 |
| sp38a | sp39a | SCC/SMC/SPI/I2C outputs—internal clock (NMSI) | 10 | 10 | 10 | 10 | 0 | 0 | 0 | 0 |
| sp38b | sp39b | SCC/SMC/SPI/I2C outputs—external clock (NMSI) | 8 | 8 | 8 | 8 | 2 | 2 | 2 | 2 |
| sp40 | sp41 | TDM outputs/SI | 11 | 11 | 11 | 11 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp42 | sp43 | TIMER/IDMA outputs | 11 | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 | 0.5 |
| sp42a | sp43a | PIO outputs | 11 | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 | 0.5 |

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 11. AC Characteristics for CPM Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 2.5 | 2.5 | 2.5 | 2.5 | 2 | 2 | 2 | 2 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 |
| sp20 | sp21 | TDM inputs/SI | 3 | 3 | 3 | 3 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 8 | 8 | 8 | 8 | 0.5 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

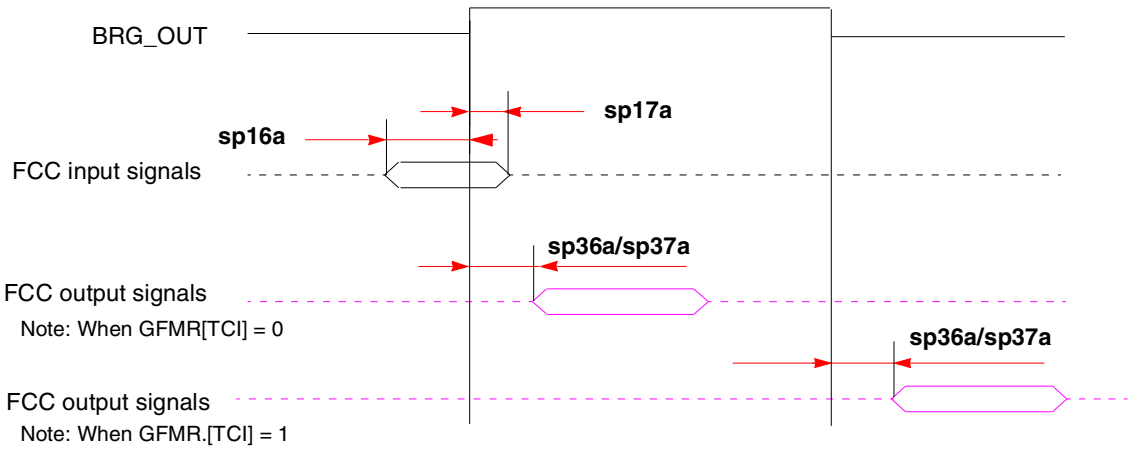



**Figure 3. FCC Internal Clock Diagram**

This figure shows the FCC external clock.

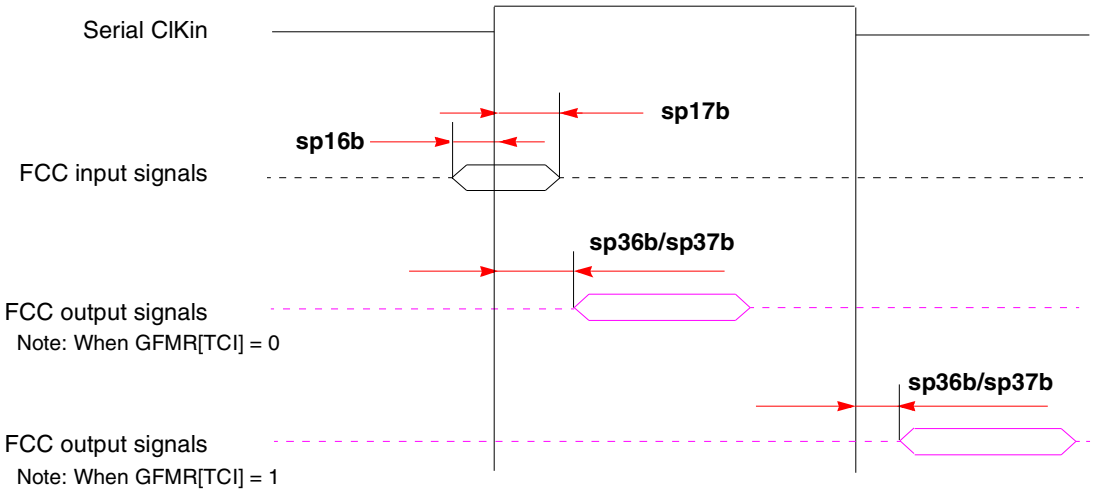
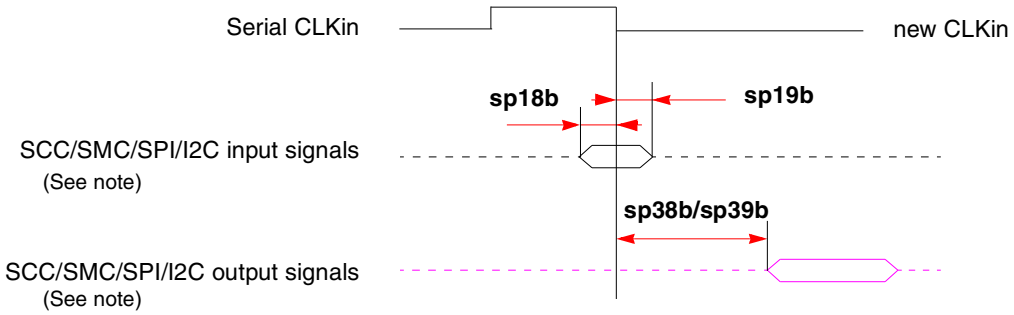



**Figure 4. FCC External Clock Diagram**

This figure shows the SCC/SMC/SPI/$I^2C$ external clock.

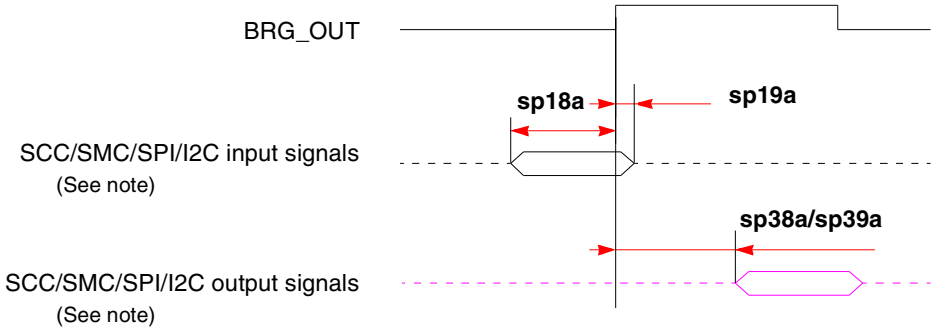



**Note:** There are four possible timing conditions for SPI:
1. Input sampled on the rising edge and output driven on the rising edge.
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge (shown).
4. Input sampled on the falling edge and output driven on the rising edge.

**Note:** There are two possible timing conditions for SCC/SMC/$I^2C$:
1. Input sampled on the falling edge and output driven on the falling edge (shown).
2. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/$I^2C$ External Clock Diagram**

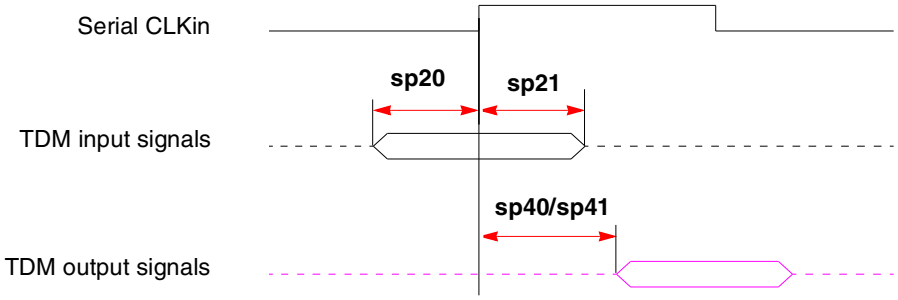
This figure shows the SCC/SMC/SPI/I$^2$C internal clock.




**Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I$^2$C Internal Clock Diagram**

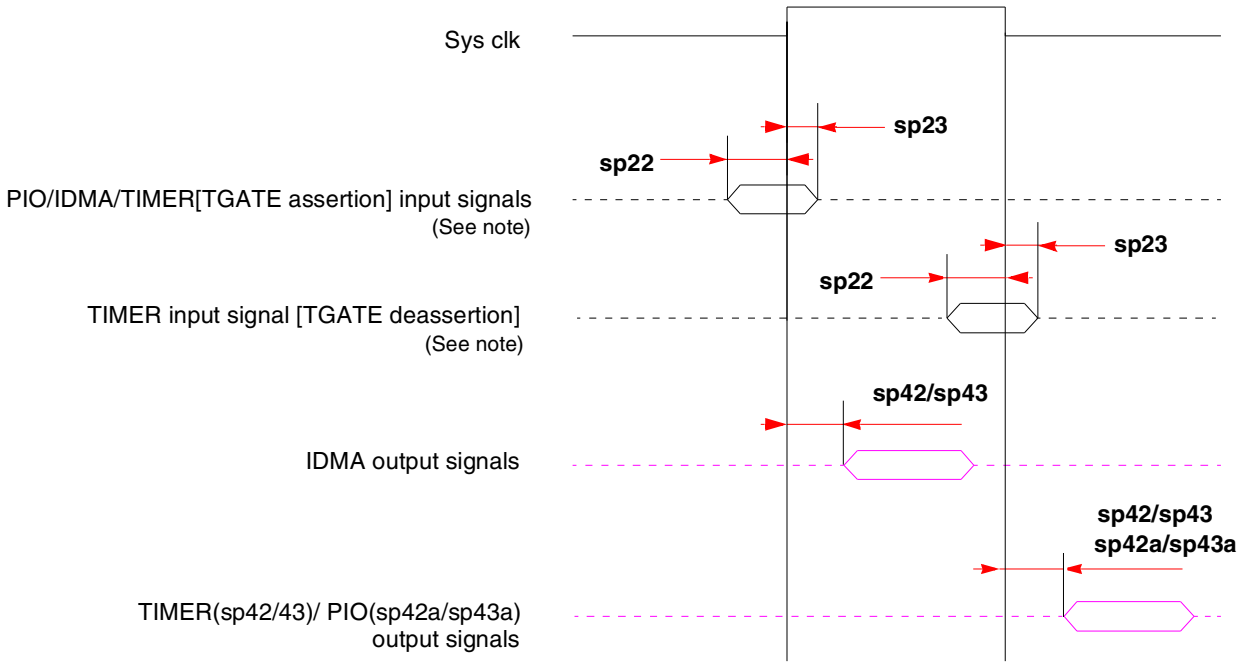
This figure shows TDM input and output signals.




**Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

This figure shows PIO and timer signals.




**Note:** TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

**Figure 8. PIO and Timer Signal Diagram**

## 6.2 SIU AC Characteristics

This table lists SIU input characteristics.

### NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (peak-to-peak) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60.

### NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

### NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 6 | 300.0 | 400.0 | 6 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 7 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 8 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0101_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0101_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3.5 | 175.0 | 233.3 | 2 | 50.0 | 66.7 |
| 0101_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4 | 200.0 | 266.6 | 2 | 50.0 | 66.7 |
| 0101_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4.5 | 225.0 | 300.0 | 2 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_101 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 3.5 | 291.7 | 388.9 | 5 | 50.0 | 66.7 |
| 0101_110 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 5 | 50.0 | 66.7 |
| 0101_111 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 2.5 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0110_001 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0110_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |
| 0110_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0110_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 3 | 50.0 | 66.7 |
| 0110_101 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 5 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0110_110 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 6 | 360.0 | 480.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0111_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1011_100 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 4 | 50.0 | 66.7 |
| 1011_101 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 4.5 | 360.0 | 480.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1101_000 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 5 | 50.0 | 66.7 |
| 1101_001 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 5 | 50.0 | 66.7 |
| 1101_010 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 5 | 50.0 | 66.7 |
| 1101_011 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 5 | 50.0 | 66.7 |
| 1101_100 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1101_101 | 125.0 | 166.7 | 2 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| 1101_110 | 125.0 | 166.7 | 2 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1110_000 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 3.5 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 1110_001 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| 1110_010 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 6 | 50.0 | 66.7 |
| 1110_011 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 6 | 50.0 | 66.7 |
| 1110_100 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. SeeTable 18 for lower range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 0, the ratio of CPM_CLK/PCI_CLK should be calculated from SCCR[PCIDF] as follows:
CPM_CLK/PCI_CLK = (PCIDF + 1) / 2.

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| Default Modes (MODCK_H=0000) | | | | | | | | | | | |
| 0000_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0000_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0000_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0000_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0000_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0000_101 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0000_110 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0000_111 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 0001_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 6 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0001_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 7 | 350.0 | 700.0 | 6 | 25.0 | 50.0 |
| 0001_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 8 | 400.0 | 800.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_000 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 0010_001 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 6 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 0010_010 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 7 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| 0010_011 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 8 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_100 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 0010_101 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5.5 | 206.3 | 412.5 | 6 | 25.0 | 50.0 |
| 0010_110 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 6 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0011_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 5 | 150.0 | 250.0 | 5 | 30.0 | 50.0 |
| 0011_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 6 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 0011_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 7 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 0011_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 8 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 1010_110 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1010_111 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 2 | 60.0 | 100.0 |
| 0000_001 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 2 | 50.0 | 100.0 |
| 0000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 0000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0000_110 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0000_111 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_001 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0001_010 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 6 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0001_011 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 7 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0001_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 8 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0010_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0010_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 0010_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | 37.5 | 50.0 | 4 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0011_010 | 32.1 | 50.0 | 4 | 128.6 | 200.0 | 3.5 | 150.0 | 233.3 | 3 | 42.9 | 66.7 |
| 0011_011 | 28.1 | 50.0 | 4 | 112.5 | 200.0 | 4 | 150.0 | 266.7 | 3 | 37.5 | 66.7 |
| 0011_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 4.5 | 150.0 | 300.0 | 3 | 33.3 | 66.7 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 3 | 50.0 | 100.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{TS}$ | | D1 |
| A0 | | A3 |
| A1 | | B5 |
| A2 | | D8 |
| A3 | | C6 |
| A4 | | A4 |
| A5 | | A6 |
| A6 | | B6 |
| A7 | | C7 |
| A8 | | B7 |
| A9 | | A7 |
| A10 | | D9 |
| A11 | | E11 |
| A12 | | C9 |
| A13 | | B9 |
| A14 | | D11 |
| A15 | | A9 |
| A16 | | B10 |
| A17 | | A10 |
| A18 | | B11 |
| A19 | | A11 |
| A20 | | D12 |
| A21 | | A12 |
| A22 | | D13 |
| A23 | | B13 |
| A24 | | C13 |
| A25 | | C14 |
| A26 | | B14 |
| A27 | | D14 |
| A28 | | E14 |
| A29 | | A14 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| A30 | | B15 |
| A31 | | A15 |
| TT0 | | B3 |
| TT1 | | E8 |
| TT2 | | D7 |
| TT3 | | C4 |
| TT4 | | E7 |
| $\overline{\text{TBST}}$ | | E3 |
| TSIZ0 | | E4 |
| TSIZ1 | | E5 |
| TSIZ2 | | C3 |
| TSIZ3 | | D5 |
| $\overline{\text{AACK}}$ | | D3 |
| $\overline{\text{ARTRY}}$ | | C2 |
| $\overline{\text{DBG}}$/$\overline{\text{IRQ7}}$ | | F16 |
| $\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$ | | D18 |
| D0 | | AC1 |
| D1 | | AA1 |
| D2 | | V3 |
| D3 | | R5 |
| D4 | | P4 |
| D5 | | M4 |
| D6 | | J4 |
| D7 | | G1 |
| D8 | | W6 |
| D9 | | Y3 |
| D10 | | V1 |
| D11 | | N6 |
| D12 | | P3 |
| D13 | | M2 |
| D14 | | J5 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| MODCK1/$\overline{\text{RSRV}}$/TC0/BNKSEL0 | | A20 |
| MODCK2/CSE0/TC1/BNKSEL1 | | C20 |
| MODCK3/CSE1/TC2/BNKSEL2 | | A21 |
| CLKIN1 | | D21 |
| PA8/SMRXD2 | | AF25[3] |
| PA9/SMTXD2 | | AA22[3] |
| PA10/MSNUM5 | FCC1_UT_RXD0 | AB23[3] |
| PA11/MSNUM4 | FCC1_UT_RXD1 | AD26[3] |
| PA12/MSNUM3 | FCC1_UT_RXD2 | AD25[3] |
| PA13/MSNUM2 | FCC1_UT_RXD3 | AA24[3] |
| PA14/FCC1_MII_HDLC_RXD3 | FCC1_UT_RXD4 | W22[3] |
| PA15/FCC1_MII_HDLC_RXD2 | FCC1_UT_RXD5 | Y24[3] |
| PA16/FCC1_MII_HDLC_RXD1 | FCC1_UT_RXD6 | T22[3] |
| PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RXD0 | FCC1_UT_RXD7 | W26[3] |
| PA18/FCC1_MII_HDLC_TXD0/FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0 | FCC1_UT_TXD7 | V26[3] |
| PA19/FCC1_MII_HDLC_TXD1/FCC1_RMII_TXD1 | FCC1_UT_TXD6 | R23[3] |
| PA20/FCC1_MII_HDLC_TXD2 | FCC1_UT_TXD5 | P25[3] |
| PA21/FCC1_MII_HDLC_TXD3 | FCC1_UT_TXD4 | N22[3] |
| PA22 | FCC1_UT_TXD3 | N26[3] |
| PA23 | FCC1_UT_TXD2 | N23[3] |
| PA24/MSNUM1 | FCC1_UT_TXD1 | H26[3] |
| PA25/MSNUM0 | FCC1_UT_TXD0 | G25[3] |
| PA26/FCC1_MII_RMIIRX_ER | FCC1_UT_RXCLAV | L22[3] |
| PA27/FCC1_MII_RX_DV/FCC1_RMII_CRS_DV | FCC1_UT_RXSOC | G24[3] |
| PA28/FCC1_MII_RMII_TX_EN | FCC1_UT_RXENB | G23[3] |
| PA29/FCC1_MII_TX_ER | $\overline{\text{FCC1\_UT\_TXSOC}}$ | B26[3] |
| PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$ | FCC1_UT_TXCLAV | A25[3] |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| CLKIN2 | | C21 |
| No connect[4] | | D19[4], J3[4], AD24[5] |
| I/O power | | B4, F3, J2, N4, AD1, AD5, AE8, AC13, AD18, AB24, AB26, W23, R25, M25, F25, C25, C22, B17, B12, B8, E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9 |
| Core Power | | F5, K5, M5, AA5, AB7, AA13, AA19, AA21, Y22, AC25, U22, R22, L21, H22, E22, E20, E15, F13, F11, F8, L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10 |
| Ground | | E19, E2, K1, Y2, AE1, AE4, AD9, AC14, AE17, AC19, AE25, V24, P26, M26, G26, E26, B21, C12, C11, C8, A8, B18, A18, A2, B1, B2, A5, C5, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17 |

1 Must be tied to ground.

2 Should be tied to VDDH via a 2K Ω external pull-up resistor.

3 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

4 This pin is not connected. It should be left floating.

5 Must be pulled down or left floating

# 9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

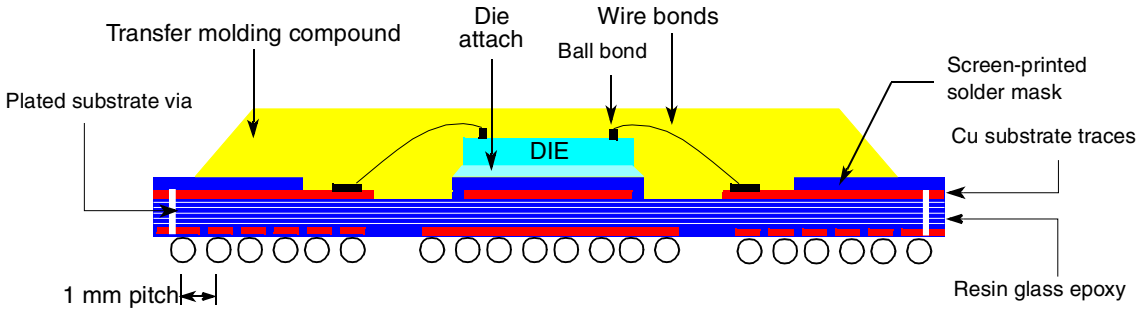



**Figure 13. Side View of the PBGA Package Remove**

## 9.1 Package Parameters

This table provides package parameters.

**Table 22. Package Parameters**

| Code | Type | Outline (mm) | Interconnects | Pitch (mm) | Nominal Unmounted Height (mm) |
|---|---|---|---|---|---|
| VR, ZQ | PBGA | 27 x 27 | 516 | 1 | 2.25 |

**NOTE: Temperature Reflow for the VR Package**

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

## 9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

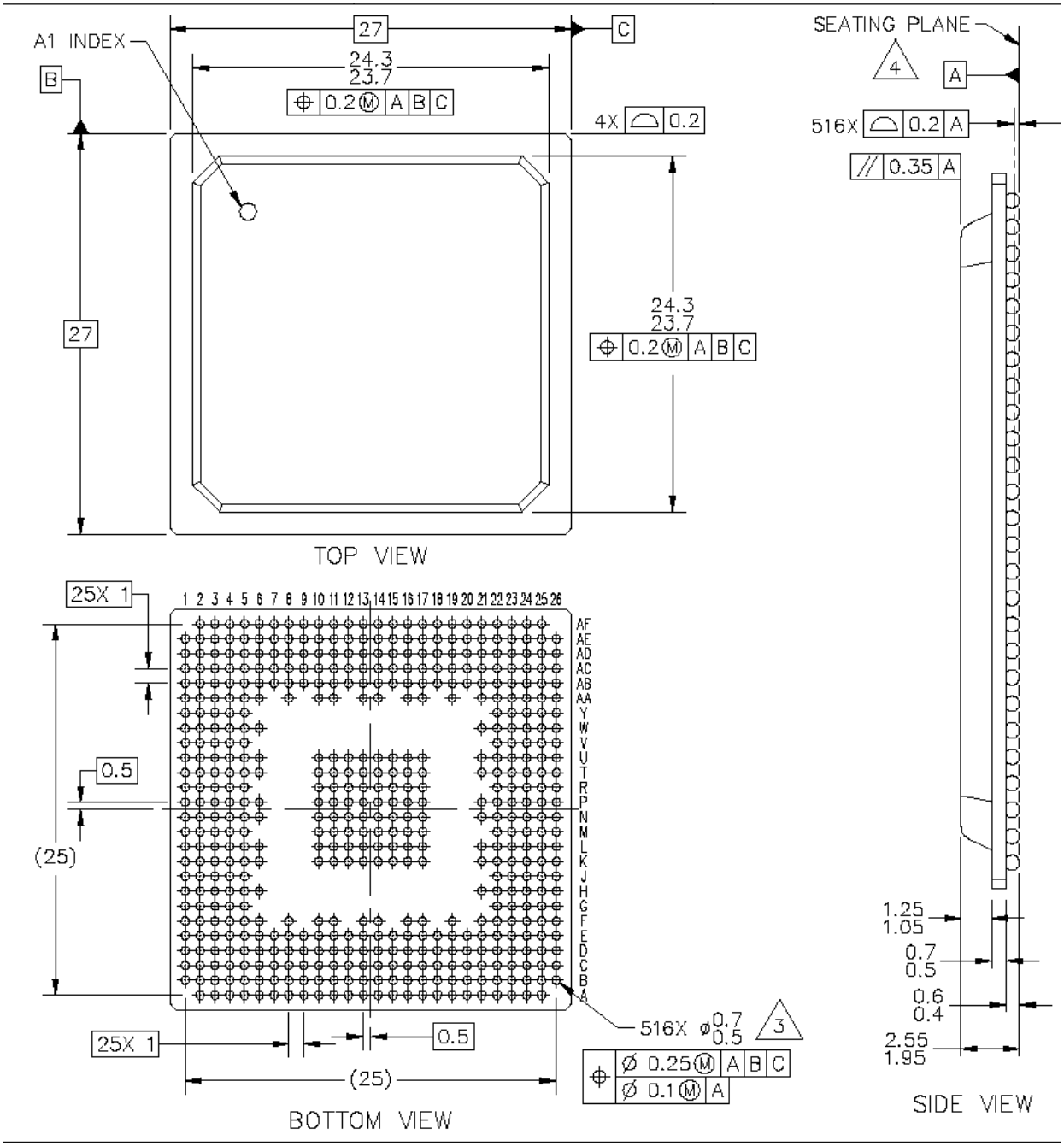



**Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA**