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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8271cvrtiea

  - Floating-point unit (FPU) supports floating-point arithmetic
  - Support for cache locking
- Low-power consumption
- Separate power supply for internal logic (1.5 V) and for I/O (3.3 V)
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 5.5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs—up to two external masters
  - Supports single transfers and burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
    - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- Eight bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x)
  - Dedicated interface logic for SDRAM
- Disable CPU mode

3 DC Electrical Characteristics

This table shows DC electrical characteristics.

Table 5. DC Electrical Characteristics[1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2]	V_{IH}	2.0	3.465	V
Input low voltage[3]	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH[4]	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	μA
Signal low input current, V_{IL} = 0.8 V	I_L	—	1	μA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	μA
Output high voltage, I_{OH} = –2 mA except UTOPIA mode, and open drain pins In UTOPIA mode[5] (UTOPIA pins only): I_{OH} = -8.0mA PA[8–31] PB[18–31] PC[0–1,4–29] PD[7–25, 29–31]	V_{OH}	2.4	—	V
In UTOPIA mode[5] (UTOPIA pins only): I_{OL} = 8.0mA PA[8–31] PB[18–31] PC[0–1,4–29] PD[7–25, 29–31]	V_{OL}	—	0.5	V

Table 5. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0–5] CS6/BCTL1/SMI CS7/TLBSYNC BADDR27/ IRQ1 BADDR28/ IRQ2 ALE/ IRQ4 BCTL0 PWE[0–7]/PSDDQM[0–7]/PBS[0–7] PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4 PSDAMUX/PGPL5 PCI_CFG0 (PCI_HOST_EN) PCI_CFG1 (PCI_ARB_EN) PCI_CFG2 (DLL_ENABLE) MODCK1/RSRV/TC(0)/BNKSEL(0) MODCK2/CSE0/TC(1)/BNKSEL(1) MODCK3CSE1/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA PCI_PAR PCI_FRAME PCI_TRDY PCI_IRDY PCI_STOP PCI_DEVSEL PCI_IDSEL PCI_PERR PCI_SERR PCI_REQ0 PCI_REQ1/ CPI_HS_ES PCI_GNT0 PCI_GNT1/ CPI_HS_LES PCI_GNT2/ CPI_HS_ENUM PCI_RST PCI_INTA PCI_REQ2 DLLOUT PCI_AD(0-31) PCI_C(0–3)/BE(0-3) PA[8–31] PB[18–31] PC[0–1,4–29] PD[7–25, 29–31] TDO				

1 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.

4 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

Table 6.

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE[0–7]/PSDDQM[0–7]/PBS[0–7] PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3] LSDA10/LGPL0/PCI_MODCKH0 LSDWE/LGPL1/PCI_MODCKH1 LOE/LSDRAS/LGPL2/PCI_MODCKH2 LSDCAS/LGPL3/PCI_MODCKH3 LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK LWR MODCK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2]	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR L_A15/FRAME/SMI L_A16/TRDY L_A17/IRDY/CKSTP_OUT L_A18/STOP L_A19/DEVSEL L_A20/IDSEL L_A21/PERR L_A22/SERR L_A23/REQ0 L_A24/REQ1/HSEJSW L_A25/GNT0 L_A26/GNT1/HSLED L_A27/GNT2/HSENUM L_A28/RST/CORE_SRESET L_A29/INTAL_A30/REQ2 L_A31 LCL_D[0-31)]/AD[0-31] LCL_DP[03]/C/BE[0-3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO QREQ				

1 TCK, TRST and PORESET have min VIH = 2.5V.

2 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

3 V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

This figure shows the FCC external clock.

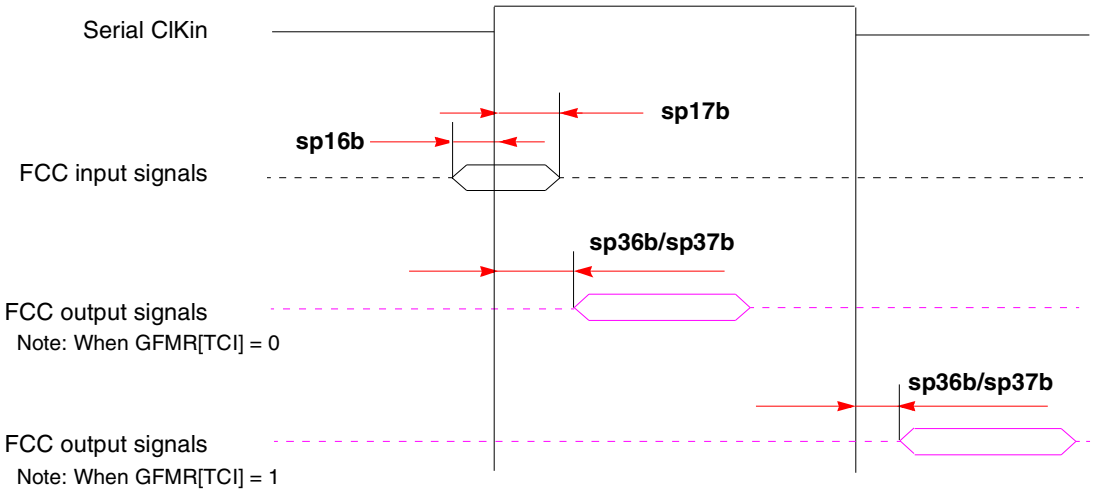
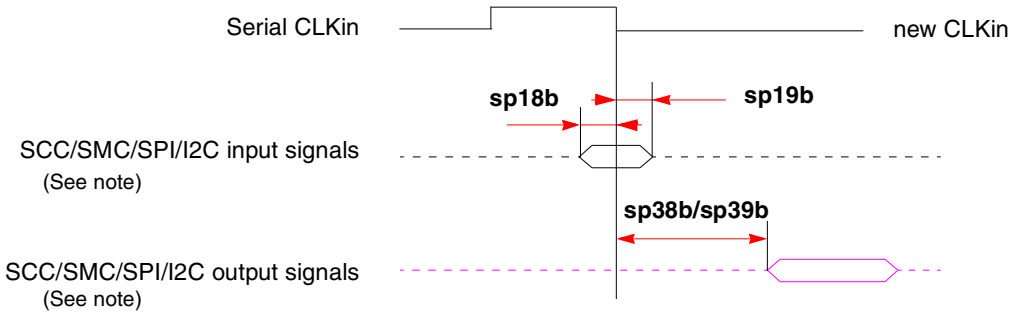


Figure 4. FCC External Clock Diagram

This figure shows the SCC/SMC/SPI/I^2C external clock.



Note: There are four possible timing conditions for SPI:
1. Input sampled on the rising edge and output driven on the rising edge.
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge (shown).
4. Input sampled on the falling edge and output driven on the rising edge.

Note: There are two possible timing conditions for SCC/SMC/I^2C:
1. Input sampled on the falling edge and output driven on the falling edge (shown).
2. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^2C External Clock Diagram

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing.

This figure shows the interaction of several bus signals.

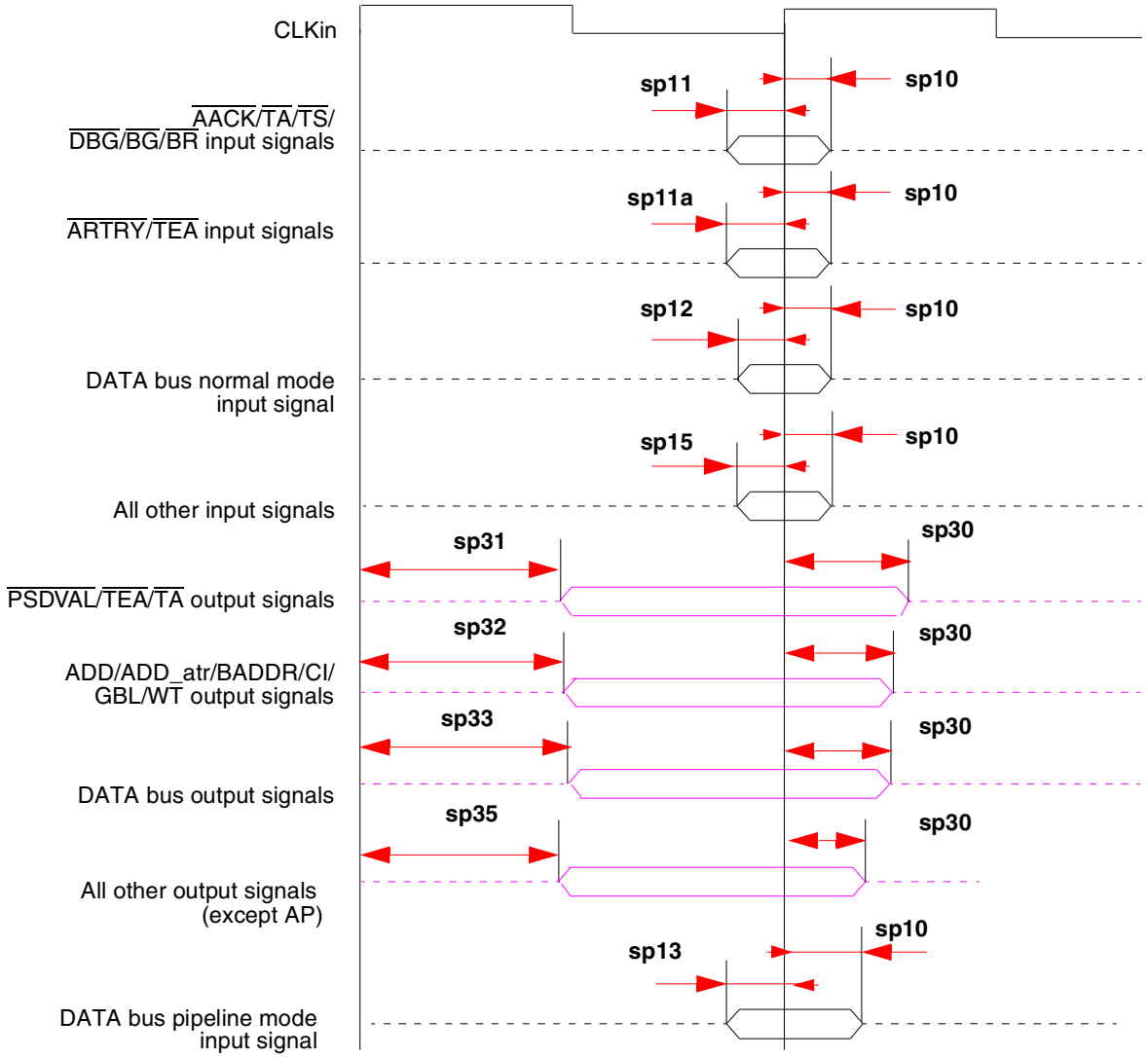


Figure 9. Bus Signals

7 Clock Configuration Modes

As shown in this table, the clocking mode is set according to two sources:

- PCI_CFG[0]— An input signal. Also defined as "$\overline{\text{PCI\_HOST\_EN}}$." See Chapter 6, "External Signals," and Chapter 9, "PCI Bridge," in the SoC reference manual.
- PCI_MODCK—Bit 27 in the Hard Reset Configuration Word. See Chapter 5, "Reset," in the SoC reference manual.

Table 16. SoC Clocking Modes

Pins		Clocking Mode	PCI Clock Frequency Range (MHz)	Reference
PCI_CFG[0][1]	PCI_MODCK[2]			
0	0	PCI host	50–66	Table 17
0	1		25–50	Table 18
1	0	PCI agent	50–66	Table 19
1	1		25–50	Table 20

1 PCI_HOST_EN
2 Determines PCI clock frequency range.

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

NOTE: Tval (Output Hold)

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

7.1 PCI Host Mode

These tables show configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI host mode the input clock is the bus clock.

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_100	80.0	106.7	2.5	200.0	266.6	4	320.0	426.6	4	50.0	66.7
1011_101	80.0	106.7	2.5	200.0	266.6	4.5	360.0	480.0	4	50.0	66.7
1101_000	100.0	133.3	2.5	250.0	333.3	3	300.0	400.0	5	50.0	66.7
1101_001	100.0	133.3	2.5	250.0	333.3	3.5	350.0	466.6	5	50.0	66.7
1101_010	100.0	133.3	2.5	250.0	333.3	4	400.0	533.3	5	50.0	66.7
1101_011	100.0	133.3	2.5	250.0	333.3	4.5	450.0	599.9	5	50.0	66.7
1101_100	100.0	133.3	2.5	250.0	333.3	5	500.0	666.6	5	50.0	66.7
1101_101	125.0	166.7	2	250.0	333.3	3	375.0	500.0	5	50.0	66.7
1101_110	125.0	166.7	2	250.0	333.3	4	500.0	666.6	5	50.0	66.7
1110_000	100.0	133.3	3	300.0	400.0	3.5	350.0	466.6	6	50.0	66.7
1110_001	100.0	133.3	3	300.0	400.0	4	400.0	533.3	6	50.0	66.7
1110_010	100.0	133.3	3	300.0	400.0	4.5	450.0	599.9	6	50.0	66.7
1110_011	100.0	133.3	3	300.0	400.0	5	500.0	666.6	6	50.0	66.7
1110_100	100.0	133.3	3	300.0	400.0	5.5	550.0	733.3	6	50.0	66.7
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. SeeTable 18 for lower range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 0, the ratio of CPM_CLK/PCI_CLK should be calculated from SCCR[PCIDF] as follows:
CPM_CLK/PCI_CLK = (PCIDF + 1) / 2.

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2]

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0000_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0000_010	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0000_011	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0000_100	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0000_101	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0000_110	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0000_111	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
Full Configuration Modes											
0001_000	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
0001_001	50.0	100.0	3	150.0	300.0	6	300.0	600.0	6	25.0	50.0
0001_010	50.0	100.0	3	150.0	300.0	7	350.0	700.0	6	25.0	50.0
0001_011	50.0	100.0	3	150.0	300.0	8	400.0	800.0	6	25.0	50.0
0010_000	50.0	100.0	4	200.0	400.0	5	250.0	500.0	8	25.0	50.0
0010_001	50.0	100.0	4	200.0	400.0	6	300.0	600.0	8	25.0	50.0
0010_010	50.0	100.0	4	200.0	400.0	7	350.0	700.0	8	25.0	50.0
0010_011	50.0	100.0	4	200.0	400.0	8	400.0	800.0	8	25.0	50.0
0010_100	37.5	75.0	4	150.0	300.0	5	187.5	375.0	6	25.0	50.0
0010_101	37.5	75.0	4	150.0	300.0	5.5	206.3	412.5	6	25.0	50.0
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0000_110	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
Full Configuration Modes											
0001_001	60.0	66.7	2	120.0	133.3	5	150.0	166.7	4	30.0	33.3
0001_010	50.0	66.7	2	100.0	133.3	6	150.0	200.0	4	25.0	33.3
0001_011	50.0	66.7	2	100.0	133.3	7	175.0	233.3	4	25.0	33.3
0001_100	50.0	66.7	2	100.0	133.3	8	200.0	266.6	4	25.0	33.3
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0010_011	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_010	Reserved										
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1011_101	25.0	50.0	8	200.0	400.0	2.5	250.0	500.0	2	100.0	200.0
1011_110	25.0	50.0	8	200.0	400.0	3	300.0	600.0	2	100.0	200.0
1011_111	25.0	50.0	8	200.0	400.0	3.5	350.0	700.0	2	100.0	200.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D15		G3
D16		AB3
D17		Y1
D18		T4
D19		T3
D20		P2
D21		M1
D22		J1
D23		G4
D24		AB2
D25		W4
D26		V2
D27		T1
D28		N5
D29		L1
D30		H1
D31		G5
D32		W5
D33		W2
D34		T5
D35		T2
D36		N1
D37		K3
D38		H2
D39		F1
D40		AA2
D41		W1
D42		U3
D43		R2
D44		N2
D45		L2

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D46		H4
D47		F2
D48		AB1
D49		U4
D50		U1
D51		R3
D52		N3
D53		K2
D54		H5
D55		F4
D56		AA3
D57		U5
D58		U2
D59		P5
D60		M3
D61		K4
D62		H3
D63		E1
$\overline{\text{IRQ3}}$/CKSTP_OUT/EXT_BR3		B16
$\overline{\text{IRQ4}}$/CORE_SRESET/EXT_BG3		C15
$\overline{\text{IRQ5}}$/TBEN/EXT_DBG3/$\overline{\text{CINT}}$		Y4
$\overline{\text{PSDVAL}}$		C19
$\overline{\text{TA}}$		AA4
$\overline{\text{TEA}}$		AB6
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		D15
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		D16
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		C16
BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		E17
$\overline{\text{CPU\_BR}}$/$\overline{\text{INT\_OUT}}$		B20
$\overline{\text{CS0}}$		AE6
$\overline{\text{CS1}}$		AD7

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
$\overline{\text{CS2}}$		AF5
$\overline{\text{CS3}}$		AC8
$\overline{\text{CS4}}$		AF6
$\overline{\text{CS5}}$		AD8
$\overline{\text{CS6}}$/BCTL1/$\overline{\text{SMI}}$		AC9
$\overline{\text{CS7}}$/TLBISYNC		AB9
BADDR27/$\overline{\text{IRQ1}}$		AB8
BADDR28/$\overline{\text{IRQ2}}$		AC7
ALE/$\overline{\text{IRQ4}}$		AF4
$\overline{\text{BCTL0}}$		AF3
$\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$		AD6
$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$		AE5
$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$		AE3
$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$		AF2
$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$		AC6
$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$		AC5
$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$		AD4
$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$		AB5
PSDA10/PGPL0		AE2
$\overline{\text{PSDWE}}$/PGPL1		AD3
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2		AB4
$\overline{\text{PSDCAS}}$/PGPL3		AC3
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4		AD2
PSDAMUX/PGPL5		AC2
$\overline{\text{PCI\_MODE}}$[1]		AD22
PCI_CFG0 ($\overline{\text{PCI\_HOST\_EN}}$)		AC21
PCI_CFG1 ($\overline{\text{PCI\_ARB\_EN}}$)		AE22
PCI_CFG2 (DLL_ENABLE)		AE23
PCI_ PAR		AF12
$\overline{\text{PCI\_FRAME}}$		AD15
$\overline{\text{PCI\_TRDY}}$		AF16

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
CLKIN2		C21
No connect[4]		D19[4], J3[4], AD24[5]
I/O power		B4, F3, J2, N4, AD1, AD5, AE8, AC13, AD18, AB24, AB26, W23, R25, M25, F25, C25, C22, B17, B12, B8, E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9
Core Power		F5, K5, M5, AA5, AB7, AA13, AA19, AA21, Y22, AC25, U22, R22, L21, H22, E22, E20, E15, F13, F11, F8, L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground		E19, E2, K1, Y2, AE1, AE4, AD9, AC14, AE17, AC19, AE25, V24, P26, M26, G26, E26, B21, C12, C11, C8, A8, B18, A18, A2, B1, B2, A5, C5, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

1 Must be tied to ground.

2 Should be tied to VDDH via a 2K Ω external pull-up resistor.

3 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

4 This pin is not connected. It should be left floating.

5 Must be pulled down or left floating

9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

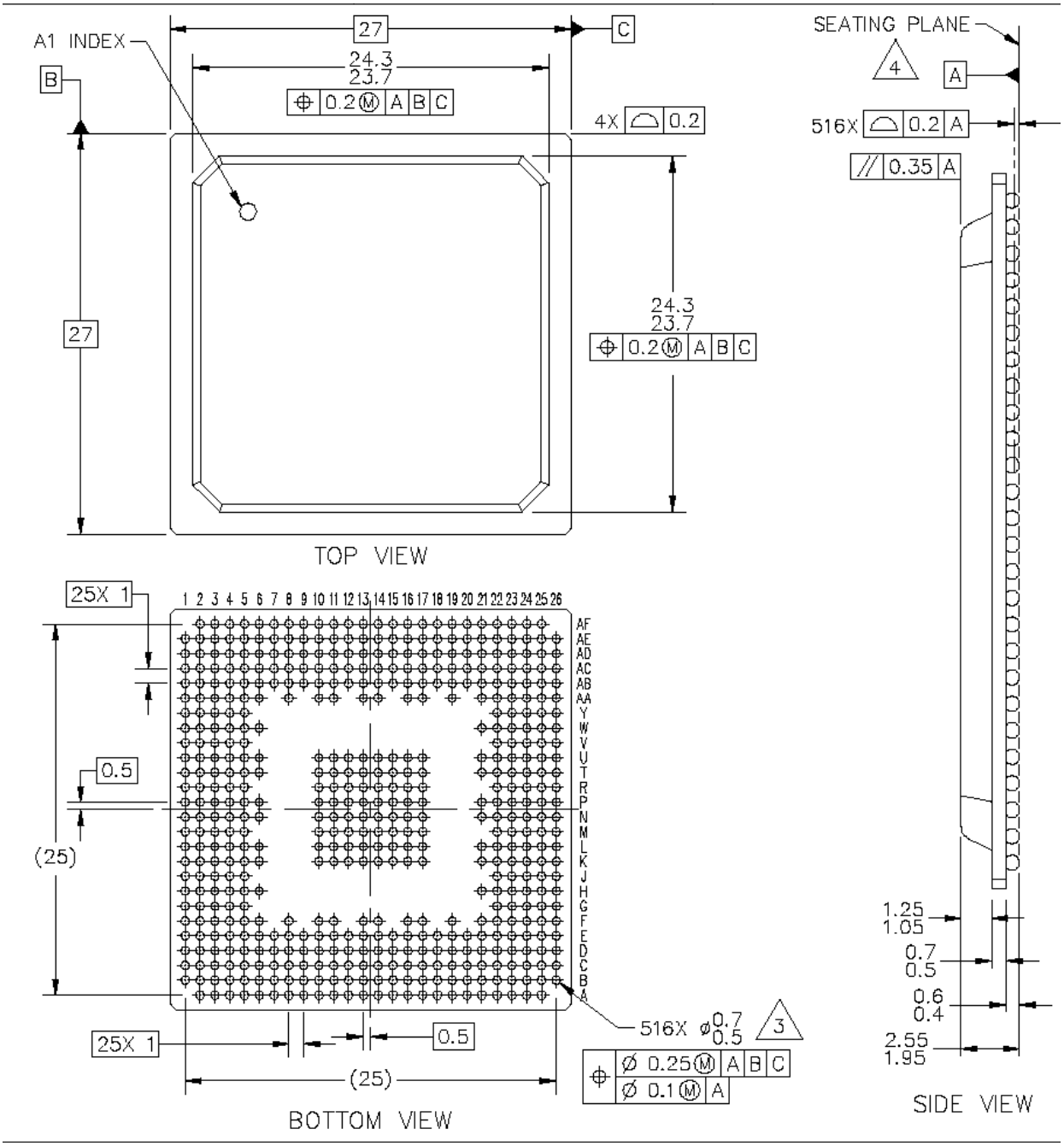


Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

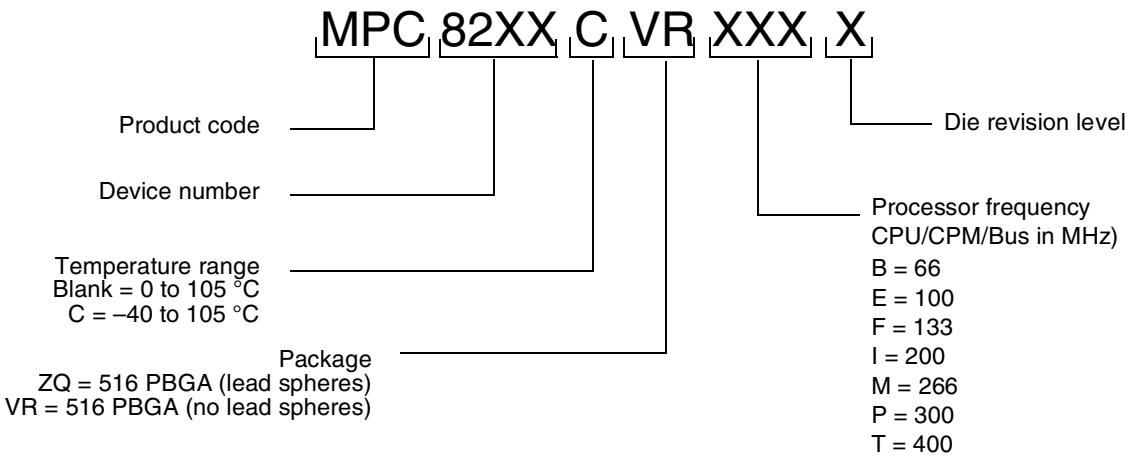


Figure 15. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
3	09/2011	In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
2	12/2008	• Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes. • In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.” • In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency. • Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.” • Removed overbar from DLL_ENABLE in Table 21, “Pinout.”
1.5	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.4	05/2006	• Added row for 133 MHz configurations to Table 8.
1.3	02/2006	• Inserted Section 6.3, “JTAG Timings.”

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
1.2	09/2005	• Added 133-MHz to the list of frequencies in the opening sentence of Section 6, "AC Electrical Characteristics". • Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13. • Added footnote 2 to Table 13. • Added the conditions note directly above Table 12.
1.1	01/2005	• Modification for correct display of assertion level ("overbar") for some signals
1.0	12/2004	• Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values • Section 2: removed voltage tracking note • Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset • Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V • Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed. • Section 4.6: Updated description of layout practices • Table 8: Note 3 added regarding IIC compatibility • Table 8: Updated nominal and maximum power dissipation values • Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance • Section 6: Added sentence providing derating factor • Section 6.1: added Note: Rise/Fall Time on CPM Input Pins • Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a • Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22 • Section 6.2: added spread spectrum clocking note • Section 6.2: added CLKIN jitter note • Table 12: combined specs sp11 and sp11a • Table 13: sp30 Data Bus minimum delay values changed to 0.8 • Section 7: unit of ns added to Tval notes • Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. • Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. • Table 21: correct superscript of footnote number after pin AD22 • Table 21: remove DONE3 from PC12 • Table 21: signals referring to TDMs C2 and D2 removed