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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8271czqtiea

  - Floating-point unit (FPU) supports floating-point arithmetic
  - Support for cache locking
- Low-power consumption
- Separate power supply for internal logic (1.5 V) and for I/O (3.3 V)
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 5.5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs—up to two external masters
  - Supports single transfers and burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
    - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- Eight bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x)
  - Dedicated interface logic for SDRAM
- Disable CPU mode

- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
  - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
  - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
  - Microcode tracing capabilities
  - Eight CPM trap registers
- Universal serial bus (USB) controller
  - Supports USB 2.0 full/low rate compatible
  - USB host mode
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
  - Supports USB slave mode
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Two fast communication controllers (FCCs) supporting the following protocols:
    - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—up to T3 rates (clear channel)

[4] MPC8280, MPC8275VR, MPC8275ZQ only.

4 Thermal Characteristics

This table describes thermal characteristics. See Table 2 for information on a given SoC’s package. Discussions of each characteristic are provided in Section 4.1, “Estimation with Junction-to-Ambient Thermal Resistance,” through Section 4.7, “References.” For the these discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

Table 7. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Air Flow
Junction-to-ambient—single-layer board[1]	$R_{\theta JA}$	27	°C/W	Natural convection
		21		1 m/s
Junction-to-ambient—four-layer board	$R_{\theta JA}$	19	°C/W	Natural convection
		16		1 m/s
Junction-to-board[2]	$R_{\theta JB}$	11	°C/W	—
Junction-to-case[3]	$R_{\theta JC}$	8	°C/W	—
Junction-to-package top[4]	$R_{\theta JT}$	2	°C/W	—

[1] Assumes no thermal vias

[2] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[3] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[4] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in ▯ C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board’s power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

4.7 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

Table 8. Estimated Power Dissipation for Various Configurations[1]

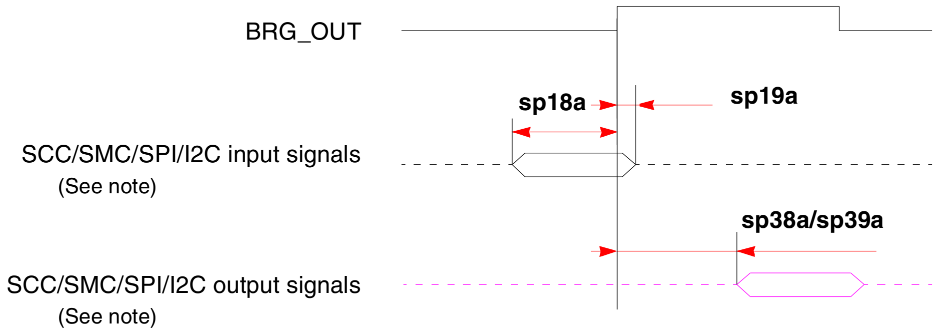
Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	P_{INT}(W)[2,3]	
					Vddl 1.5 Volts	
					Nominal	Maximum
66.67	3	200	4	266	1	1.2
100	2	200	3	300	1.1	1.3
100	2	200	4	400	1.3	1.5
133	2	267	3	400	1.5	1.8

[1] Test temperature = 105° C

[2] $P_{INT} = I_{DD} \times V_{DD}$ Watts

[3] Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.35 W (nominal), 0.4 W (maximum)
83.3 MHz = 0.4 W (nominal), 0.5 W (maximum)
100 MHz = 0.5 W (nominal), 0.6 W (maximum)
133 MHz = 0.7 W (nominal), 0.8 W (maximum)

This figure shows the SCC/SMC/SPI/I^2C internal clock.

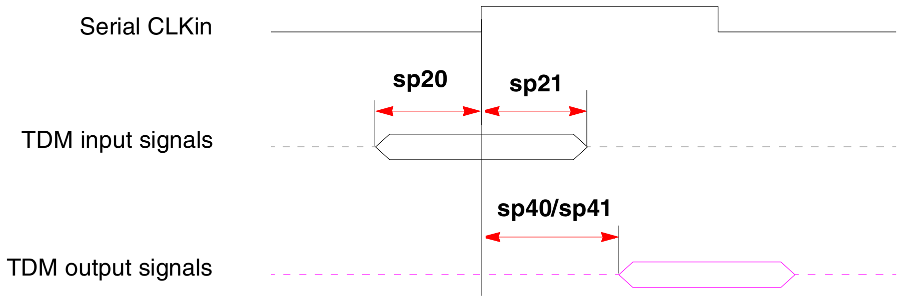


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^2C Internal Clock Diagram

This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

This figure shows signal behavior in MEMC mode.

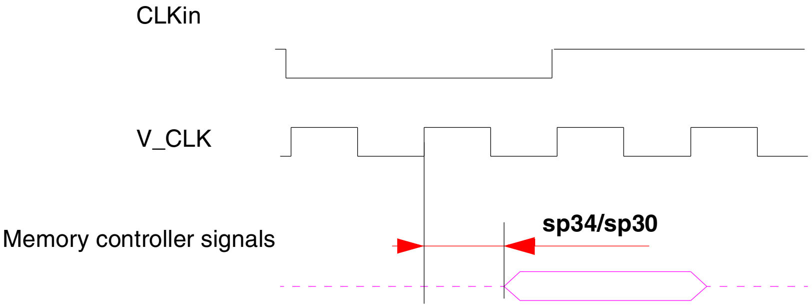


Figure 10. MEMC Mode Diagram

NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 14.

Table 14. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

This table is a representation of the information in Table 14.

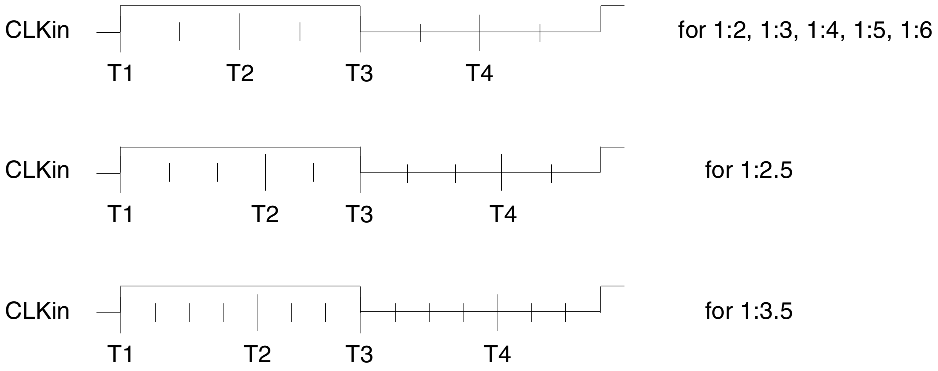


Figure 11. Internal Tick Spacing for Memory Controller Signals

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0101_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0101_010	50.0	66.7	2	100.0	133.3	3.5	175.0	233.3	2	50.0	66.7
0101_011	50.0	66.7	2	100.0	133.3	4	200.0	266.6	2	50.0	66.7
0101_100	50.0	66.7	2	100.0	133.3	4.5	225.0	300.0	2	50.0	66.7
0101_101	83.3	111.1	3	250.0	333.3	3.5	291.7	388.9	5	50.0	66.7
0101_110	83.3	111.1	3	250.0	333.3	4	333.3	444.4	5	50.0	66.7
0101_111	83.3	111.1	3	250.0	333.3	4.5	375.0	500.0	5	50.0	66.7
0110_000	60.0	80.0	2.5	150.0	200.0	2.5	150.0	200.0	3	50.0	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0110_011	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7
0111_000	Reserved										
0111_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0111_010	50.0	66.7	3	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0111_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0111_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
1000_000	Reserved										
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_010	66.7	88.9	3	200.0	266.6	3.5	233.3	311.1	4	50.0	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200.0	266.6	3.5	200.0	266.6	4	50.0	66.7
1001_011	57.1	76.2	3.5	200.0	266.6	4	228.6	304.7	4	50.0	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1010_101	100.0	133.3	2	200.0	266.6	2.5	250.0	333.3	4	50.0	66.7
1010_110	100.0	133.3	2	200.0	266.6	3	300.0	400.0	4	50.0	66.7
1010_111	100.0	133.3	2	200.0	266.6	3.5	350.0	466.6	4	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

[1] The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

[2] PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

[3] MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

[4] CPM multiplication factor = CPM clock/bus clock

[5] CPU multiplication factor = Core PLL multiplication factor

[6] CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI agent mode the input clock is PCI clock.

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0000_110	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
Full Configuration Modes											
0001_001	60.0	66.7	2	120.0	133.3	5	150.0	166.7	4	30.0	33.3
0001_010	50.0	66.7	2	100.0	133.3	6	150.0	200.0	4	25.0	33.3
0001_011	50.0	66.7	2	100.0	133.3	7	175.0	233.3	4	25.0	33.3
0001_100	50.0	66.7	2	100.0	133.3	8	200.0	266.6	4	25.0	33.3
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0010_011	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0100_100	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
0101_000	30.0	50.0	5	150.0	250.0	2.5	150.0	250.0	2.5	60.0	100.0
0101_001	25.0	50.0	5	125.0	250.0	3	150.0	300.0	2.5	50.0	100.0
0101_010	25.0	50.0	5	125.0	250.0	3.5	175.0	350.0	2.5	50.0	100.0
0101_011	25.0	50.0	5	125.0	250.0	4	200.0	400.0	2.5	50.0	100.0
0101_100	25.0	50.0	5	125.0	250.0	4.5	225.0	450.0	2.5	50.0	100.0
0101_101	25.0	50.0	5	125.0	250.0	5	250.0	500.0	2.5	50.0	100.0
0101_110	25.0	50.0	5	125.0	250.0	5.5	275.0	550.0	2.5	50.0	100.0
0110_000	Reserved										
0110_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
0110_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0110_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
0110_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
0111_000	25.0	50.0	6	150.0	300.0	2	150.0	300.0	2	75.0	150.0
0111_001	25.0	50.0	6	150.0	300.0	2.5	187.5	375.0	2	75.0	150.0
0111_010	25.0	50.0	6	150.0	300.0	3	225.0	450.0	2	75.0	150.0
0111_011	25.0	50.0	6	150.0	300.0	3.5	262.5	525.0	2	75.0	150.0
1000_000	Reserved										
1000_001	25.0	50.0	6	150.0	300.0	2.5	150.0	300.0	2.5	60.0	120.0
1000_010	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
1000_011	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1000_100	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1000_101	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1001_000	Reserved										
1001_001	Reserved										

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_010	Reserved										
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1011_101	25.0	50.0	8	200.0	400.0	2.5	250.0	500.0	2	100.0	200.0
1011_110	25.0	50.0	8	200.0	400.0	3	300.0	600.0	2	100.0	200.0
1011_111	25.0	50.0	8	200.0	400.0	3.5	350.0	700.0	2	100.0	200.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

[1] The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

[2] PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

[3] MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

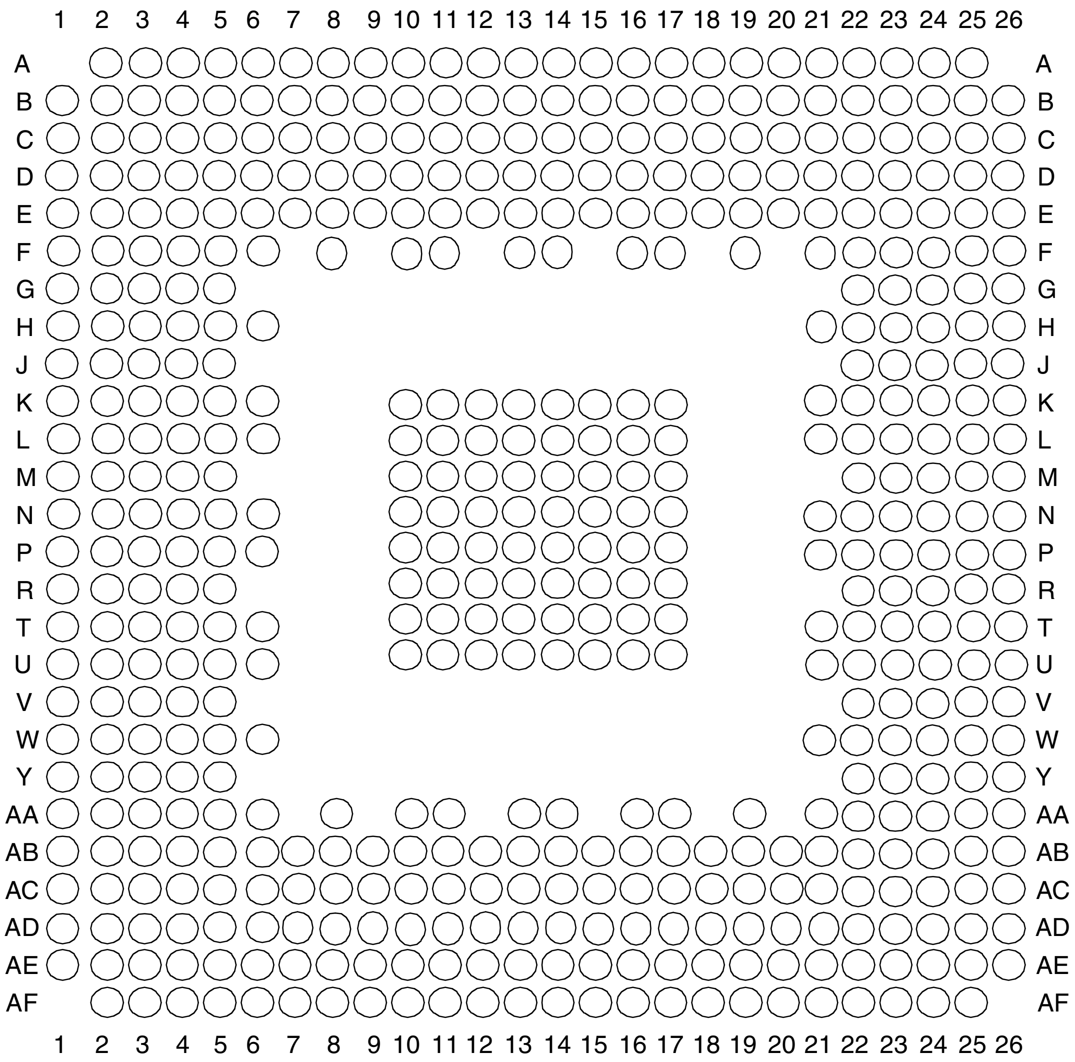
[4] CPM multiplication factor = CPM clock/bus clock

[5] CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.

This figure shows the pinout of the 516 PBGA package as viewed from the top surface.



Not to Scale

Figure 12. Pinout of the 516 PBGA Package (View from Top)

This table lists the pins of the MPC8272. Note that the pins in the “MPC8272/8271 Only” column relate to Utopia functionality.

Table 21. Pinout

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	**MPC8272/MPC8271 Only**	
$\overline{\text{BR}}$		A19
$\overline{\text{BG}}$/$\overline{\text{IRQ6}}$		D2
$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$		C1

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	**MPC8272/MPC8271 Only**	
A30		B15
A31		A15
TT0		B3
TT1		E8
TT2		D7
TT3		C4
TT4		E7
$\overline{\text{TBST}}$		E3
TSIZ0		E4
TSIZ1		E5
TSIZ2		C3
TSIZ3		D5
$\overline{\text{AACK}}$		D3
$\overline{\text{ARTRY}}$		C2
$\overline{\text{DBG}}/\overline{\text{IRQ7}}$		F16
$\overline{\text{DBB}}/\overline{\text{IRQ3}}$		D18
D0		AC1
D1		AA1
D2		V3
D3		R5
D4		P4
D5		M4
D6		J4
D7		G1
D8		W6
D9		Y3
D10		V1
D11		N6
D12		P3
D13		M2
D14		J5

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
MODCK1/$\overline{\text{RSRV}}$/TC0/BNKSEL0		A20
MODCK2/CSE0/TC1/BNKSEL1		C20
MODCK3/CSE1/TC2/BNKSEL2		A21
CLKIN1		D21
PA8/SMRXD2		AF25[3]
PA9/SMTXD2		AA22[3]
PA10/MSNUM5	FCC1_UT_RXD0	AB23[3]
PA11/MSNUM4	FCC1_UT_RXD1	AD26[3]
PA12/MSNUM3	FCC1_UT_RXD2	AD25[3]
PA13/MSNUM2	FCC1_UT_RXD3	AA24[3]
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT_RXD4	W22[3]
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT_RXD5	Y24[3]
PA16/FCC1_MII_HDLC_RXD1	FCC1_UT_RXD6	T22[3]
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RXD0	FCC1_UT_RXD7	W26[3]
PA18/FCC1_MII_HDLC_TXD0/FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT_TXD7	V26[3]
PA19/FCC1_MII_HDLC_TXD1/FCC1_RMII_TXD1	FCC1_UT_TXD6	R23[3]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT_TXD5	P25[3]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT_TXD4	N22[3]
PA22	FCC1_UT_TXD3	N26[3]
PA23	FCC1_UT_TXD2	N23[3]
PA24/MSNUM1	FCC1_UT_TXD1	H26[3]
PA25/MSNUM0	FCC1_UT_TXD0	G25[3]
PA26/FCC1_MII_RMIIRX_ER	FCC1_UT_RXCLAV	L22[3]
PA27/FCC1_MII_RX_DV/FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	G24[3]
PA28/FCC1_MII_RMII_TX_EN	FCC1_UT_RXENB	G23[3]
PA29/FCC1_MII_TX_ER	$\overline{\text{FCC1\_UT\_TXSOC}}$	B26[3]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UT_TXCLAV	A25[3]

9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

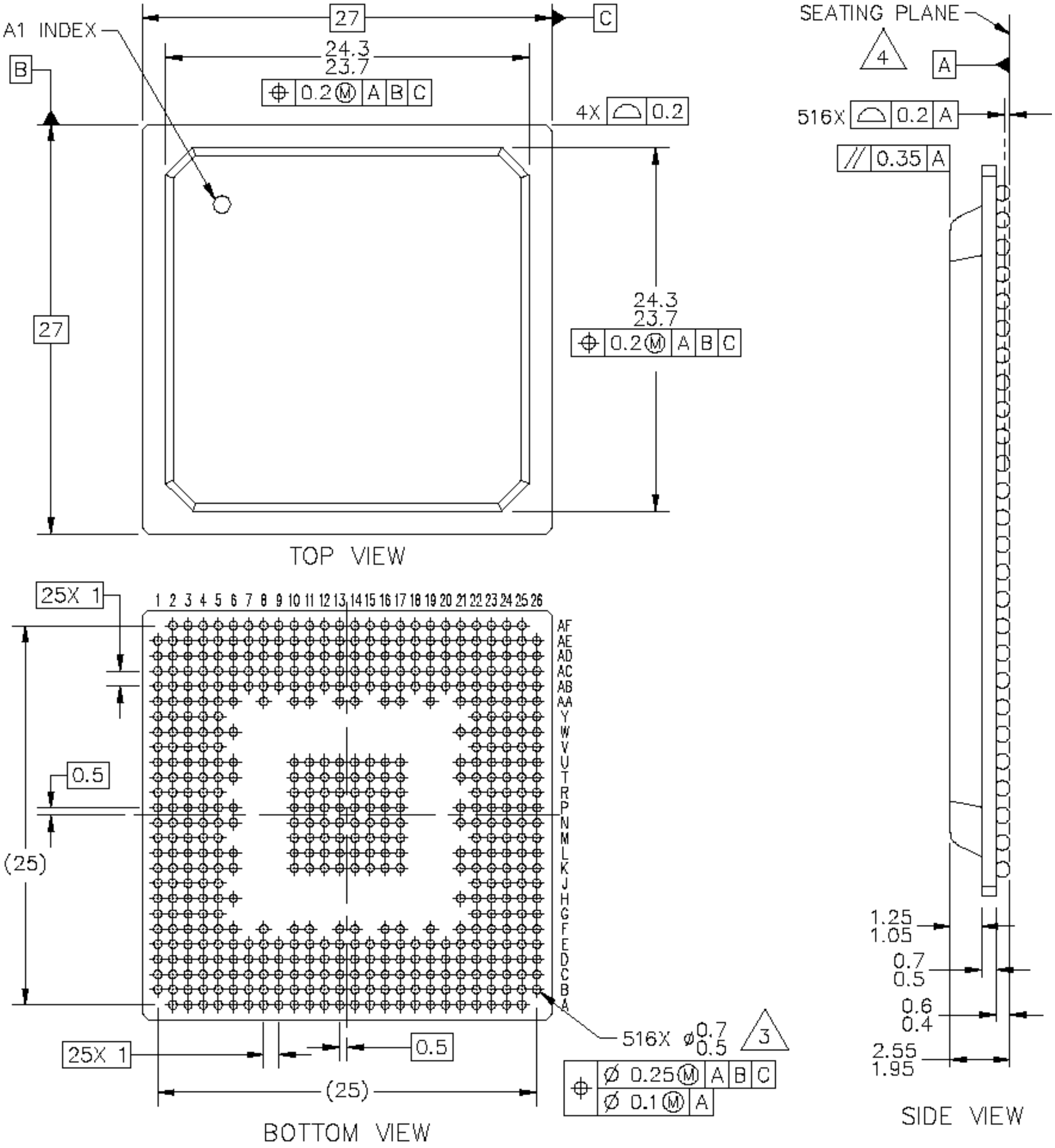


Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

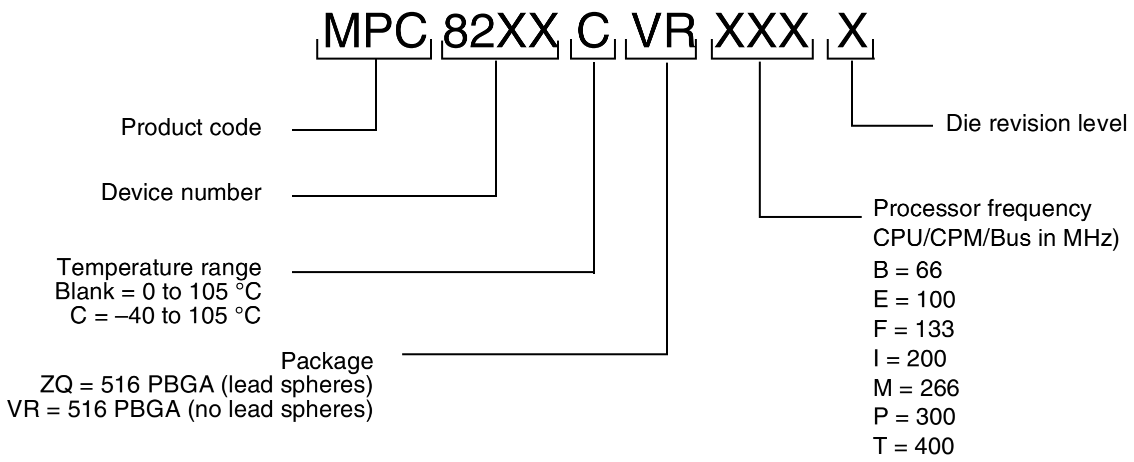


Figure 15. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
3	09/2011	In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
2	12/2008	• Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes. • In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.” • In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency. • Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.” • Removed overbar from DLL_ENABLE in Table 21, “Pinout.”
1.5	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.4	05/2006	• Added row for 133 MHz configurations to Table 8.
1.3	02/2006	• Inserted Section 6.3, “JTAG Timings.”