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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8247czqmiba">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8247czqmiba</a>

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 11. AC Characteristics for CPM Inputs<sup>1</sup>**

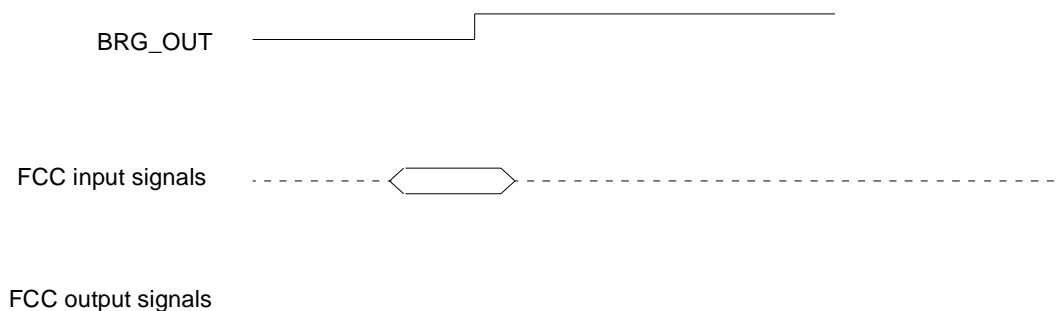
Spec Number		Characteristic	Value (ns)							
Setup	Hold		Setup				Hold			
			66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2.5	2	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	4	2	2	2	2
sp20	sp21	TDM inputs/SI	3	3	3	3	2.5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	8	0.5	0.5	0.5	0.5

<sup>1</sup> Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

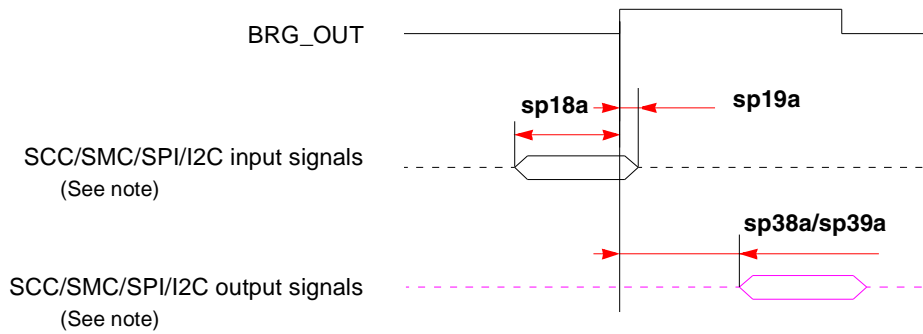
Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.



**Figure 3. FCC Internal Clock Diagram**

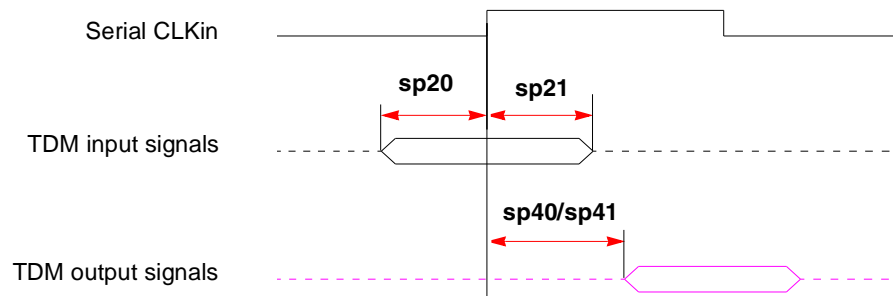
This figure shows the SCC/SMC/SPI/I<sup>2</sup>C internal clock.



- Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
  2. Input sampled on the rising edge and output driven on the falling edge.
  3. Input sampled on the falling edge and output driven on the falling edge.
  4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I<sup>2</sup>C Internal Clock Diagram**

This figure shows TDM input and output signals.



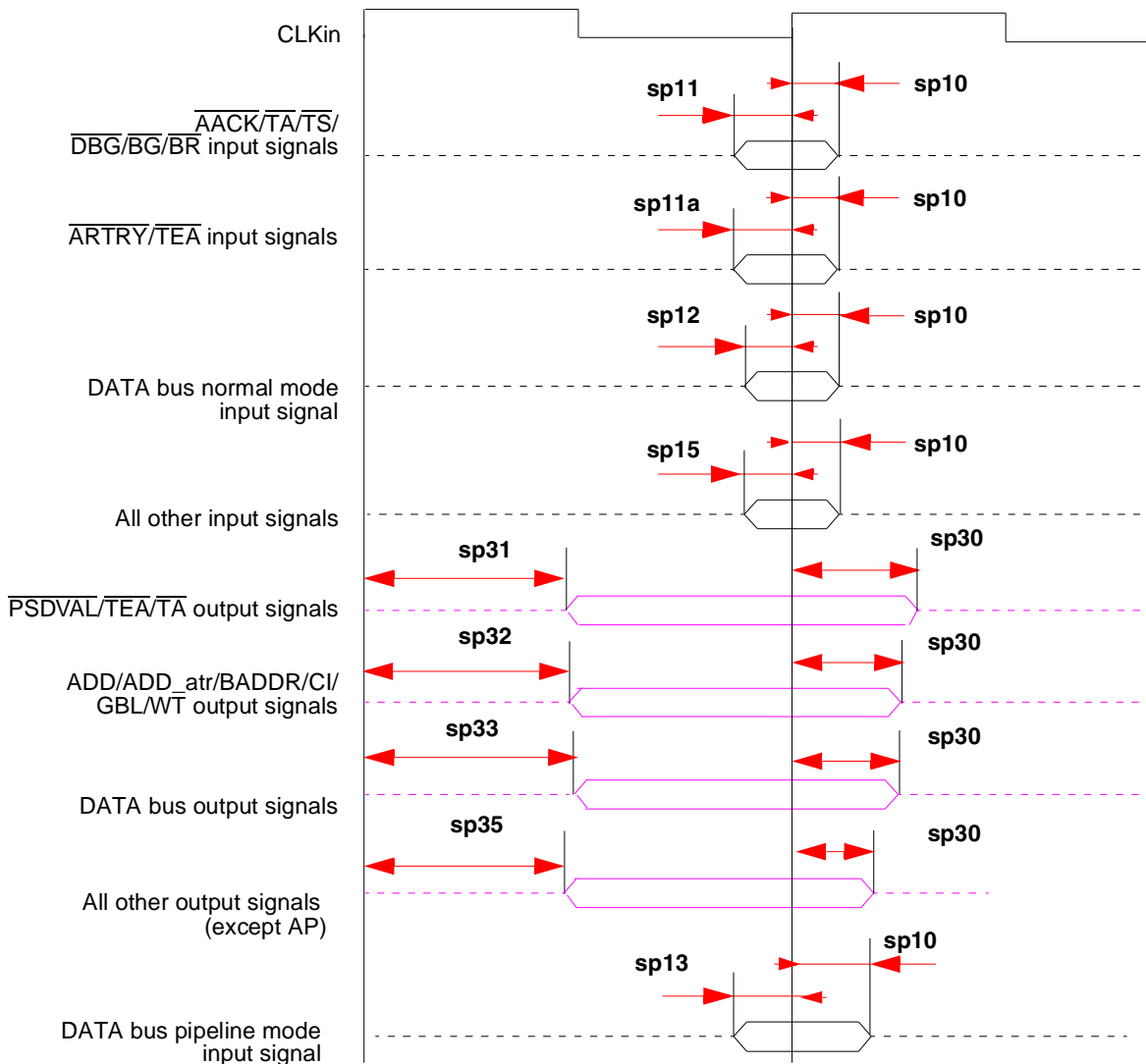
- Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
  2. Input sampled on the rising edge and output driven on the falling edge.
  3. Input sampled on the falling edge and output driven on the falling edge.
  4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

**NOTE**

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing.

This figure shows the interaction of several bus signals.



**Figure 9. Bus Signals**

This figure shows signal behavior in MEMC mode.

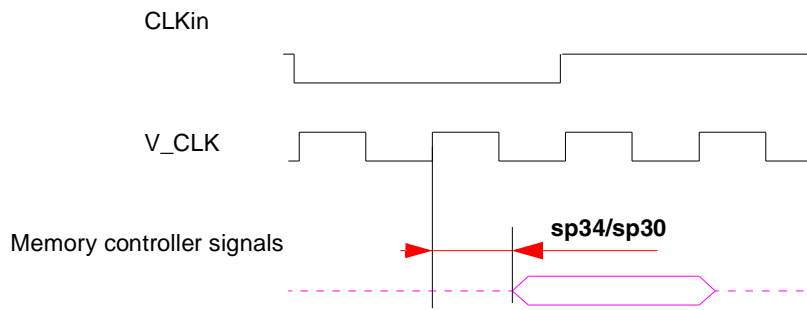


Figure 10. MEMC Mode Diagram

**NOTE**

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 14.

**Table 14. Tick Spacing for Memory Controller Signals**

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

This table is a representation of the information in Table 14.

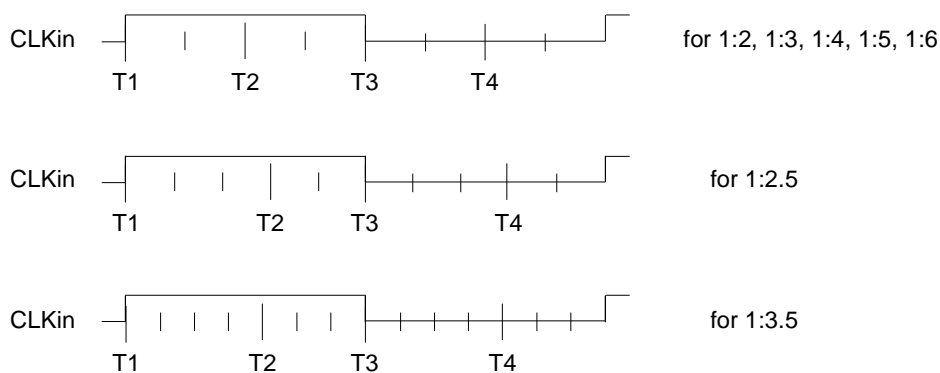


Figure 11. Internal Tick Spacing for Memory Controller Signals

**Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup>**

Mode <sup>3</sup>	Bus Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		PCI Division Factor <sup>6</sup>	PCI Clock (MHz)	
	MODCK_H-MODCK[1-3]	Low		High	Low		High	Low		High	Low
<b>Default Modes (MODCK_H=0000)</b>											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0000_011	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0000_100	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0000_101	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_110	50.0	66.7	3.5	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0000_111	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
<b>Full Configuration Modes</b>											
0001_000	50.0	66.7	3	150.0	200.0	5	250.0	333.3	3	50.0	66.7
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7
<b>Reserved</b>											
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
<b>Reserved</b>											
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
<b>Reserved</b>											
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
<b>Reserved</b>											
0100_000	Reserved										

**Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup> (continued)**

Mode <sup>3</sup>	Bus Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		PCI Division Factor <sup>6</sup>	PCI Clock (MHz)	
	MODCK_H-MODCK[1-3]	Low		High	Low		High	Low		High	Low
1000_010	66.7	88.9	3	200.0	266.6	3.5	233.3	311.1	4	50.0	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200.0	266.6	3.5	200.0	266.6	4	50.0	66.7
1001_011	57.1	76.2	3.5	200.0	266.6	4	228.6	304.7	4	50.0	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1010_101	100.0	133.3	2	200.0	266.6	2.5	250.0	333.3	4	50.0	66.7
1010_110	100.0	133.3	2	200.0	266.6	3	300.0	400.0	4	50.0	66.7
1010_111	100.0	133.3	2	200.0	266.6	3.5	350.0	466.6	4	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7

**Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup> (continued)**

Mode <sup>3</sup>	Bus Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		PCI Division Factor <sup>6</sup>	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
1011_100	80.0	106.7	2.5	200.0	266.6	4	320.0	426.6	4	50.0	66.7
1011_101	80.0	106.7	2.5	200.0	266.6	4.5	360.0	480.0	4	50.0	66.7
1101_000	100.0	133.3	2.5	250.0	333.3	3	300.0	400.0	5	50.0	66.7
1101_001	100.0	133.3	2.5	250.0	333.3	3.5	350.0	466.6	5	50.0	66.7
1101_010	100.0	133.3	2.5	250.0	333.3	4	400.0	533.3	5	50.0	66.7
1101_011	100.0	133.3	2.5	250.0	333.3	4.5	450.0	599.9	5	50.0	66.7
1101_100	100.0	133.3	2.5	250.0	333.3	5	500.0	666.6	5	50.0	66.7
1101_101	125.0	166.7	2	250.0	333.3	3	375.0	500.0	5	50.0	66.7
1101_110	125.0	166.7	2	250.0	333.3	4	500.0	666.6	5	50.0	66.7
1110_000	100.0	133.3	3	300.0	400.0	3.5	350.0	466.6	6	50.0	66.7
1110_001	100.0	133.3	3	300.0	400.0	4	400.0	533.3	6	50.0	66.7
1110_010	100.0	133.3	3	300.0	400.0	4.5	450.0	599.9	6	50.0	66.7
1110_011	100.0	133.3	3	300.0	400.0	5	500.0	666.6	6	50.0	66.7
1110_100	100.0	133.3	3	300.0	400.0	5.5	550.0	733.3	6	50.0	66.7
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

<sup>1</sup> The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

<sup>2</sup> PCI\_MODCK determines the PCI clock frequency range. See [Table 18](#) for lower range configurations.

<sup>3</sup> MODCK\_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

<sup>4</sup> CPM multiplication factor = CPM clock/bus clock

<sup>5</sup> CPU multiplication factor = Core PLL multiplication factor

<sup>6</sup> CPM\_CLK/PCI\_CLK ratio. When PCI\_MODCK = 0, the ratio of CPM\_CLK/PCI\_CLK should be calculated from SCCR[PCIDF] as follows:

$$\text{CPM\_CLK/PCI\_CLK} = (\text{PCIDF} + 1) / 2.$$



**Table 18. Clock Configurations for PCI Host Mode (PCI\_MODCK=1)<sup>1,2</sup>**

Mode <sup>3</sup>	Bus Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		PCI Division Factor <sup>6</sup>	PCI Clock (MHz)	
	MODCK_H-MODCK[1-3]	Low		High	Low		High	Low		High	Low
Default Modes (MODCK_H=0000)											
0000_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0000_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0000_010	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0000_011	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0000_100	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0000_101	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0000_110	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0000_111	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
Full Configuration Modes											
0001_000	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
0001_001	50.0	100.0	3	150.0	300.0	6	300.0	600.0	6	25.0	50.0
0001_010	50.0	100.0	3	150.0	300.0	7	350.0	700.0	6	25.0	50.0
0001_011	50.0	100.0	3	150.0	300.0	8	400.0	800.0	6	25.0	50.0
0010_000	50.0	100.0	4	200.0	400.0	5	250.0	500.0	8	25.0	50.0
0010_001	50.0	100.0	4	200.0	400.0	6	300.0	600.0	8	25.0	50.0
0010_010	50.0	100.0	4	200.0	400.0	7	350.0	700.0	8	25.0	50.0
0010_011	50.0	100.0	4	200.0	400.0	8	400.0	800.0	8	25.0	50.0
0010_100	37.5	75.0	4	150.0	300.0	5	187.5	375.0	6	25.0	50.0
0010_101	37.5	75.0	4	150.0	300.0	5.5	206.3	412.5	6	25.0	50.0
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										

Table 18. Clock Configurations for PCI Host Mode (PCI\_MODCK=1)<sup>1,2</sup> (continued)

Mode <sup>3</sup>	Bus Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		PCI Division Factor <sup>6</sup>	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

- <sup>6</sup> CPM\_CLK/PCI\_CLK ratio. When PCI\_MODCK = 1, the ratio of CPM\_CLK/PCI\_CLK should be calculated from PCIDF as follows:  
 PCIDF = 3 > CPM\_CLK/PCI\_CLK = 4  
 PCIDF = 5 > CPM\_CLK/PCI\_CLK = 6  
 PCIDF = 7 > CPM\_CLK/PCI\_CLK = 8  
 PCIDF = 9 > CPM\_CLK/PCI\_CLK = 5  
 PCIDF = B > CPM\_CLK/PCI\_CLK = 6

## 7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI agent mode the input clock is PCI clock.

**Table 19. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup>**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
<b>Default Modes (MODCK_H=0000)</b>											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0000_110	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
<b>Full Configuration Modes</b>											
0001_001	60.0	66.7	2	120.0	133.3	5	150.0	166.7	4	30.0	33.3
0001_010	50.0	66.7	2	100.0	133.3	6	150.0	200.0	4	25.0	33.3
0001_011	50.0	66.7	2	100.0	133.3	7	175.0	233.3	4	25.0	33.3
0001_100	50.0	66.7	2	100.0	133.3	8	200.0	266.6	4	25.0	33.3
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0010_011	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0

Table 19. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup> (continued)

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
0011_000	Reserved										
0011_001	Reserved										
0011_010	Reserved										
0011_011	Reserved										
0011_100	Reserved										
0100_000	Reserved										
0100_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0100_010	50.0	66.7	3	150.0	200.0	3.5	175.0	200.0	3	50.0	66.7
0100_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0100_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
0101_000	50.0	66.7	5	250.0	333.3	2.5	250.0	333.3	2.5	100.0	133.3
0101_001	50.0	66.7	5	250.0	333.3	3	300.0	400.0	2.5	100.0	133.3
0101_010	50.0	66.7	5	250.0	333.3	3.5	350.0	466.6	2.5	100.0	133.3
0101_011	50.0	66.7	5	250.0	333.3	4	400.0	533.3	2.5	100.0	133.3
0101_100	50.0	66.7	5	250.0	333.3	4.5	450.0	599.9	2.5	100.0	133.3
0101_101	50.0	66.7	5	250.0	333.3	5	500.0	666.6	2.5	100.0	133.3
0101_110	50.0	66.7	5	250.0	333.3	5.5	550.0	733.3	2.5	100.0	133.3
0110_000	Reserved										
0110_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
0110_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0110_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
0110_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
0111_000	50.0	66.7	3	150.0	200.0	2	150.0	200.0	2	75.0	100.0
0111_001	50.0	66.7	3	150.0	200.0	2.5	187.5	250.0	2	75.0	100.0
0111_010	50.0	66.7	3	150.0	200.0	3	225.0	300.0	2	75.0	100.0
0111_011	50.0	66.7	3	150.0	200.0	3.5	262.5	350.0	2	75.0	100.0

**Table 19. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup> (continued)**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
1000_000	Reserved										
1000_001	50.0	66.7	3	150.0	200.0	2.5	150.0	166.7	2.5	60.0	80.0
1000_010	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
1000_011	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
1000_100	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
1000_101	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0	266.6	4.5	225.0	300.0	4	50.0	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1011_101	50.0	66.7	4	200.0	266.6	2.5	250.0	333.3	2	100.0	133.3
1011_110	50.0	66.7	4	200.0	266.6	3	300.0	400.0	2	100.0	133.3
1011_111	50.0	66.7	4	200.0	266.6	3.5	350.0	466.6	2	100.0	133.3

**Table 20. Clock Configurations for PCI Agent Mode (PCI\_MODCK=1)<sup>1,2</sup>**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	MODCK_H-MODCK[1-3]	Low		High	Low		High	Low		High	Low
<b>Default Modes (MODCK_H=0000)</b>											
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
<b>Full Configuration Modes</b>											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
<b>Reserved</b>											
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
<b>Reserved</b>											
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
<b>Reserved</b>											
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
	$\overline{TS}$	D1
	A0	A3
	A1	B5
	A2	D8
	A3	C6
	A4	A4
	A5	A6
	A6	B6
	A7	C7
	A8	B7
	A9	A7
	A10	D9
	A11	E11
	A12	C9
	A13	B9
	A14	D11
	A15	A9
	A16	B10
	A17	A10
	A18	B11
	A19	A11
	A20	D12
	A21	A12
	A22	D13
	A23	B13
	A24	C13
	A25	C14
	A26	B14
	A27	D14
	A28	E14
	A29	A14

**Table 21. Pinout (continued)**

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
	A30	B15
	A31	A15
	TT0	B3
	TT1	E8
	TT2	D7
	TT3	C4
	TT4	E7
	$\overline{\text{TBST}}$	E3
	TSIZ0	E4
	TSIZ1	E5
	TSIZ2	C3
	TSIZ3	D5
	$\overline{\text{AACK}}$	D3
	$\overline{\text{ARTRY}}$	C2
	$\overline{\text{DBG/IRQ7}}$	F16
	$\overline{\text{DBB/IRQ3}}$	D18
	D0	AC1
	D1	AA1
	D2	V3
	D3	R5
	D4	P4
	D5	M4
	D6	J4
	D7	G1
	D8	W6
	D9	Y3
	D10	V1
	D11	N6
	D12	P3
	D13	M2
	D14	J5



Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
	D15	G3
	D16	AB3
	D17	Y1
	D18	T4
	D19	T3
	D20	P2
	D21	M1
	D22	J1
	D23	G4
	D24	AB2
	D25	W4
	D26	V2
	D27	T1
	D28	N5
	D29	L1
	D30	H1
	D31	G5
	D32	W5
	D33	W2
	D34	T5
	D35	T2
	D36	N1
	D37	K3
	D38	H2
	D39	F1
	D40	AA2
	D41	W1
	D42	U3
	D43	R2
	D44	N2
	D45	L2

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D46		H4
D47		F2
D48		AB1
D49		U4
D50		U1
D51		R3
D52		N3
D53		K2
D54		H5
D55		F4
D56		AA3
D57		U5
D58		U2
D59		P5
D60		M3
D61		K4
D62		H3
D63		E1
$\overline{\text{IRQ3}}/\text{CKSTP\_OUT}/\text{EXT\_BR3}$		B16
$\overline{\text{IRQ4}}/\text{CORE\_SRESET}/\text{EXT\_BG3}$		C15
$\overline{\text{IRQ5}}/\text{TBEN}/\text{EXT\_DBG3}/\text{CINT}$		Y4
$\overline{\text{PSDVAL}}$		C19
$\overline{\text{TA}}$		AA4
$\overline{\text{TEA}}$		AB6
$\overline{\text{GBL}}/\text{IRQ1}$		D15
$\overline{\text{CI}}/\text{BADDR29}/\text{IRQ2}$		D16
$\overline{\text{WT}}/\text{BADDR30}/\text{IRQ3}$		C16
$\text{BADDR31}/\text{IRQ5}/\text{CINT}$		E17
$\overline{\text{CPU\_BR}}/\text{INT\_OUT}$		B20
$\overline{\text{CS0}}$		AE6
$\overline{\text{CS1}}$		AD7

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
	$\overline{CS2}$	AF5
	$\overline{CS3}$	AC8
	$\overline{CS4}$	AF6
	$\overline{CS5}$	AD8
	$\overline{CS6/BCTL1/SMI}$	AC9
	$\overline{CS7/TLBISYNC}$	AB9
	BADDR27/ $\overline{IRQ1}$	AB8
	BADDR28/ $\overline{IRQ2}$	AC7
	ALE/ $\overline{IRQ4}$	AF4
	$\overline{BCTL0}$	AF3
	$\overline{PWE0/PSDDQM0/PBS0}$	AD6
	$\overline{PWE1/PSDDQM1/PBS1}$	AE5
	$\overline{PWE2/PSDDQM2/PBS2}$	AE3
	$\overline{PWE3/PSDDQM3/PBS3}$	AF2
	$\overline{PWE4/PSDDQM4/PBS4}$	AC6
	$\overline{PWE5/PSDDQM5/PBS5}$	AC5
	$\overline{PWE6/PSDDQM6/PBS6}$	AD4
	$\overline{PWE7/PSDDQM7/PBS7}$	AB5
	PSDA10/PGPL0	AE2
	$\overline{PSDWE/PGPL1}$	AD3
	$\overline{POE/PSDRAS/PGPL2}$	AB4
	$\overline{PSDCAS/PGPL3}$	AC3
	$\overline{PGTA/PUPMWAIT/PGPL4}$	AD2
	PSDAMUX/PGPL5	AC2
	$\overline{PCI\_MODE^1}$	AD22
	PCI_CFG0 ( $\overline{PCI\_HOST\_EN}$ )	AC21
	PCI_CFG1 ( $\overline{PCI\_ARB\_EN}$ )	AE22
	PCI_CFG2 (DLL_ENABLE)	AE23
	PCI_PAR	AF12
	$\overline{PCI\_FRAME}$	AD15
	$\overline{PCI\_TRDY}$	AF16

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UT\_TXENB}}$	G22 <sup>3</sup>
PB18/FCC2_MII_HDLC_RXD3		T25 <sup>3</sup>
PB19/FCC2_MII_HDLC_RXD2		P22 <sup>3</sup>
PB20/FCC2_MII_HDLC_RMII_RXD1		L25 <sup>3</sup>
PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD		J26 <sup>3</sup>
PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0		U23 <sup>3</sup>
PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1		U26 <sup>3</sup>
PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2		M24 <sup>3</sup>
PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2		M23 <sup>3</sup>
PB26/FCC2_MII_CRS/L1RXDB2		H24 <sup>3</sup>
PB27/FCC2_MII_COL/L1TXDB2		E25 <sup>3</sup>
PB28/FCC2_MII_RMII_RX_ER/ $\overline{\text{FCC2\_RTS}}$ /TXD1		D26 <sup>3</sup>
PB29/FCC2_MII_RMII_TX_EN		K21 <sup>3</sup>
PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV		D24 <sup>3</sup>
PB31/FCC2_MII_TX_ER		E23 <sup>3</sup>
PC0/ $\overline{\text{DREQ3}}$ /BRGO7/ $\overline{\text{SMSYN1}}$ /L1CLKOA2		AF23 <sup>3</sup>
PC1/BRGO6/ $\overline{\text{L1RQA2}}$		AD23 <sup>3</sup>
PC4/SMRXD1/SI2_L1ST4/ $\overline{\text{FCC2\_CD}}$		AB22 <sup>3</sup>
PC5/SMTXD1/SI2_L1ST3/ $\overline{\text{FCC2\_CTS}}$		AE24 <sup>3</sup>
PC6/ $\overline{\text{FCC1\_CD}}$ /SI2_L1ST2	FCC1_UT_RXADDR2	AF24 <sup>3</sup>
PC7/ $\overline{\text{FCC1\_CTS}}$	FCC1_UT_TXADDR2	AE26 <sup>3</sup>
PC8/ $\overline{\text{CD4}}$ /RTS1/SI2_L1ST2/ $\overline{\text{CTS3}}$		AC24 <sup>3</sup>
PC9/ $\overline{\text{CTS4}}$ /L1TSYNCA2		AA23 <sup>3</sup>
PC10/ $\overline{\text{CD3}}$ /USB_RN		AB25 <sup>3</sup>
PC11/ $\overline{\text{CTS3}}$ /USB_RP/L1TXD3A2		V22 <sup>3</sup>
PC12	FCC1_UT_RXADDR1	AA26 <sup>3</sup>
PC13/BRGO5	FCC1_UT_TXADDR1	V23 <sup>3</sup>
PC14/ $\overline{\text{CD1}}$	FCC1_UT_RXADDR0	W24 <sup>3</sup>
PC15/ $\overline{\text{CTS1}}$	FCC1_UT_TXADDR0	U24 <sup>3</sup>
PC16/CLK16		T23 <sup>3</sup>

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
1.2	09/2005	<ul style="list-style-type: none"> <li>Added 133-MHz to the list of frequencies in the opening sentence of <a href="#">Section 6, “AC Electrical Characteristics”</a>.</li> <li>Added 133 MHz columns to <a href="#">Table 9</a>, <a href="#">Table 11</a>, <a href="#">Table 12</a>, and <a href="#">Table 13</a>.</li> <li>Added footnote 2 to <a href="#">Table 13</a>.</li> <li>Added the conditions note directly above <a href="#">Table 12</a>.</li> </ul>
1.1	01/2005	<ul style="list-style-type: none"> <li>Modification for correct display of assertion level (“<math>\overline{\text{overbar}}</math>”) for some signals</li> </ul>
1.0	12/2004	<ul style="list-style-type: none"> <li>Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values</li> <li>Section 2: removed voltage tracking note</li> <li><a href="#">Table 3</a>: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset</li> <li><a href="#">Table 4</a>: Updated VDD and VCCSYN to 1.425 V - 1.575 V</li> <li><a href="#">Table 8</a>: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed.</li> <li>Section 4.6: Updated description of layout practices</li> <li><a href="#">Table 8</a>: Note 3 added regarding IIC compatibility</li> <li><a href="#">Table 8</a>: Updated nominal and maximum power dissipation values</li> <li><a href="#">Table 9</a>: updated PCI impedance to 27 <math>\Omega</math>, updated 60x and MEMC values and added note to reflect configurable impedance</li> <li>Section 6: Added sentence providing derating factor</li> <li>Section 6.1: added Note: Rise/Fall Time on CPM Input Pins</li> <li><a href="#">Table 9</a>: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a</li> <li><a href="#">Table 11</a>: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22</li> <li>Section 6.2: added spread spectrum clocking note</li> <li>Section 6.2: added CLKIN jitter note</li> <li><a href="#">Table 12</a>: combined specs sp11 and sp11a</li> <li><a href="#">Table 13</a>: sp30 Data Bus minimum delay values changed to 0.8</li> <li>Section 7: unit of ns added to Tval notes</li> <li>Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.</li> <li><a href="#">Section 7, “Clock Configuration Modes”</a>: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.</li> <li><a href="#">Table 21</a>: correct superscript of footnote number after pin AD22</li> <li><a href="#">Table 21</a>: remove DONE3 from PC12</li> <li><a href="#">Table 21</a>: signals referring to TDMs C2 and D2 removed</li> </ul>