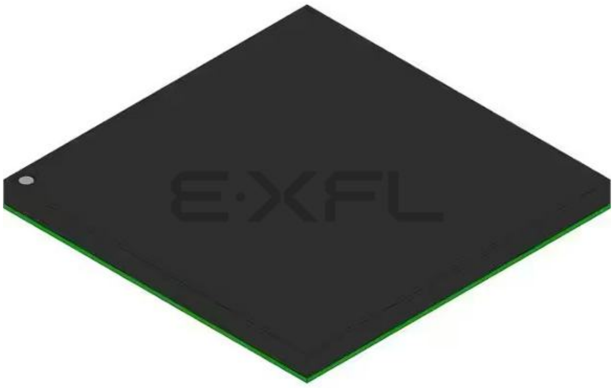

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8247vrmiba

1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

Table 1. MPC8272 PowerQUICC II Family Functionality

Functionality	SoCs			
	MPC8272	MPC8248	MPC8271	MPC8247
Package[1]	516 PBGA			
Serial communications controllers (SCCs)	3	3	3	3
QUICC multi-channel controller (QMC)	Yes	Yes	Yes	Yes
Fast communication controllers (FCCs)	2	2	2	2
I-Cache (Kbyte)	16	16	16	16
D-Cache (Kbyte)	16	16	16	16
Ethernet (10/100)	2	2	2	2
UTOPIA II Ports	1	0	1	0
Multi-channel controllers (MCCs)	0	0	0	0
PCI bridge	Yes	Yes	Yes	Yes
Transmission convergence (TC) layer	—	—	—	—
Inverse multiplexing for ATM (IMA)	—	—	—	—
Universal serial bus (USB) 2.0 full/low rate	1	1	1	1
Security engine (SEC)	Yes	Yes	—	—

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

Table 2. MPC8272 PowerQUICC II Device Packages

Code (Package)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8272VR	MPC8272ZQ
	MPC8248VR	MPC8248ZQ
	MPC8271VR	MPC8271ZQ
	MPC8247VR	MPC8247ZQ

- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
  - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
  - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
  - Microcode tracing capabilities
  - Eight CPM trap registers
- Universal serial bus (USB) controller
  - Supports USB 2.0 full/low rate compatible
  - USB host mode
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
  - Supports USB slave mode
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Two fast communication controllers (FCCs) supporting the following protocols:
    - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—up to T3 rates (clear channel)

4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature (ºC)
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 11. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Value (ns)							
			Setup				Hold			
Setup	Hold		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2.5	2	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	4	2	2	2	2
sp20	sp21	TDM inputs/SI	3	3	3	3	2.5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	8	0.5	0.5	0.5	0.5

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

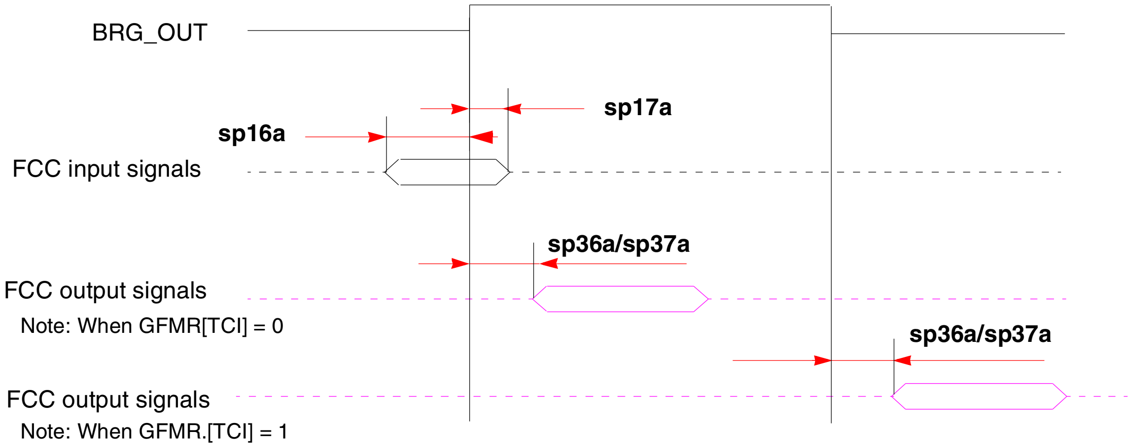


Figure 3. FCC Internal Clock Diagram

This figure shows signal behavior in MEMC mode.

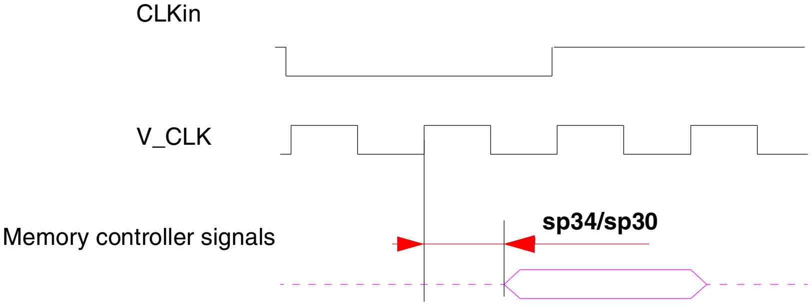


Figure 10. MEMC Mode Diagram

NOTE

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 14.

Table 14. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

This table is a representation of the information in Table 14.

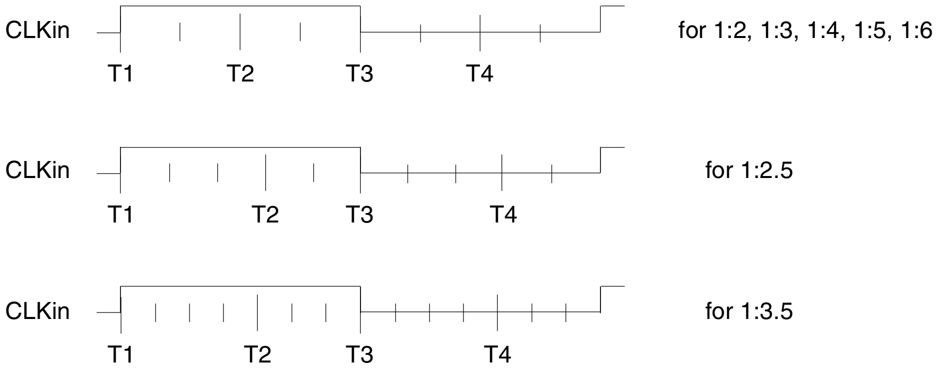


Figure 11. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin’s rising edge.

6.3 JTAG Timings

This table lists the JTAG timings.

Table 15. JTAG Timings[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times					
Boundary-scan data	t_{JTDVKH}	4	—	ns	4, 7
TMS, TDI	t_{JTIVKH}	4	—	ns	4, 7
Input hold times					
Boundary-scan data	t_{JTDXKH}	10	—	ns	4, 7
TMS, TDI	t_{JTIXKH}	10	—	ns	4, 7
Output valid times					
Boundary-scan data	t_{JTKLDV}	—	10	ns	5, 7
TDO	t_{JTKLOV}	—	10	ns	5. 7
Output hold times					
Boundary-scan data	t_{JTKLDX}	1	—	ns	5, 7
TDO	t_{JTKLOX}	1	—	ns	5, 7
JTAG external clock to output high impedance					
Boundary-scan data	t_{JTKLDZ}	1	10	ns	5, 6
TDO	t_{JTKLOZ}	1	10	ns	5, 6

[1] All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

[2] The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

[3] TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

[4] Non-JTAG signal input timing with respect to t_{TCLK}.

[5] Non-JTAG signal output timing with respect to t_{TCLK}.

[6] Guaranteed by design.

[7] Guaranteed by design and device characterization.

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_010	66.7	88.9	3	200.0	266.6	3.5	233.3	311.1	4	50.0	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200.0	266.6	3.5	200.0	266.6	4	50.0	66.7
1001_011	57.1	76.2	3.5	200.0	266.6	4	228.6	304.7	4	50.0	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1010_101	100.0	133.3	2	200.0	266.6	2.5	250.0	333.3	4	50.0	66.7
1010_110	100.0	133.3	2	200.0	266.6	3	300.0	400.0	4	50.0	66.7
1010_111	100.0	133.3	2	200.0	266.6	3.5	350.0	466.6	4	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2]

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0000_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0000_010	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0000_011	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0000_100	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0000_101	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0000_110	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0000_111	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
Full Configuration Modes											
0001_000	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
0001_001	50.0	100.0	3	150.0	300.0	6	300.0	600.0	6	25.0	50.0
0001_010	50.0	100.0	3	150.0	300.0	7	350.0	700.0	6	25.0	50.0
0001_011	50.0	100.0	3	150.0	300.0	8	400.0	800.0	6	25.0	50.0
0010_000	50.0	100.0	4	200.0	400.0	5	250.0	500.0	8	25.0	50.0
0010_001	50.0	100.0	4	200.0	400.0	6	300.0	600.0	8	25.0	50.0
0010_010	50.0	100.0	4	200.0	400.0	7	350.0	700.0	8	25.0	50.0
0010_011	50.0	100.0	4	200.0	400.0	8	400.0	800.0	8	25.0	50.0
0010_100	37.5	75.0	4	150.0	300.0	5	187.5	375.0	6	25.0	50.0
0010_101	37.5	75.0	4	150.0	300.0	5.5	206.3	412.5	6	25.0	50.0
0010_110	37.5	75.0	4	150.0	300.0	6	225.0	450.0	6	25.0	50.0
0011_000	30.0	50.0	5	150.0	250.0	5	150.0	250.0	5	30.0	50.0
0011_001	25.0	50.0	5	125.0	250.0	6	150.0	300.0	5	25.0	50.0
0011_010	25.0	50.0	5	125.0	250.0	7	175.0	350.0	5	25.0	50.0
0011_011	25.0	50.0	5	125.0	250.0	8	200.0	400.0	5	25.0	50.0
0100_000	Reserved										

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7
1110_011	50.0	66.7	5	250.0	333.3	4	500.0	666.6	2	125.0	166.7
1110_100	50.0	66.7	5	250.0	333.3	4	333.3	444.4	3	83.3	111.1
1110_101	50.0	66.7	5	250.0	333.3	4.5	375.0	500.0	3	83.3	111.1
1110_110	50.0	66.7	5	250.0	333.3	5	416.7	555.5	3	83.3	111.1
1110_111	50.0	66.7	5	250.0	333.3	5.5	458.3	611.1	3	83.3	111.1
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

[1] The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

[2] PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower range configurations.

[3] MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

[4] CPM multiplication factor = CPM clock/bus clock

[5] CPU multiplication factor = Core PLL multiplication factor

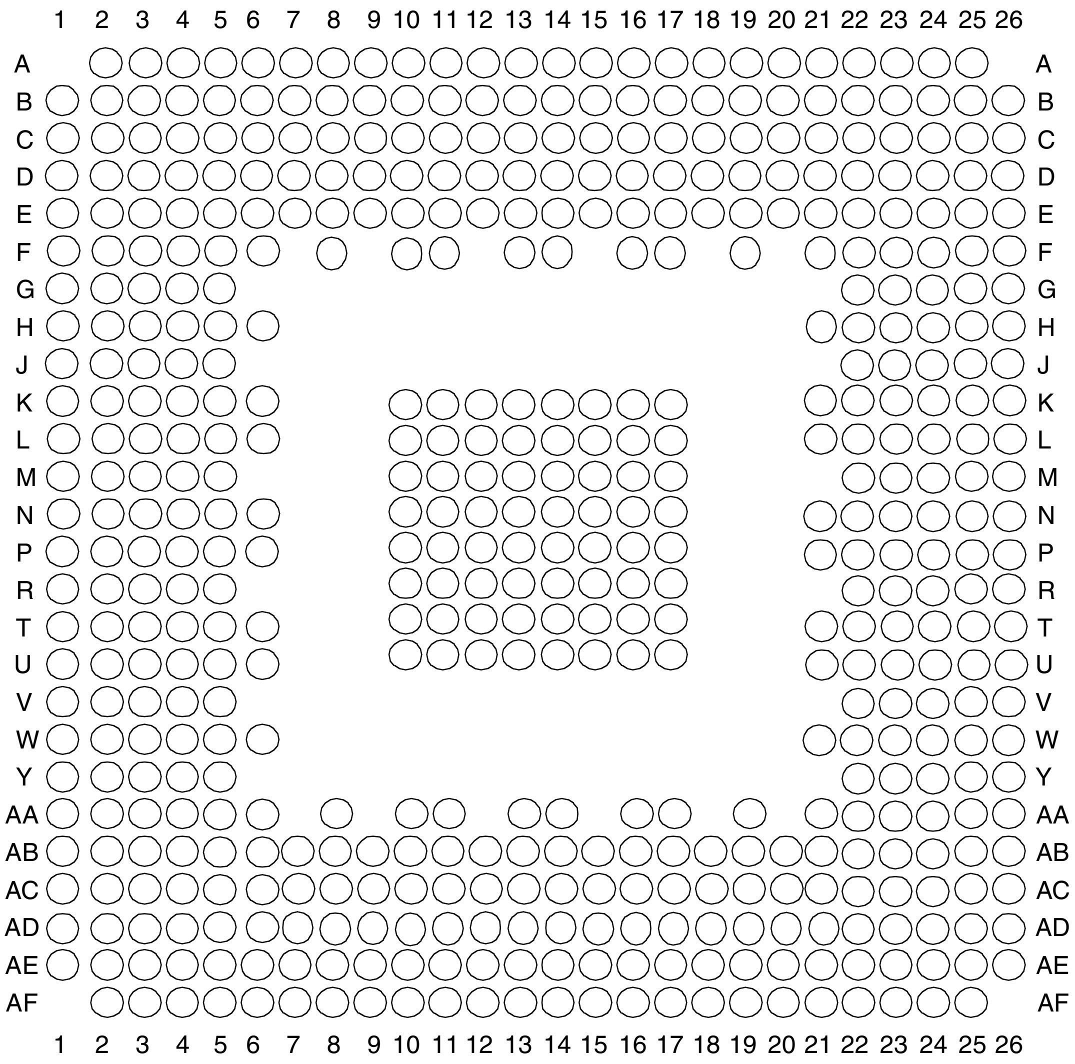
Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0100_100	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
0101_000	30.0	50.0	5	150.0	250.0	2.5	150.0	250.0	2.5	60.0	100.0
0101_001	25.0	50.0	5	125.0	250.0	3	150.0	300.0	2.5	50.0	100.0
0101_010	25.0	50.0	5	125.0	250.0	3.5	175.0	350.0	2.5	50.0	100.0
0101_011	25.0	50.0	5	125.0	250.0	4	200.0	400.0	2.5	50.0	100.0
0101_100	25.0	50.0	5	125.0	250.0	4.5	225.0	450.0	2.5	50.0	100.0
0101_101	25.0	50.0	5	125.0	250.0	5	250.0	500.0	2.5	50.0	100.0
0101_110	25.0	50.0	5	125.0	250.0	5.5	275.0	550.0	2.5	50.0	100.0
0110_000	Reserved										
0110_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
0110_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0110_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
0110_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
0111_000	25.0	50.0	6	150.0	300.0	2	150.0	300.0	2	75.0	150.0
0111_001	25.0	50.0	6	150.0	300.0	2.5	187.5	375.0	2	75.0	150.0
0111_010	25.0	50.0	6	150.0	300.0	3	225.0	450.0	2	75.0	150.0
0111_011	25.0	50.0	6	150.0	300.0	3.5	262.5	525.0	2	75.0	150.0
1000_000	Reserved										
1000_001	25.0	50.0	6	150.0	300.0	2.5	150.0	300.0	2.5	60.0	120.0
1000_010	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
1000_011	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1000_100	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1000_101	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1001_000	Reserved										
1001_001	Reserved										

This figure shows the pinout of the 516 PBGA package as viewed from the top surface.



Not to Scale

Figure 12. Pinout of the 516 PBGA Package (View from Top)

This table lists the pins of the MPC8272. Note that the pins in the “MPC8272/8271 Only” column relate to Utopia functionality.

Table 21. Pinout

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
$\overline{\text{BR}}$		A19
$\overline{\text{BG}}$/$\overline{\text{IRQ6}}$		D2
$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$		C1

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D46		H4
D47		F2
D48		AB1
D49		U4
D50		U1
D51		R3
D52		N3
D53		K2
D54		H5
D55		F4
D56		AA3
D57		U5
D58		U2
D59		P5
D60		M3
D61		K4
D62		H3
D63		E1
$\overline{\text{IRQ3}}$/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$		B16
$\overline{\text{IRQ4}}$/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$		C15
$\overline{\text{IRQ5}}$/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$/$\overline{\text{CINT}}$		Y4
$\overline{\text{PSDVAL}}$		C19
$\overline{\text{TA}}$		AA4
$\overline{\text{TEA}}$		AB6
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		D15
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		D16
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		C16
BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		E17
$\overline{\text{CPU\_BR}}$/$\overline{\text{INT\_OUT}}$		B20
$\overline{\text{CS0}}$		AE6
$\overline{\text{CS1}}$		AD7

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
MODCK1/$\overline{\text{RSRV}}$/TC0/BNKSEL0		A20
MODCK2/CSE0/TC1/BNKSEL1		C20
MODCK3/CSE1/TC2/BNKSEL2		A21
CLKIN1		D21
PA8/SMRXD2		AF25[3]
PA9/SMTXD2		AA22[3]
PA10/MSNUM5	FCC1_UT_RXD0	AB23[3]
PA11/MSNUM4	FCC1_UT_RXD1	AD26[3]
PA12/MSNUM3	FCC1_UT_RXD2	AD25[3]
PA13/MSNUM2	FCC1_UT_RXD3	AA24[3]
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT_RXD4	W22[3]
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT_RXD5	Y24[3]
PA16/FCC1_MII_HDLC_RXD1	FCC1_UT_RXD6	T22[3]
PA17/FCC1_MII_HDLC_RXD0/FCC1_MII_TRAN_RXD/FCC1_RMII_RXD0	FCC1_UT_RXD7	W26[3]
PA18/FCC1_MII_HDLC_TXD0/FCC1_MII_TRAN_TXD/FCC1_RMII_TXD0	FCC1_UT_TXD7	V26[3]
PA19/FCC1_MII_HDLC_TXD1/FCC1_RMII_TXD1	FCC1_UT_TXD6	R23[3]
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT_TXD5	P25[3]
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT_TXD4	N22[3]
PA22	FCC1_UT_TXD3	N26[3]
PA23	FCC1_UT_TXD2	N23[3]
PA24/MSNUM1	FCC1_UT_TXD1	H26[3]
PA25/MSNUM0	FCC1_UT_TXD0	G25[3]
PA26/FCC1_MII_RMIIRX_ER	FCC1_UT_RXCLAV	L22[3]
PA27/FCC1_MII_RX_DV/FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	G24[3]
PA28/FCC1_MII_RMII_TX_EN	FCC1_UT_RXENB	G23[3]
PA29/FCC1_MII_TX_ER	$\overline{\text{FCC1\_UT\_TXSOC}}$	B26[3]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	FCC1_UT_TXCLAV	A25[3]

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
PA31/FCC1_MII_COL	FCC1_UT_TXENB	G22[3]
PB18/FCC2_MII_HDLC_RXD3		T25[3]
PB19/FCC2_MII_HDLC_RXD2		P22[3]
PB20/FCC2_MII_HDLC_RMII_RXD1		L25[3]
PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD		J26[3]
PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0		U23[3]
PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1		U26[3]
PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2		M24[3]
PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2		M23[3]
PB26/FCC2_MII_CRS/L1RXDB2		H24[3]
PB27/FCC2_MII_COL/L1TXDB2		E25[3]
PB28/FCC2_MII_RMII_RX_ER/FCC2_RTS/TXD1		D26[3]
PB29/FCC2_MII_RMII_TX_EN		K21[3]
PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV		D24[3]
PB31/FCC2_MII_TX_ER		E23[3]
PC0/DREQ3/BRGO7/SMSYN1/L1CLKOA2		AF23[3]
PC1/BRGO6/L1RQA2		AD23[3]
PC4/SMRXD1/SI2_L1ST4/FCC2_CD		AB22[3]
PC5/SMTXD1/SI2_L1ST3/FCC2_CTS		AE24[3]
PC6/FCC1_CD/SI2_L1ST2	FCC1_UT_RXADDR2	AF24[3]
PC7/FCC1_CTS	FCC1_UT_TXADDR2	AE26[3]
PC8/CD4/RTS1/SI2_L1ST2/CTS3		AC24[3]
PC9/CTS4/L1TSYNCA2		AA23[3]
PC10/CD3/USB_RN		AB25[3]
PC11/CTS3/USB_RP/L1TXD3A2		V22[3]
PC12	FCC1_UT_RXADDR1	AA26[3]
PC13/BRGO5	FCC1_UT_TXADDR1	V23[3]
PC14/CD1	FCC1_UT_RXADDR0	W24[3]
PC15/CTS1	FCC1_UT_TXADDR0	U24[3]
PC16/CLK16		T23[3]

9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

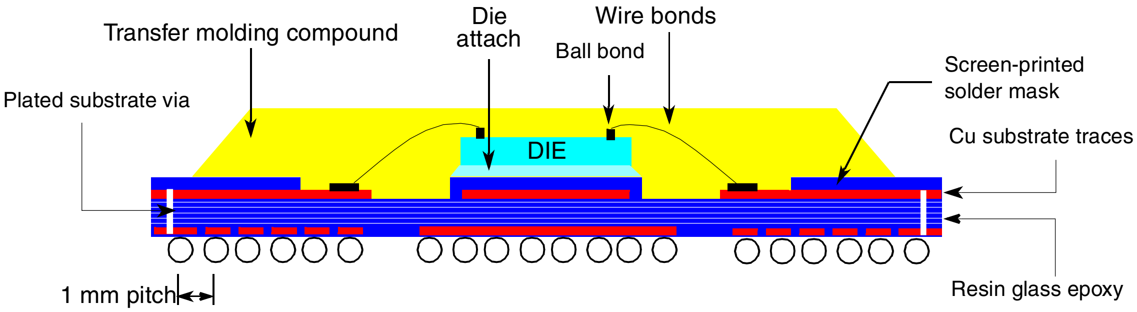


Figure 13. Side View of the PBGA Package Remove

9.1 Package Parameters

This table provides package parameters.

Table 22. Package Parameters

Code	Type	Outline (mm)	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
VR, ZQ	PBGA	27 x 27	516	1	2.25

NOTE: Temperature Reflow for the VR Package

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

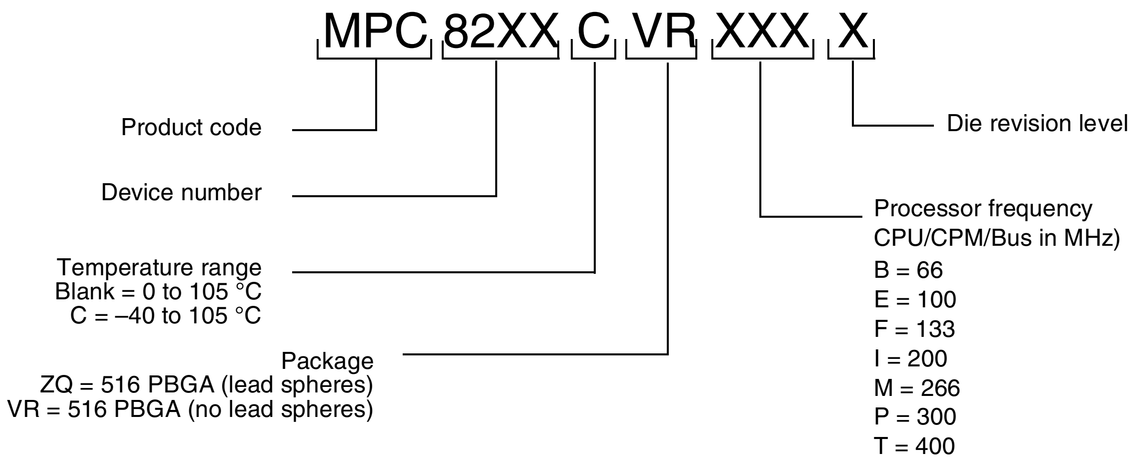


Figure 15. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
3	09/2011	In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
2	12/2008	• Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes. • In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.” • In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency. • Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.” • Removed overbar from DLL_ENABLE in Table 21, “Pinout.”
1.5	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.4	05/2006	• Added row for 133 MHz configurations to Table 8.
1.3	02/2006	• Inserted Section 6.3, “JTAG Timings.”

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
1.2	09/2005	• Added 133-MHz to the list of frequencies in the opening sentence of Section 6, “AC Electrical Characteristics”. • Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13. • Added footnote 2 to Table 13. • Added the conditions note directly above Table 12.
1.1	01/2005	• Modification for correct display of assertion level (“$\overline{\text{overbar}}$”) for some signals
1.0	12/2004	• Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values • Section 2: removed voltage tracking note • Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset • Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V • Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed. • Section 4.6: Updated description of layout practices • Table 8: Note 3 added regarding IIC compatibility • Table 8: Updated nominal and maximum power dissipation values • Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance • Section 6: Added sentence providing derating factor • Section 6.1: added Note: Rise/Fall Time on CPM Input Pins • Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a • Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22 • Section 6.2: added spread spectrum clocking note • Section 6.2: added CLKIN jitter note • Table 12: combined specs sp11 and sp11a • Table 13: sp30 Data Bus minimum delay values changed to 0.8 • Section 7: unit of ns added to Tval notes • Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. • Section 7, “Clock Configuration Modes”: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. • Table 21: correct superscript of footnote number after pin AD22 • Table 21: remove DONE3 from PC12 • Table 21: signals referring to TDMs C2 and D2 removed

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.2	12/2003	• Table 1: New • Table 2: New • Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V • Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) • Table 8 and Table 21: Addition of muxed signals CPCI_HS_ES to PCI_REQ1 (AF14) CPCI_HS_LED to PCI_GNT1 (AE13) CPCI_HS_ENUM to PCI_GNT2 (AF21) • Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices: PCI_CFG0 (PCI_HOST_EN) (AC21) PCI_CFG1 (PCI_ARB_EN) (AE22) PCI_CFG2 (DLL_ENABLE) (AE23) PCI_PAR (AF12) PCI_FRAME (AD15) PCI_TRDY(AF16) PCI_IRDY (AF15) PCI_STOP (AE15) DEVSEL (AE14) PCI_IDSEL (AC17) PCI_PERR (AD14) PCI_SERR (AD13) PCI_REQ0–2 (AAE20, AF14, AB14) PCI_GNT0–2 (AD20, AE13, AF21) PCI_RST (AF22) PCI_INTA (AE21) PCI_C0-3 (AE12, AF13, AC15, AE18) PCI_AD0-31 • Table 8 and Table 21: Corrected assertion level (added “‾“) PCI_HOST_EN (AC21) and PCI_ARB_EN (AE22) • Table 7: Addition of $R_{\theta JT}$ and note 4 • Sections 4.1–4.5 and 4.7 on thermal characteristics: New • Section 7, “Clock Configuration Modes”: Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family. • Addition of “Note: Temperature Reflow for the VR Package" on page 56 • Table 21: Addition of note 2 to TRST (E21) and PORESET (C24) • Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now “No connects.” Note 4 unchanged. • Table 21: Removal of Spare0 (AD24). This pin is now a “No connect.” Note 5 unchanged. • Table 21: Addition of PCI_MODE (AD22). This pin was previously listed as “Ground.” Addition of note 1.
0.1	9/2003	• Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine) • Table 8: Addition of note 2 to V_{IH} • Table 8: Changed I_{OL} for 60x signals to 6.0 mA • Modification of note 1 for Table 17, Table 18, Table 19, and Table 20 • Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both CS5 and GND. AD8 is only assigned to CS5. • Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3) • Addition of ZQ package code to Figure 15
0	5/2003	NDA release