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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8247zqtmfa

1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

Table 1. MPC8272 PowerQUICC II Family Functionality

Functionality	SoCs			
	MPC8272	MPC8248	MPC8271	MPC8247
Package[1]	516 PBGA			
Serial communications controllers (SCCs)	3	3	3	3
QUICC multi-channel controller (QMC)	Yes	Yes	Yes	Yes
Fast communication controllers (FCCs)	2	2	2	2
I-Cache (Kbyte)	16	16	16	16
D-Cache (Kbyte)	16	16	16	16
Ethernet (10/100)	2	2	2	2
UTOPIA II Ports	1	0	1	0
Multi-channel controllers (MCCs)	0	0	0	0
PCI bridge	Yes	Yes	Yes	Yes
Transmission convergence (TC) layer	—	—	—	—
Inverse multiplexing for ATM (IMA)	—	—	—	—
Universal serial bus (USB) 2.0 full/low rate	1	1	1	1
Security engine (SEC)	Yes	Yes	—	—

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

Table 2. MPC8272 PowerQUICC II Device Packages

Code (Package)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8272VR	MPC8272ZQ
	MPC8248VR	MPC8248ZQ
	MPC8271VR	MPC8271ZQ
	MPC8247VR	MPC8247ZQ

This figure shows the block diagram of the SoC.

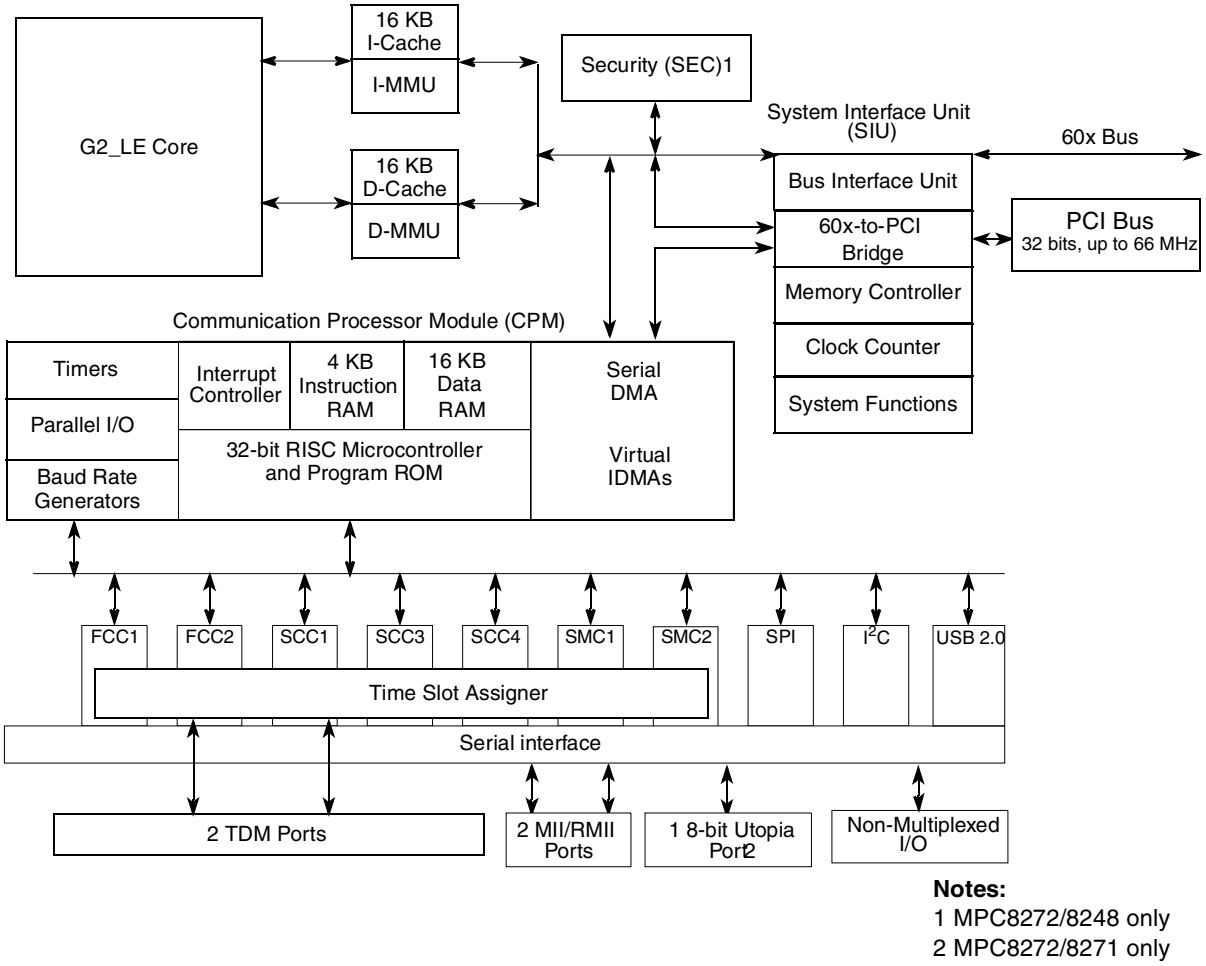

Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the MPC603e microprocessor
  - System core microprocessor supporting frequencies of 266–400 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - Supports bus snooping for cache coherency

  - One of the FCCs supports ATM (MPC8272 and MPC8271 only)—full-duplex SAR at 155 Mbps, 8-bit UTOPIA interface 31 Mphys, AAL5, AAL1, AAL2, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64-K external connections

— Three serial communications controllers (SCCs) identical to those on the MPC860 supporting the digital portions of the following protocols:
  - Ethernet/IEEE 802.3 CDMA/CS
  - HDLC/SDLC and HDLC bus
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous (BiSync) communications
  - Transparent
  - QUICC multichannel controller (QMC) up to 64 channels
    - Independent transmit and receive routing, frame synchronization.
    - Serial-multiplexed (full-duplex) input/output 2048, 1544, and 1536 Kbps PCM highways
    - Compatible with T1/DS1 24-channel and CEPT E1 32-channel PCM highway, ISDN basic rate, ISDN primary rate, and user defined.
    - Subchanneling on each time slot.
    - Independent transmit and receive routing, frame synchronization and clocking
    - Concatenation of any not necessarily consecutive time slots to channels independently for receiver/transmitter
    - Supports H1,H11, and H12 channels
    - Allows dynamic allocation of channels
  - SCC3 in NMSI mode is not usable when USB is enabled.
— Two serial management controllers (SMCs), identical to those of the MPC860
  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
— One serial peripheral interface identical to the MPC860 SPI
— One I^2C controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
— Up to two TDM interfaces
  - Supports one groups of two TDM channels
  - 1024 bytes of SI RAM
— Eight independent baud rate generators and 14 input clock pins for supplying clocks to FCC, SCC, SMC, and USB serial channels
— Four independent 16-bit timers that can be interconnected as two 32-bit timers

This table lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions[1]

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.425 – 575	V
PLL supply voltage	VCCSYN	1.425 – 575	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T_j	105[2]	°C
Ambient temperature	T_A	0–70[2]	°C

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A}$ – 105_{T_j}.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

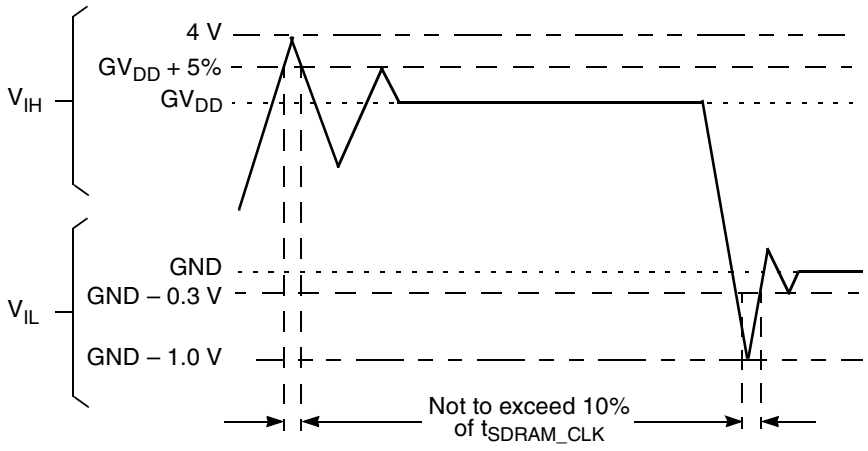

Figure 2. Overshoot/Undershoot Voltage

Table 5. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 6.0mA BR BG/IRQ6 ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG/IRQ7 DBB/IRQ3 D[0–63] IRQ3/CKSTP_OUT/EXT_BR3 IRQ4/CORE_SRESET/EXT_BG3 IRQ5/TBEN/EXT_DBG3/CINT PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 BADDR31/IRQ5/CINT CPU_BR/INT_OUT IRQ0/NMI_OUT PORESET/PCI_RST HRESET SRESET RSTCONF	V_{OL}	—	0.4	V

5 MPC8272 and MPC8271 only.

Table 6.

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, TRST and PORESET[1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH[2]	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	μA
Signal low input current, V_{IL} = 0.8 V[3]	I_L	—	1	μA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	μA
Output high voltage, I_{OH} = –2 mA except UTOPIA mode, and open drain pins In UTOPIA mode[4] (UTOPIA pins only): I_{OH} = -8.0mA	V_{OH}	2.4	—	V
In UTOPIA mode[4] (UTOPIA pins only): I_{OL} = 8.0mA	V_{OL}	—	0.5	V

I_{OL} = 6.0mA
BR
BG
ABB/IRQ2
TS
A[0-31]
TT[0-4]
TBST
TSIZE[0–3]
AACK
ARTRY
DBG
DBB/IRQ3
D[0-63]
//EXT_BR3
//EXT_BG3
/TBEN/EXT_DBG3/CINT
PSDVAL
TA
TEA
GBL/IRQ1
CI/BADDR29/IRQ2
WT/BADDR30/IRQ3
BADDR31/IRQ5/CINT
CPU_BR
IRQ0/NMI_OUT
/PCI_RST
HRESET
SRESET
RSTCONF
	V_{OL}	—	0.4	V

4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100/133 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Table 9. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27[2]
Memory controller	45 or 27[2]
Parallel I/O	45
PCI	27

1 These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.
2 Impedance value is selected through SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

This table lists CPM output characteristics.

Table 10. AC Characteristics for CPM Outputs[1]

Spec Number		Characteristic	Value (ns)							
			Maximum Delay				Minimum Delay			
Max	Min		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	5.5	0.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	8	2	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	10	0	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	8	2	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	11	2.5	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	11	0.5	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	11	0.5	0.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

Table 12. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Value (ns)							
			Setup				Hold			
Setup	Hold		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp11	sp10	$\overline{\text{AACK}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{ARTRY}}/\overline{\text{TEA}}$	6	5	3.5	N/A	0.5	0.5	0.5	N/A
sp12	sp10	Data bus in normal mode	5	4	3.5	N/A	0.5	0.5	0.5	N/A
sp13	sp10	Data bus in pipeline mode (without ECC and PARITY)	N/A	4	2.5	1.5	N/A	0.5	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	N/A	0.5	0.5	0.5	N/A

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 13. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Value (ns)							
			Maximum Delay				Minimum Delay			
Max	Min		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	5.5	N/A	1	1	1	N/A
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	4.5[2]	1	1	1	1 [2]
sp33	sp30	Data bus[3]	6.5	6.5	5.5	4.5	0.8	0.8	0.8	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	4.5	1	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	N/A	1	1	1	N/A

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2 Value is for ADD only; other sp32/sp30 signals are not applicable.
3 To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.

Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2]

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0000_011	60.0	80.0	2.5	150.0	200.0	3.5	210.0	280.0	3	50.0	66.7
0000_100	60.0	80.0	2.5	150.0	200.0	4	240.0	320.0	3	50.0	66.7
0000_101	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_110	50.0	66.7	3.5	150.0	200.0	3.5	175.0	233.3	3	50.0	66.7
0000_111	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
Full Configuration Modes											
0001_000	50.0	66.7	3	150.0	200.0	5	250.0	333.3	3	50.0	66.7
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
0100_000	Reserved										

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0000_110	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
Full Configuration Modes											
0001_001	60.0	66.7	2	120.0	133.3	5	150.0	166.7	4	30.0	33.3
0001_010	50.0	66.7	2	100.0	133.3	6	150.0	200.0	4	25.0	33.3
0001_011	50.0	66.7	2	100.0	133.3	7	175.0	233.3	4	25.0	33.3
0001_100	50.0	66.7	2	100.0	133.3	8	200.0	266.6	4	25.0	33.3
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
0010_011	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0011_000	Reserved										
0011_001	Reserved										
0011_010	Reserved										
0011_011	Reserved										
0011_100	Reserved										
0100_000	Reserved										
0100_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0100_010	50.0	66.7	3	150.0	200.0	3.5	175.0	200.0	3	50.0	66.7
0100_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7
0100_100	50.0	66.7	3	150.0	200.0	4.5	225.0	300.0	3	50.0	66.7
0101_000	50.0	66.7	5	250.0	333.3	2.5	250.0	333.3	2.5	100.0	133.3
0101_001	50.0	66.7	5	250.0	333.3	3	300.0	400.0	2.5	100.0	133.3
0101_010	50.0	66.7	5	250.0	333.3	3.5	350.0	466.6	2.5	100.0	133.3
0101_011	50.0	66.7	5	250.0	333.3	4	400.0	533.3	2.5	100.0	133.3
0101_100	50.0	66.7	5	250.0	333.3	4.5	450.0	599.9	2.5	100.0	133.3
0101_101	50.0	66.7	5	250.0	333.3	5	500.0	666.6	2.5	100.0	133.3
0101_110	50.0	66.7	5	250.0	333.3	5.5	550.0	733.3	2.5	100.0	133.3
0110_000	Reserved										
0110_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
0110_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
0110_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
0110_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
0111_000	50.0	66.7	3	150.0	200.0	2	150.0	200.0	2	75.0	100.0
0111_001	50.0	66.7	3	150.0	200.0	2.5	187.5	250.0	2	75.0	100.0
0111_010	50.0	66.7	3	150.0	200.0	3	225.0	300.0	2	75.0	100.0
0111_011	50.0	66.7	3	150.0	200.0	3.5	262.5	350.0	2	75.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_010	Reserved										
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1011_101	25.0	50.0	8	200.0	400.0	2.5	250.0	500.0	2	100.0	200.0
1011_110	25.0	50.0	8	200.0	400.0	3	300.0	600.0	2	100.0	200.0
1011_111	25.0	50.0	8	200.0	400.0	3.5	350.0	700.0	2	100.0	200.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D15		G3
D16		AB3
D17		Y1
D18		T4
D19		T3
D20		P2
D21		M1
D22		J1
D23		G4
D24		AB2
D25		W4
D26		V2
D27		T1
D28		N5
D29		L1
D30		H1
D31		G5
D32		W5
D33		W2
D34		T5
D35		T2
D36		N1
D37		K3
D38		H2
D39		F1
D40		AA2
D41		W1
D42		U3
D43		R2
D44		N2
D45		L2

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	**MPC8272/MPC8271 Only**	
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UT\_TXENB}}$	G22[3]
PB18/FCC2_MII_HDLC_RXD3		T25[3]
PB19/FCC2_MII_HDLC_RXD2		P22[3]
PB20/FCC2_MII_HDLC_RMII_RXD1		L25[3]
PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD		J26[3]
PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0		U23[3]
PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1		U26[3]
PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2		M24[3]
PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2		M23[3]
PB26/FCC2_MII_CRS/L1RXDB2		H24[3]
PB27/FCC2_MII_COL/L1TXDB2		E25[3]
PB28/FCC2_MII_RMII_RX_ER/$\overline{\text{FCC2\_RTS}}$/TXD1		D26[3]
PB29/FCC2_MII_RMII_TX_EN		K21[3]
PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV		D24[3]
PB31/FCC2_MII_TX_ER		E23[3]
PC0/$\overline{\text{DREQ3}}$/BRGO7/$\overline{\text{SMSYN1}}$/L1CLKOA2		AF23[3]
PC1/BRGO6/$\overline{\text{L1RQA2}}$		AD23[3]
PC4/SMRXD1/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$		AB22[3]
PC5/SMTXD1/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$		AE24[3]
PC6/$\overline{\text{FCC1\_CD}}$/SI2_L1ST2	FCC1_UT_RXADDR2	AF24[3]
PC7/$\overline{\text{FCC1\_CTS}}$	FCC1_UT_TXADDR2	AE26[3]
PC8/$\overline{\text{CD4}}$/RTS1/SI2_L1ST2/$\overline{\text{CTS3}}$		AC24[3]
PC9/$\overline{\text{CTS4}}$/L1TSYNCA2		AA23[3]
PC10/$\overline{\text{CD3}}$/USB_RN		AB25[3]
PC11/$\overline{\text{CTS3}}$/USB_RP/L1TXD3A2		V22[3]
PC12	FCC1_UT_RXADDR1	AA26[3]
PC13/BRGO5	FCC1_UT_TXADDR1	V23[3]
PC14/$\overline{\text{CD1}}$	FCC1_UT_RXADDR0	W24[3]
PC15/$\overline{\text{CTS1}}$	FCC1_UT_TXADDR0	U24[3]
PC16/CLK16		T23[3]

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
PC17/CLK15/BRGO8/$\overline{\text{DONE2}}$		T26[3]
PC18/CLK14/$\overline{\text{TGATE2}}$		R26[3]
PC19/CLK13/BRGO7/$\overline{\text{TGATE1}}$		P24[3]
PC20/CLK12/$\overline{\text{USBOE}}$		L26[3]
PC21/CLK11/BRGO6/CP_INT		L24[3]
PC22/CLK10/$\overline{\text{DONE3}}$	FCC1_UT_TXPRTY	L23[3]
PC23/CLK9/BRGO5/$\overline{\text{DACK3}}$/$\overline{\text{CD1}}$		K24[3]
PC24/CLK8/TIN3/$\overline{\text{TOUT4}}$/DREQ2/BRGO1		K23[3]
PC25/CLK7/BRGO4/$\overline{\text{DACK2}}$/SPISEL		F26[3]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK		H23[3]
PC27/CLK5/BRGO3/$\overline{\text{TOUT1}}$	FCC1_UT_RXPRTY	K22[3]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/SPICLK		D25[3]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$		F24[3]
PD7/SMSYN2	FCC1_UT_TXADDR3	AB21[3]
PD14/I2CSCL		AC26[3]
PD15/I2CSDA		Y23[3]
PD16/SPIMISO	FCC1_UT_TXPRTY	AA25[3]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	Y26[3]
PD18/SPICLK	FCC1_UT_RXADDR4	W25[3]
PD19/SPISEL/BRGO1	FCC1_UT_TXADDR4	V25[3]
PD20/$\overline{\text{RTS4}}$/L1RSYNCA2		R24[3]
PD21/TXD4/L1RXD0A2		P23[3]
PD22/RXD4/L1TXD0A2		N25[3]
PD23/$\overline{\text{RTS3}}$/USB_TP		K26[3]
PD24/TXD3/USB_TN		K25[3]
PD25/RXD3/USB_RXD		J25[3]
PD29/$\overline{\text{RTS1}}$	FCC1_UT_RXADDR3	C26[3]
PD30/TXD1		E24[3]
PD31/RXD1		B25[3]
VCCSYN		C18
VCCSYN1		K6

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.2	12/2003	• Table 1: New • Table 2: New • Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V • Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) • Table 8 and Table 21: Addition of muxed signals CPCI_HS_ES to PCI_REQ1 (AF14) CPCI_HS_LED to PCI_GNT1 (AE13) CPCI_HS_ENUM to PCI_GNT2 (AF21) • Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices: PCI_CFG0 (PCI_HOST_EN) (AC21) PCI_CFG1 (PCI_ARB_EN) (AE22) PCI_CFG2 (DLL_ENABLE) (AE23) PCI_PAR (AF12) PCI_FRAME (AD15) PCI_TRDY(AF16) PCI_IRDY (AF15) PCI_STOP (AE15) DEVSEL (AE14) PCI_IDSEL (AC17) PCI_PERR (AD14) PCI_SERR (AD13) PCI_REQ0–2 (AAE20, AF14, AB14) PCI_GNT0–2 (AD20, AE13, AF21) PCI_RST (AF22) PCI_INTA (AE21) PCI_C0-3 (AE12, AF13, AC15, AE18) PCI_AD0-31 • Table 8 and Table 21: Corrected assertion level (added "‾") PCI_HOST_EN (AC21) and PCI_ARB_EN (AE22) • Table 7: Addition of $R_{\theta JT}$ and note 4 • Sections 4.1–4.5 and 4.7 on thermal characteristics: New • Section 7, "Clock Configuration Modes": Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family. • Addition of "Note: Temperature Reflow for the VR Package" on page 56 • Table 21: Addition of note 2 to TRST (E21) and PORESET (C24) • Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now "No connects." Note 4 unchanged. • Table 21: Removal of Spare0 (AD24). This pin is now a "No connect." Note 5 unchanged. • Table 21: Addition of PCI_MODE (AD22). This pin was previously listed as "Ground." Addition of note 1.
0.1	9/2003	• Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine) • Table 8: Addition of note 2 to V_{IH} • Table 8: Changed I_{OL} for 60x signals to 6.0 mA • Modification of note 1 for Table 17, Table 18, Table 19, and Table 20 • Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both CS5 and GND. AD8 is only assigned to CS5. • Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3) • Addition of ZQ package code to Figure 15
0	5/2003	NDA release